Instrumentation Amplifier Application Note

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Introduction to the Instrumentation Amplifier

This Application Note describes the Intersil bipolar and MOS input (see Table 1). Instrumentation Amplifiers, theory of operation, advantages, and typical application circuits. These devices are micropower Instrumentation Amplifiers which deliver rail-to-rail input amplification and rail-to-rail output swing on a single 2.4V to 5V supply. These Instrumentation Amplifiers deliver excellent DC and AC specifications while consuming only 60µA typical supply current. Because they provide an independent pair of feedback terminals to set the gain and to adjust output level, these Instrumentation Amplifiers achieve high common-mode rejection ratios regardless of the tolerance of the gain setting resistors. The ISL28271 and ISL28272 have an $\overline{\text{ENABLE}}$ pin to reduce power consumption, typically less than 5.0µA, while the Instrumentation Amplifier is disabled.

TABLE 1.

PART	INPUT STAGE	# OF AMPLIFIERS	MINIMUM CLOSED LOOP GAIN	BW (kHz)	$\overline{\text{ENABLE}}$?
EL8170	Bipolar	1	100	192	No
EL8171	PMOS	1	10	450	No
EL8172	PMOS	1	100	170	No
EL8173	Bipolar	1	10	396	No
ISL28270	Bipolar	2	100	240	No
ISL28271	PMOS	2	10	180	Yes
ISL28272	PMOS	2	100	100	Yes
ISL28273	Bipolar	2	10	230	No
ISL28470	Bipolar	2	100	240	No

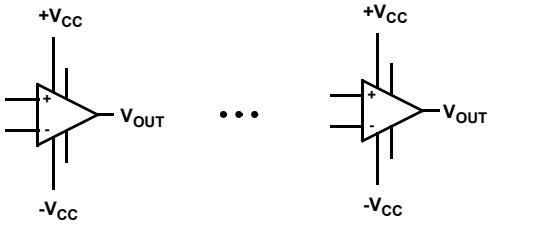

FIGURE 1.

An Instrumentation Amplifier is a confused animal – confused by its cousin, the op amp.

- Its symbol looks like an op amp (see Figure 1)
- It has many of the same basic properties and specifications as an op amp Offset Voltage, Input Bias Current, CMRR, PSRR, etc.
- You can make an Instrumentation Amplifier from a simple op amp circuit.

But the behavior of an Instrumentation Amplifier is profoundly different than an op amp! And it is very difficult to make a precision Instrumentation Amplifier from a simple op amp circuit – many have tried, but most have failed.

An Instrumentation Amplifier provides a voltage subtraction block followed by a fixed gain block; i.e.

$$V_{OUT} = (IN+ - IN-) \times Gain \quad \text{(EQ. 1)}$$

Often, there is an optional output reference input which allows the output voltage to be shifted by a fixed voltage:

$$V_{OUT} = (IN+ - IN-) \times Gain + V_{REF} \quad \text{(EQ. 2)}$$

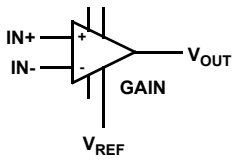

FIGURE 3.

In contrast, an op amp by definition only provides extremely high gain with provisions to apply negative feedback to establish a fixed gain or unique transfer function, H(s), such as an integrator or filter.

Review of Standard Instrumentation Amplifier Design Techniques

Difference Amplifier

In its most basic topology, an Instrumentation Amplifier can be configured from a single op amp and four resistors as shown in Figure 4; this is often referred to as a Difference Amplifier.

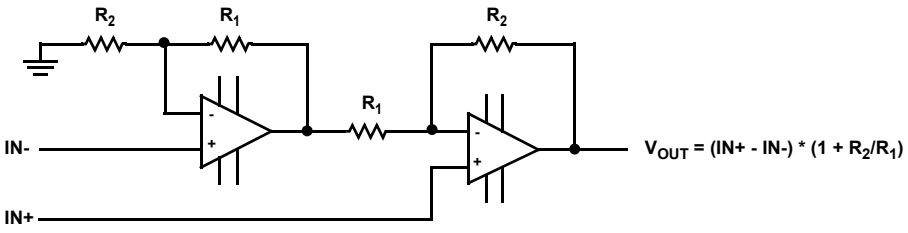

FIGURE 2. TWO OP AMP INSTRUMENTATION AMPLIFIER

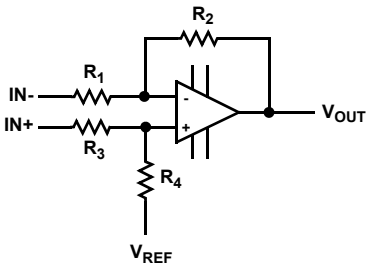

FIGURE 4.

In this configuration, the gain is set by resistors R_1 and R_2:

$$Gain = R_2/R_1 \quad \text{(EQ. 3)}$$

$$V_{OUT} = (IN+ - IN-) \times Gain + V_{REF} \quad \text{(EQ. 4)}$$

For the ability to reject a voltage that appears on both IN- and IN+ (i.e., common mode voltage), resistor values must match such that $R_1 = R_3$ and $R_2 = R_4$. The common mode rejection ratio (CMRR) is set by the matching ratio of R_1:R_3 and R_2:R_4. High common mode rejection ratio requires a very high degree of ratio matching.

It can be shown that the CMRR is:

$$CMRR = 20 \times \log_{10}(x) \quad \text{(EQ. 5)}$$

$$\text{Where } x = R_4/(R_3 + R_4) \times (R_1 + R_2)/R_1 - R_2/R_1 \quad \text{(EQ. 6)}$$

Worse case CMRR occurs when the tolerance of R_4 and R_1 are at their maximum, and R_2 and R_3 are at their minimum value. The following table shows the relationship between resistor tolerance and CMRR for gains of 1, 10, and 100.

TABLE 2.

RESISTOR	CMRR		
TOLERANCE	GAIN =1	GAIN = 10	GAIN =100
±5%	-20.4dB	-15.6dB	-14.8dB
±1%	-34.1dB	-28.9dB	-28.1dB
±0.1%	-54.0dB	-48.8dB	-48.0dB
±0.01%	-74.0dB	-68.8dB	-68.0dB

The Difference Amplifier has the advantage of simplicity and the ability to operate with high common mode voltage on its inputs, IN+ and IN-. However, the input resistance is set by the resistor values R_3 and R_4, and does not provide high input resistance as is common in most Instrumentation Amplifier circuits.

Additionally, the REF input must be driven by a very low source impedance since the CMRR will be degraded by any source resistance that contributes to the value of R_4 and causes increased mismatch between R_2 and R_4.

Also note that the common mode voltage will bias internal nodes at a voltage that is set by the ratio of R_3 and R_4, or the gain of the circuit. For example, in Figure 5, for a gain of 100 and a common voltage of 10V, the inputs to the op amp will be sitting at a voltage of 9.9V. This circuit would not be possible if the op amp was operated with V_{CC} of +5V since the op amp input's voltage would exceed the supply voltage.

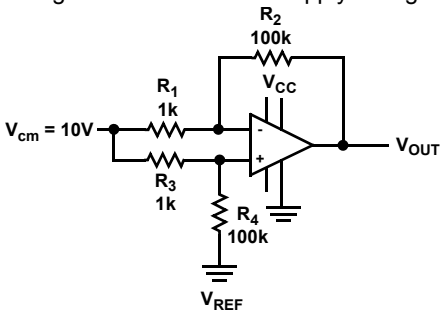

FIGURE 5.

Two Amplifier Instrumentation Amplifier

To provide a high input impedance, a two amplifier Instrumentation Amplifier can be used as in Figure 6.

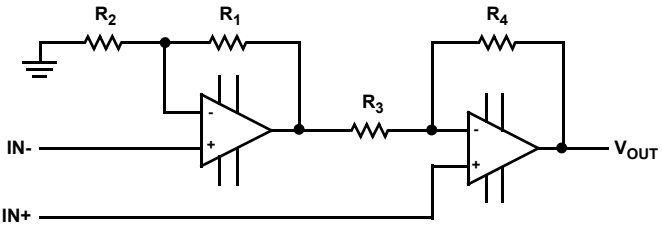

FIGURE 6. TWO AMPLIFIER INSTRUMENTATION AMPLIFIER

In this configuration, the gain is set by resistors R_3 and R_4:

$$Gain = 1 + R_4/R_3 \quad \text{(EQ. 7)}$$

$$V_{OUT} = (IN+ - IN-) \times Gain \quad \text{(EQ. 8)}$$

The ability to reject a voltage that appears on both IN- and IN+ (i.e., common mode voltage), depends on matched resistor values such that, $R_1 = R_3$ and $R_2 = R_4$. The common mode rejection ratio (CMRR) is set by the matching ratio of R_1:R_3 and R_2:R_4, and, high CMRR requires a very high degree of ratio matching. For example, with 10V of common mode voltage, resistor tolerance's must be at least ±0.01% to achieve 12-bit accuracy (72dB).

Classic Three Amplifier Instrumentation Amplifier

By adding a third op amp, the "Classic Three Amplifier Instrumentation Amplifier" can be configured as shown in Figure 7.

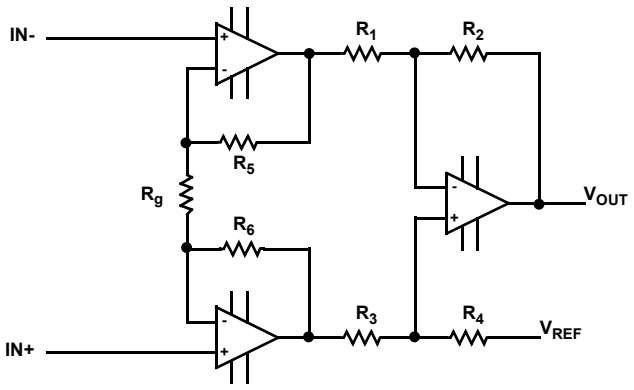

FIGURE 7. CLASSIC THREE AMPLIFIER INSTRUMENTATION AMPLIFIER

Usually, resistors R_1 through R_6 are equal value resistors of R and the gain:

$$Gain = (1 + 2 \times R / R_{gain}) \quad \text{(EQ. 9)}$$

$$V_{OUT} = (IN+ - IN-) \times Gain + V_{REF} \quad \text{(EQ. 10)}$$

With this circuit, the Gain can be set with a single resistor, R_{GAIN} and the input impedance is very high. However, the common mode rejection ratio, CMRR, just like the Difference Amplifier topology, is still set by the resistor matching between R_1, R_2, R_3, and R_4. Extremely low tolerance resistors or precision resistor trimming is required to achieve high CMRR. The equations and Table shown for the Difference Amplifier apply directly to the Classic Three Amplifier Instrumentation Amplifier configuration.

Monolithic Instrumentation Amplifier Architecture

Each of the three basic Instrumentation Amplifier architectures that have been already discussed have been implemented in standard integrated circuit packages. To achieve a high CMRR, extensive resistor trimming is required with lasers or other suitable techniques. While each of these devices provide adequate specifications for a precision Instrumentation Amplifier, each device has its own compromise based on operating voltage range, supply current, common mode operating range, input impedance, etc. These instrumentation amplifiers use one external resistor to set the gain; while this may seem to be an advantage, there are considerations which make the single resistor configuration undesirable from a design viewpoint. The temperature coefficient (TC) of the external resistor will be a direct gain drift. Also, an external filter can not be applied to the feedback network because it is internal to the device.

Introduction to Instrumentation Amplifier Product Family

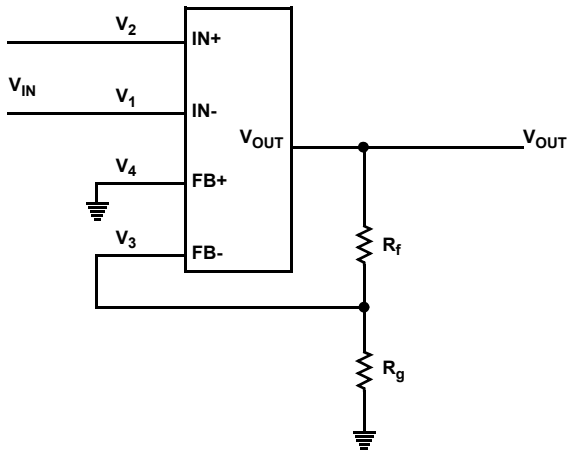

FIGURE 8. TWO AMPLIFIER INSTRUMENTATION AMPLIFIER

This Application Note describes the Intersil Instrumentation Amplifier Product Family, which includes the following features:

1. Bipolar transistor inputs for low voltage noise
2. PMOS transistor inputs for low input bias current
3. Micropower operation requiring only 60µA supply current
4. Rail-to-rail inputs and rail-to-rail output swing
5. Single supply operation from 2.4V to 5V supply
6. An independent pair of feedback terminals to set the gain and to adjust output level allow these Instrumentation Amplifier to achieve high CMRR (>104dB) regardless of the tolerance of the gain setting resistors.
7. Internal loop compensation to provide optimum bandwidth trade-off as shown in Table 1
8. The ISL28271 and ISL28272 have an $\overline{\text{ENABLE}}$ pin to reduce the supply current to a typical of less than 5µA and tri-state the output stage to a high impedance state.

Instrumentation Amplifier Specifications

Many of the Instrumentation Amplifier specifications are very similar to the standard specifications for operational amplifiers. However, the unique architecture of the Intersil Instrumentation Amplifiers make some of these specifications differ slightly. Table 3 summarizes the Specifications and Features of the Instrumentation Amplifier Product Family.

TABLE 3.

PARAMETERS	EL8170	ISL28270	ISL28470	EL8173	ISL28273	EL8171	ISL28271	EL8172	ISL28272	UNITS
Input Stage	Bipolar			Bipolar		PMOS		PMOS		
Minimum Gain	100			10		10		100		
Gain Set	2 Ext R			2 Ext R		2 Ext R		2 Ext R		
Supply Current: Enabled per Channel	65			65		65	60	65	60	µA
Supply Current: Shutdown	-	-	-	-		-	4	-	4	µA
Minimum V_{CC}	2.4			2.4		2.4		2.4		V_{DC}
Maximum V_{CC}	5.5			5.5		5.5		5.5		V_{DC}
Input Offset Voltage	200	150	150	1000	600	1500	600	300	500	µV
Offset Drift	0.24	0.7	0.7	2.5	0.7	1.5	0.7	0.14	0.7	µV/°C
Input Bias Current, Maximum	3000	2000	2500	2000	2500	50	30	50	30	pA
Input Offset Current, Maximum	2000			2000		25	30	25	30	pA
Input Bias Current Cancellation	Yes			Yes		-		-		
Bandwidth (-3dB) at A_V = 10	-			396	265	450	180	-		kHz
Bandwidth (-3dB) at A_V = 100	192	240	240	-		-		170	100	kHz
Slew Rate (Typ)	0.55	0.5	0.5	0.55	0.6	0.55	0.5	0.55	0.5	V/µs
Rail-to-Rail Input	Yes			Yes		Yes		Yes		
Rail-to-Rail Output	Yes			Yes		Yes		Yes		
Output Current Limit, V+ = 5V	±26	±29	±29	±26	±29	±26		±26		mA
Output in Shutdown Mode	-			-		-	HiZ	-	HiZ	
Gain Accuracy	±0.35	±0.5	±0.5	±0.1	±0.12	±0.15	0.08	±0.2	-0.19	%
CMRR (Typ)	114	110	110	106	110	100		100		dB
PSRR (Typ)	106	110	110	90	95	90	100	100		dB
e_N at 1kHz	58	60	60	220	210	220	240	80	78	nv/√Hz
e_N 0.1Hz to 10Hz	3.5			3.6	3.5	14	10	10	6	μV_{P-P}
Input Protection - Diodes to Rails	Yes			Yes		Yes		Yes		
Input Protection - Diodes across Inputs	Yes			No		No		No		
Max Input Diode Current	5			5		5		5		mA
Package	SO8			SO8		SO8		SO8		
Operating Temp. Range	-40 to +85			-40 to +85		-40 to +85		-40 to +85		°C
RoHS Compliant	Yes			Yes		Yes		Yes		

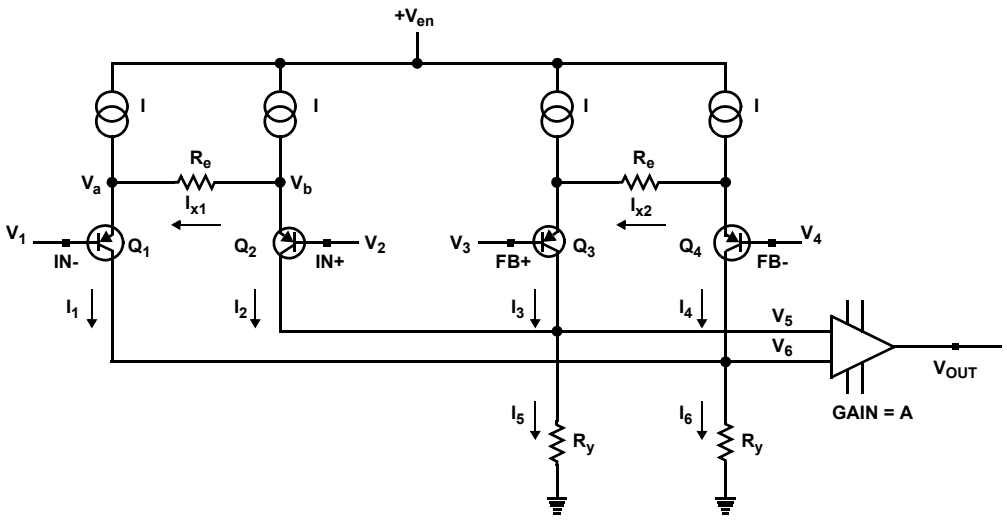

FIGURE 9. SIMPLIFIED SCHEMATIC

Instrumentation Amplifier Product Family Theory of Operation

Each of the features specifications of the Intersil Instrumentation Amplifier Product Family will be discussed in more detail in a future section of this Application Note, but first, let's study the internal operation of this unique Instrumentation Amplifier Product Family.

A simplified schematic is shown in Figure 9.

$$I_{x1} = \frac{(V_2 + V_{be2}) - (V_1 + V_{be1})}{R_e}, \text{ and since } V_{be1} = V_{be2}$$

$$I_{x1} = \frac{V_2 - V_1}{R_e} \quad \text{(EQ. 11)}$$

Assuming β high transistors:

$$I_1 = I + I_{x1} = I + (V_2 - V_1)/R_e \quad \text{(EQ. 12)}$$

$$I_2 = I - I_{x1} = I - (V_2 - V_1)/R_e \quad \text{(EQ. 13)}$$

Similarly for Q_3 and Q_4:

$$I_3 = I + I_{x2} = I + (V_4 - V_3)/R_e \quad \text{(EQ. 14)}$$

$$I_4 = I - I_{x2} = I - (V_4 - V_3)/R_e \quad \text{(EQ. 15)}$$

Summing currents:

$$I_5 = I_2 + I_3 = I - (V_2 - V_1)/R_e + I + (V_4 - V_3)/R_e \quad \text{(EQ. 16)}$$

$$I_5 = 2 \times I + (V_1 - V_2)/R_e + (V_4 - V_3)/R_e \quad \text{(EQ. 17)}$$

$$I_6 = I_1 + I_4 = I + (V_2 - V_1)/R_e + I - (V_4 - V_3)/R_e \quad \text{(EQ. 18)}$$

$$I_6 = 2 \times I + (V_2 - V_1)/R_e + (V_3 - V_4)/R_e \quad \text{(EQ. 19)}$$

$$V_5 = I_5 \times R_y = 2 \times R_y \times I + (V_1 - V_2) \times R_y/R_e + (V_4 - V_3) \times R_y/R_e \quad \text{(EQ. 20)}$$

$$V_6 = I_6 \times R_y = 2 \times R_y \times I + (V_2 - V_1) \times R_y/R_e + (V_3 - V_4) \times R_y/R_e \quad \text{(EQ. 21)}$$

$$V_{OUT} = A \times (V_5 - V_6) \quad \text{(EQ. 22)}$$

where A is the gain of the output stage

Assume $R_y/R_e = 1$ (i.e., R_e and R_y are equal value).

$$V_{OUT} = A \times [2 \times R_y \times I + (V_1 - V_2) + (V_4 - V_3) - [2 \times R_y \times I + (V_2 - V_1) + (V_3 - V_4)]] \quad \text{(EQ. 23)}$$

$$V_{OUT} = A \times [(V_1 - V_2) + (V_4 - V_3) + (V_1 - V_2) + (V_4 - V_3)] \quad \text{(EQ. 24)}$$

$$V_{OUT} = 2 \times A \times [(V_1 - V_2) + (V_4 - V_3)] \quad \text{(EQ. 25)}$$

$$V_{OUT}/(2 \times A) = [(V_1 - V_2) + (V_4 - V_3)] \quad \text{(EQ. 26)}$$

Since A is very large:

$$V_{OUT}/(2 \times A) \Rightarrow 0 \quad \text{(EQ. 27)}$$

$$0 = (V_1 - V_2) + (V_4 - V_3) \quad \text{(EQ. 28)}$$

Let $V_{IN} = V_2 - V_1$, and $V_3 = FB+$, $V_4 = FB-$

$$0 = -V_{IN} + (FB- - FB+) \quad \text{(EQ. 29)}$$

$$V_{IN} + FB- - FB+ \quad \text{(EQ. 30)}$$

or

$$IN+ - IN- = FB- - FB+ \quad \text{(EQ. 31)}$$

As you can see from Equation 31, negative feedback is applied around the amplifier so that the voltage applied to the feedback terminals (FB+ - FB-) must be equal to the voltage applied to the input terminals (IN+ - IN-).

For the standard data sheet connection:

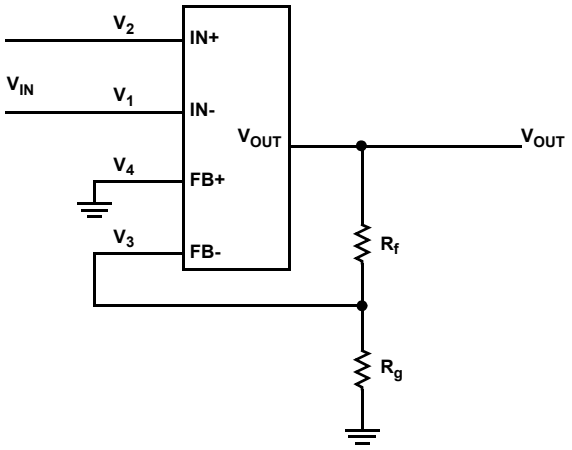

FIGURE 10. TWO AMPLIFIER INSTRUMENTATION AMPLIFIER

$$FB+ = 0V$$
$$FB- = V_{OUT} \times R_g/(R_g + R_f)$$
$$V_{IN} = FB- - FB+$$
$$V_{IN} = V_{OUT} \times R_g/(R_g + R_f) - 0$$
$$V_{OUT} = V_{IN} \times (1 + R_f/R_g) \quad \text{(EQ. 32)}$$

Features of Instrumentation Amplifier Product Family

A simplified schematic and block diagram is shown in Figure 11 to illustrate the rail-to-rail operation for both the input stage and the output stage. The same schematic applies to the PMOS input devices when the PNP transistors (Q_1 to Q_4) are replaced with P-Channel MOSFETs for ultra-low input bias current.

The input terminals (IN+ and IN-) and feedback terminals (FB+ and FB-) are single differential pair devices aided by an Input Range Enhancement Circuit to increase the headroom of operation of the common-mode input voltage. As a result, the input common-mode voltage range for all these Instrumentation Amplifiers is rail-to-rail. The parts are able to handle input voltages that are at or slightly beyond the supply and ground making these in-amps well suited for single 5V or 3.3V low voltage supply systems. There is no need then to move the common-mode input voltage of the these Instrumentation Amplifiers to achieve symmetrical input voltage.

The use of a bipolar transistor input stage vs. the MOSFET input stage allows the user to choose low bias current, high input resistance.

Rail-to-rail operation for both the inputs and outputs is an important and unique feature. The rail-to-rail inputs allow the input voltages to be slightly below the V_S- rail (typically Ground) to slightly above the V_S+ rail.

The conventional technique to achieve a rail-to-rail input stage is to use two separate input stages, as shown in Figure 12. One input stage (Q_1 and Q_2) provides common mode input range to the top rail (V_S+), and the other input stage (Q_3 and Q_4) provides common mode input range to the bottom rail.

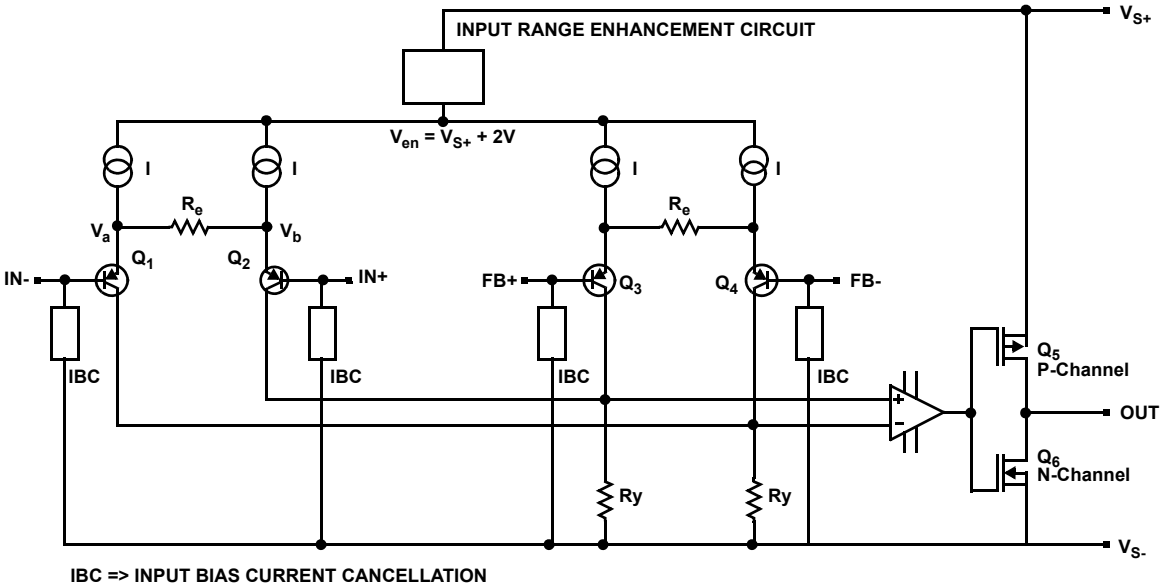

FIGURE 11. SIMPLIFIED SCHEMATIC

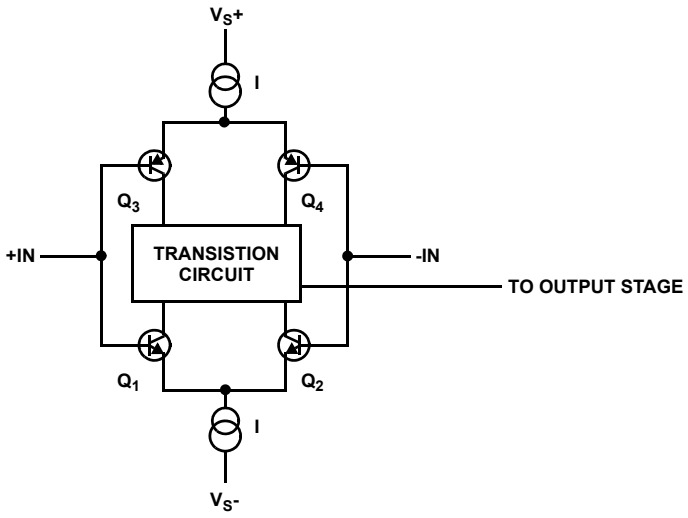

FIGURE 12. 2 AMPLIFIER INSTRUMENTATION AMPLIFIER

Unless the input stages transistors are exactly matched, changes in offset voltage and input bias current will result as the common mode input range transitions between the two input stages.

In contrast, the Product Family uses a single input stage for the IN inputs and a single input stage for the FB inputs. An Input Range Enhancement Circuit (IREC) provides a bias voltage that is approximately 2V above the VS+ rail which is used to bias the I current sources shown in the Block Diagram. Since there is a single input stage, there is no input stage transition point to create shifts in offset voltage and bias current as the input common mode voltage changes.

The effectiveness of the Single Input Stage and IREC circuit technique is evident as shown in the following Figures for the offset voltage of a EL8170 (Figure 13) and a typical rail-to-rail input amplifier (Figure 14).

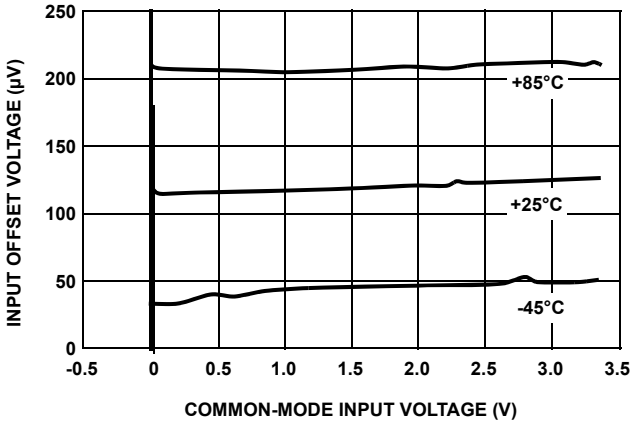

FIGURE 13. EL8170

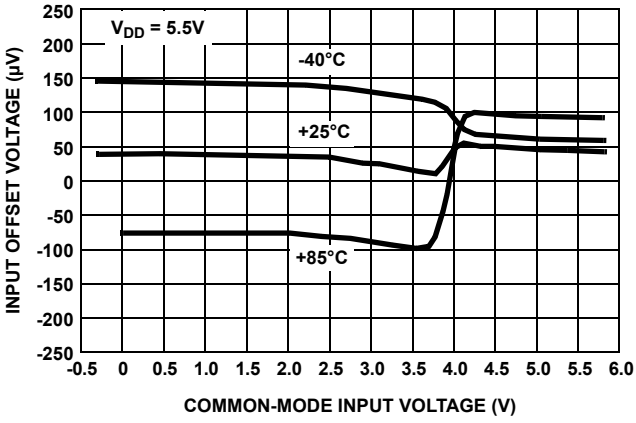

FIGURE 14. TYPICAL RAIL-TO-RAIL INPUT AMPLIFIER

In addition to shifts in offset voltage as the input common mode voltage changes, the input bias current will change dramatically as the input stages transition from a PNP transistor input stage to a NPN transistor input stage. The following graphs compare the input bias current over the common mode input range for the EL8170 (Figure 15) and a typical rail-to-rail input amplifier (Figure 16).

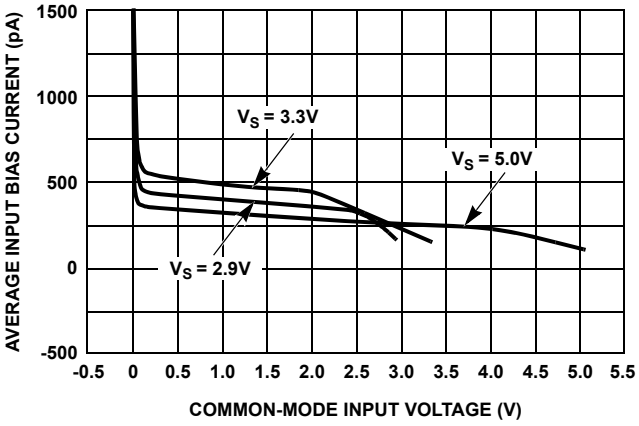

FIGURE 15. EL8170

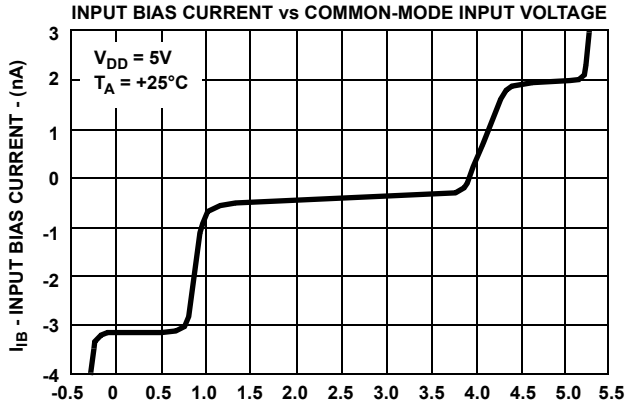

FIGURE 16. TYPICAL RAIL-TO-RAIL INPUT AMPLIFIER

The PNP input stage transistors are biased with an adequate amount of current for speed, and consequently, their base current increases. In order to keep the input bias current low, an Input Bias Current Cancellation Circuit is used to apply and equal but opposite compensation current to the inputs. This compensation current subtracts from the base currents, and the resulting input bias current is reduced to typically around 500pA. This is shown in Figure 17 for the IN+ and IN- inputs, where the FB+ and FB- are identical for proper matching between stages. The compensation current, (I_{comp}) is derived from the IBC circuit and is equal to the base current of Q_1 and Q_2.

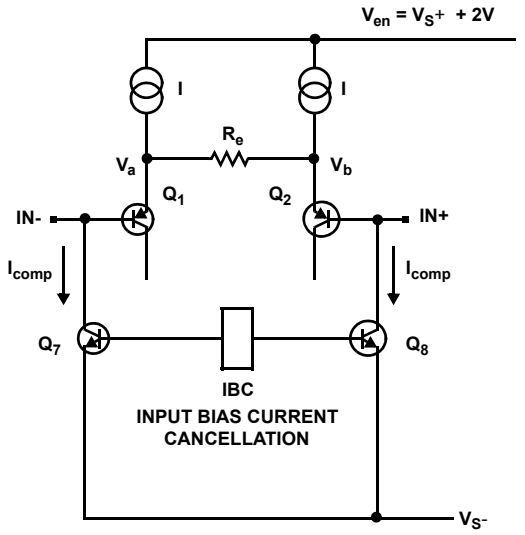

FIGURE 17. INPUT BIAS CURRENT CANCELLATION CIRCUIT

Input Bias Current Cancellation Circuit is typically active from 10mV above the negative rail (V_S-) up to the positive rail (V_S+).

Not only does the Input Bias Current Cancellation compensation circuit keep the input bias current very small, it also maintains a very small input bias current variation over a wide operating range as shown in Figure 18 for +25°C to +85°C.

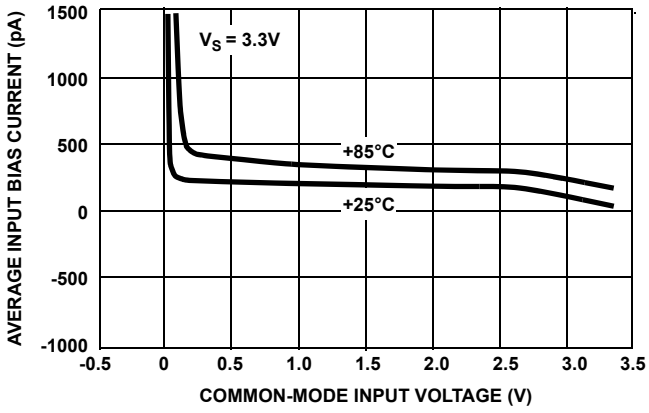

FIGURE 18.

The operating voltage range of the Instrumentation Amplifier product family is from 2.4V to 5.5V making it ideally suited for operation on 3.3V or 5V power supplies. Also, it will operate with a single 4.2 lithium ion battery. Additionally, they are well suited for battery operation since the supply current is only 66µA maximum.

Another unique feature built into the ISL28271 and ISL28272 is the ability to tri-state the output stage to a high impedance state when the part is disabled via the $\overline{\text{ENABLE}}$ pin. This allows several outputs to be wired together for a multiplexer function. This feature will be shown in the Applications section.

Because the Instrumentation Amplifier product family provides an independent pair of feedback terminals to set the gain and to adjust output level, these Instrumentation Amplifiers achieve high CMRR regardless of the tolerance of the gain setting resistors. The FB+ pin can be used as a REF terminal to center or to adjust the output voltage. Because the FB+ pin is a high impedance input, an economical resistor divider can be used to set the voltage at the REF terminal without degrading or affecting the CMRR performance. Any voltage applied to the REF terminal will shift the output voltage by V_{REF} times the closed loop gain, which is set by resistors R_F and R_G.

Since the feedback terminals are differential inputs, they can be used in applications such as current sources for a true Kelvin sense of the feedback voltage. In addition, a complex network can be placed in the feedback path for frequency shaping and filter circuits.

The basic Instrumentation Amplifier configuration is shown in Figure 19:

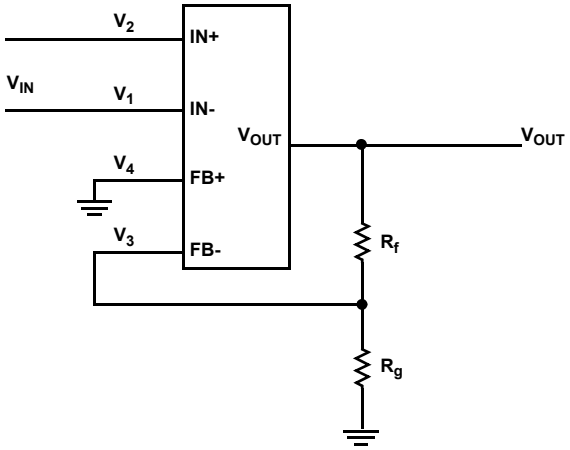

FIGURE 19. TYPICAL RAIL-TO-RAIL INSTRUMENTATION AMPLIFIER

The gain of this circuit is set by the ratio of R_f and R_g such that:

$$V_{OUT} = V_{IN} \times (1 + R_f/R_g) \quad \text{(EQ. 33)}$$

In this configuration, adjustable gain is possible with external resistors for gains from unity up to 10,000. Two external gain setting resistors are used to minimize temperature coefficient (TC) mismatch as is common with a single gain setting resistor.

Notice that resistor value mismatches only effect the gain, and CMRR is not degraded by resistor mismatches as is the case

with the other basic Instrumentation Amplifier configurations discussed previously.

The feedback terminals can be used to apply a reference voltage to shift the input voltage. These are a high impedance reference input that is not affected by gain. The basic circuit is shown in Figure 20:

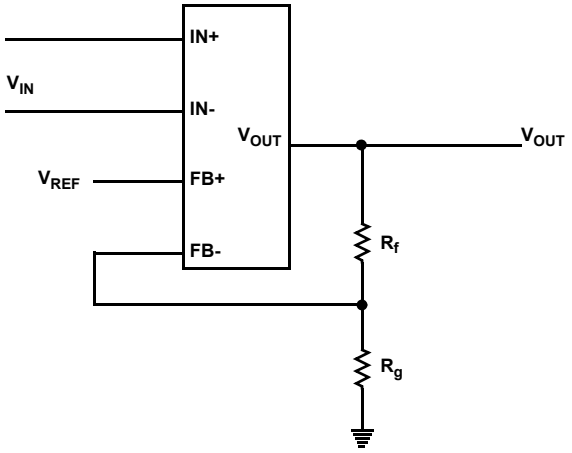

FIGURE 20. BASIC CIRCUIT

If we go back to the equations derived previously:

$$V_{IN} = FB- - FB+ \quad \text{(EQ. 34)}$$

$$V_{IN} = V_{OUT} \times R_g / (R_f + R_g) - V_{REF} \quad \text{(EQ. 35)}$$

$$V_{OUT} = (V_{IN} + V_{REF}) \times (1 + R_f / R_g) \quad \text{(EQ. 36)}$$

Since the FB+ is a high input impedance, a simple resistor divider could be used to set the V_{REF} voltage as shown in Figure 21.

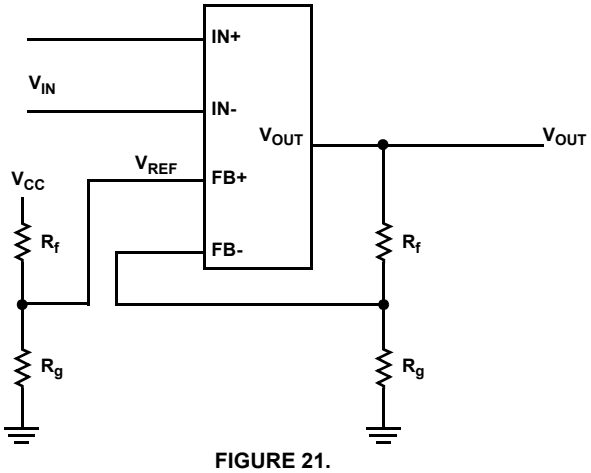

FIGURE 21.

In this case:

$$V_{REF} = V_{CC} \times R_2 / (R_1 + R_2) \quad \text{(EQ. 37)}$$

The feedback terminals can also be used to apply a reference voltage to shift the output voltage as shown in Figure 22 with R_g connected to V_{REF} instead of ground.

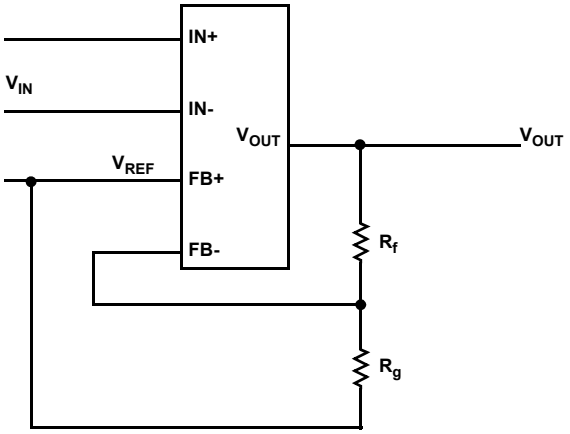

FIGURE 22.

$$V_{IN} = FB- - FB+$$

$$FB- = V_{REF} + R_g \times (V_{OUT} - V_{REF}) / (R_f + R_g)$$

$$V_{IN} = V_{REF} + R_g \times (V_{OUT} - V_{REF}) / (R_f + R_g) - V_{REF}$$

$$V_{OUT} = V_{IN} \times (1 + R_f / R_g) + V_{REF} \quad \text{(EQ. 38)}$$

Since the current in R_g must flow into V_{REF}, the driving point impedance of V_{REF} will effect the accuracy of this configuration. Therefore, V_{REF} should be a low impedance from an op amp, voltage regulator, or voltage reference. Alternately, if a resistor divider is used to obtain V_{REF}, the Thevenin resistance of the divider network must be much lower than the values of R_f and R_g, or the Thevenin resistance must be included in the value of R_g and V_{REF}. However, the CMRR is not affected by the reference voltage or its source resistance.

Care and Feeding of Instrumentation Amplifiers

As in any low voltage, high accuracy measurement system, extreme care must be taken with any of the Instrumentation Amplifiers with respect to grounding scheme, Kelvin sense connections, guarding and shielding, and interface to the digital world. If the PCB connections are made incorrectly, the most perfect measurement circuit can still have errors resulting from poor grounding considerations and not understanding the impact of Ohm's Law. Any analog or mixed signal PCB must have a well thought-out grounding scheme with multiple ground planes or traces. There must be no heavy DC current or AC current in the analog ground planes that connect system measurement points.

A one point measurement system must be established to prevent high currents from interfering with the basic measurement. This is shown in Figure 23 for interfacing a

thermocouple to an A/D Converter. The “High quality measurement Ground” must only connect to the critical ground points in the analog front-end; this ground must make a single point connection to the A/D converter at its Analog Ground pin (AGND). There must be no other connections such as digital grounds or power supply returns to the “High quality measurement Ground” except a single connection at the A/D Converter pins (AGND and DGND). To be sure there is no digital noise introduced into the Analog Ground, the two grounds are tied together at only one point at the A/D Converter. Furthermore, a 0Ω resistor can be used to connect the two grounds; this ensures a separate Net for each ground so the PCB layout software or layout person does not arbitrarily connect the two grounds. The use of a 0Ω resistor is cheap insurance against a noisy and inaccurate analog system! This Thermocouple Circuit will be discussed in more detail in the Applications section.

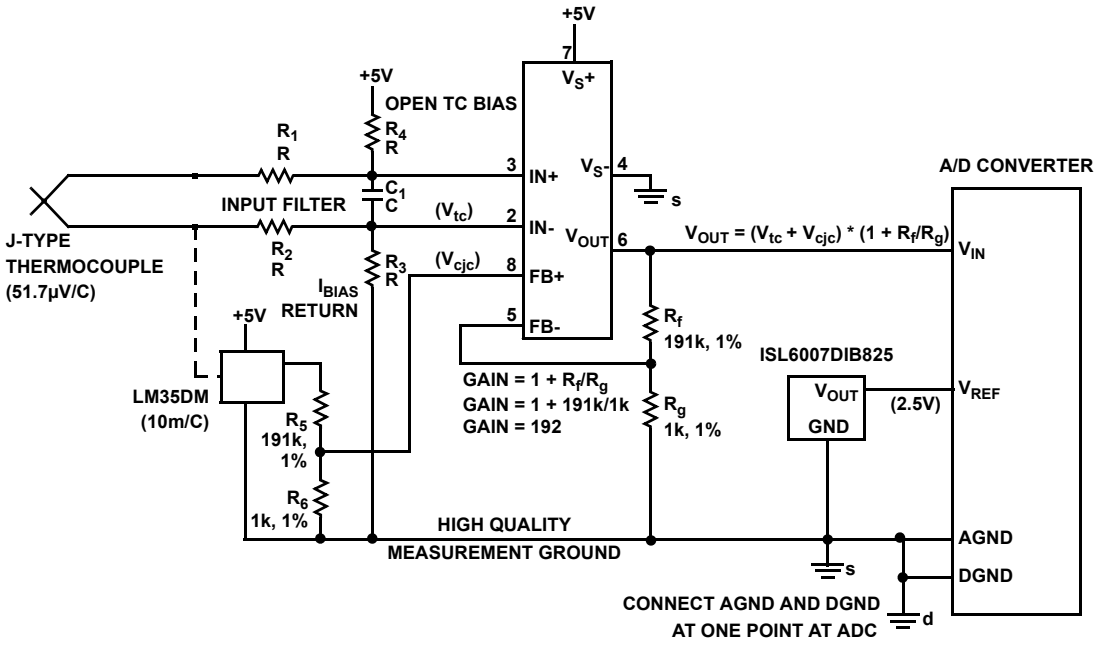

FIGURE 23.

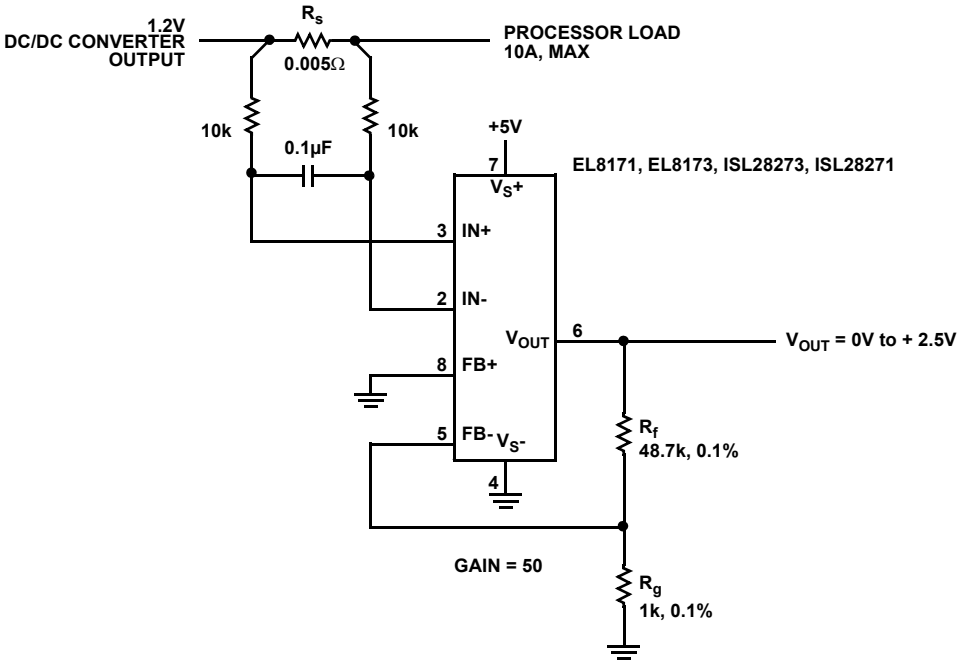

FIGURE 24.

Instrumentation Amplifiers can be used in high accuracy current sense applications as shown in the circuit in Figure 24.

Notice the use of a Kelvin connection shown on the current sense resistor R_s as indicated by the slanted connections to the resistor. To avoid errors caused by IR drops, the connections must be made directly at the leads of the 0.005Ω current sense resistor. Just 1mΩ of contact resistance or PCB trace resistance will cause a 20% error in the current reading.

Guarding and driven guards is a PCB layout technique to reduce errors caused by PCB leakage currents and improve high frequency CMRR. This can be done by surrounding high impedance input leads with traces that are driven by a low source impedance voltage that is equal to the common mode voltage.

At any point in a circuit where dissimilar metals come in contact a small thermocouple voltage is developed. Fortunately, the copper lead frame of a surface mount device is the same copper material as PCB etch, and the thermocouple effect is minimized. However, there are many other places where thermocouples can be generated; for example, across a connector finger, across relay contacts, or even across a resistor! Yes, a poorly constructed resistor can show many µV/°C of thermocouple voltage. It has been found that external components (resistors, contacts, sockets, etc.) can create thermocouple voltages that exceed 10µV/°C.

It must be recognized that thermocouple voltages are developed by the difference in temperature between the two ends of dissimilar metal junctions, and not the absolute ambient temperature. If both ends of the metal junctions are isothermal (i.e., at the same temperature) there is no thermocouple voltage developed. Therefore, the first rule to avoid thermocouple effects is to eliminate hot spots on a PCB (e.g., linear voltage regulators). If hot spots cannot be avoided, then the two ends of metal junctions must be oriented so they are on isothermal lines on the PCB.

The second rule to minimize thermocouple effects is to balance the number of junctions in a loop so that the error voltages are cancelled or become a common mode voltage that is reduced by the CMRR of the op amps in the signal chain. If the number of junctions are not balanced, then it may be necessary to create a junction by adding a series resistor that has no effect on circuit operation but balances the number of junctions.

Unknown to most design engineers is the danger of internal clipping when operating an instrumentation amplifier on a single supply. Unfortunately, the internal nodes are invisible to the user and impossible to measure; manufacturer's data sheets often ignore the issue, or they have obscure "typical characteristics" graphs or misleading paragraphs that attempt to explain the phenomena. Since the Instrumentation Amplifiers operate in a current summing mode as explained in the "Instrumentation Amplifier Product Family Theory of Operation" on page 6 there is no possibility of internal clipping.

If we review the classic three amplifier instrumentation amplifier configuration shown in Figure 25, the effect of internal clipping can be clearly shown.

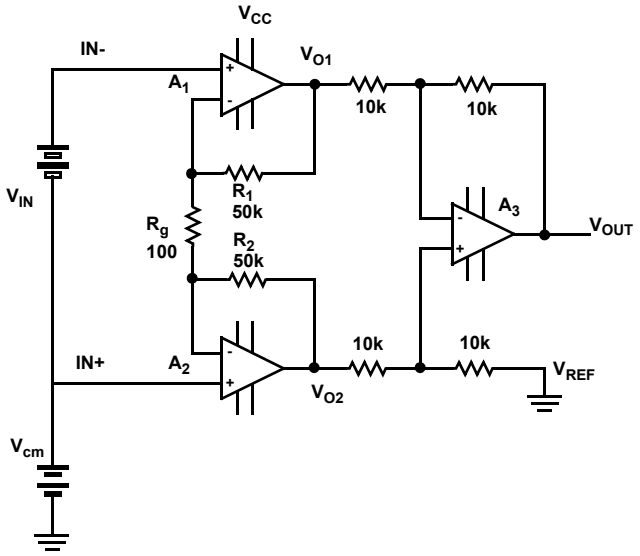

FIGURE 25.

Simple circuit analysis shows that the two internal voltage V_{O1} and V_{O2} are:

$$V_{O1} = V_{IN} \times (1 + R_1/R_g) + V_{cm} \quad \text{(EQ. 39)}$$

$$V_{O2} = V_{cm} - V_{IN} \times R_1/R_g \quad \text{(EQ. 40)}$$

Two clipping conditions will occur if the effects of V_{IN} and V_{cm} are not considered:

1. V_{O1} cannot exceed the maximum output voltage for A_1 which is the supply voltage (V_{CC}) and the saturation voltage of A_1's output stage.

$$V_{IN} \times (1 + R_1/R_g) + V_{cm} < V_{CC} + V_{sat} \quad \text{(EQ. 41)}$$

2. V_{O2} cannot go below Ground + the saturation voltage of A_2's output stage.

$$V_{cm} > V_{IN} \times R_1/R_g + V_{sat} \quad \text{(EQ. 42)}$$

In reality, this places a such a severe restriction on single supply operation that it makes this circuit almost impossible to use as a general purpose single supply instrumentation amplifier. For example, A_2 output stage saturation voltage prevents even 0V of common mode voltage!

To overcome this issue, modern monolithic IC instrumentation amplifiers add PNP level shift transistors (Q_1 and Q_2) to raise the input voltages off Ground as shown in the circuit in Figure 26.

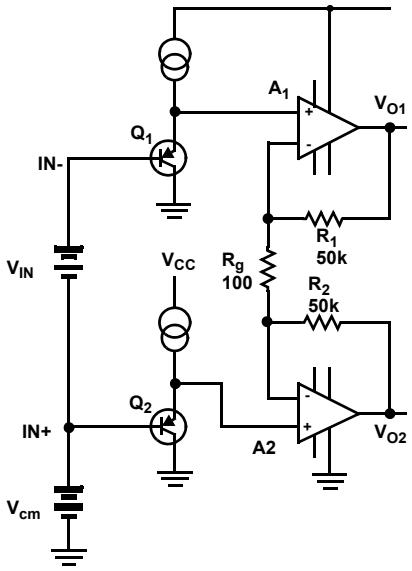

FIGURE 26.

The two internal voltage V_{O1} and V_{O2} are now:

$$V_{O1} = V_{IN} \times (1 + R_1/R_g) + V_{cm} + 0.7V \quad \text{(EQ. 43)}$$

$$V_{O2} = V_{cm} - V_{IN} \times R_1/(R_g + 0.7V) \quad \text{(EQ. 44)}$$

Now, the danger of internal clipping situation has been improved for A_2 but made worse for A_1 since an additional 0.7V has been added to V_{O1}. For example, the maximum common mode voltage is only 1.5V for this instrumentation amplifier operating on a supply voltage of 5V ±5% with a gain of 250 and a 10mV input signal! If you doubt the validity of these statements, check vendor data sheets for analog devices that exhibit these characteristics.

Since the Instrumentation Amplifiers operate in a current summing mode as explained in the “Instrumentation Amplifier Product Family Theory of Operation” on page 6, there is no possibility of internal clipping. As long as the total of the common mode voltage plus the input signal is between 0V and the V_S+ supply voltage there will be no internal clipping. The output voltage will swing within its rail-to-rail output specification of 10mV to either rail for a 100kΩ load. There is no restriction on differential input voltage or common mode voltage provided the output voltage does not exceed its full scale range due to input voltage level, gain, CMRR, and V_{REF} level.

All input and feedback terminals of the Instrumentation Amplifiers have internal ESD protection diodes to both positive (V_S+) and negative supply (V_S-) rails, limiting the input voltage to within one diode drop beyond the supply rails. The EL8170, EL8172, ISL28270 and ISL28470 have additional back-to-back diodes across the input terminals and also across the feedback terminals. If overdriving the inputs is necessary, the external input current must never exceed 5mA. On the other hand, the EL8171, EL8172, ISL28271, ISL28272 and ISL28273 have no diode clamps to limit the differential voltage on the input terminals allowing higher differential input voltages at lower gain applications. It is recommended however, that the input terminals of these devices are not overdriven beyond 1V to avoid offset drift.

An external series resistor may be used as an external protection to limit excessive external voltage and current from damaging the inputs. A 20k resistor can be used to protect the inputs against 100V transients on the inputs. If the overvoltage condition is continuous, the 20k resistor must be rated at 1W for adequate power dissipation.

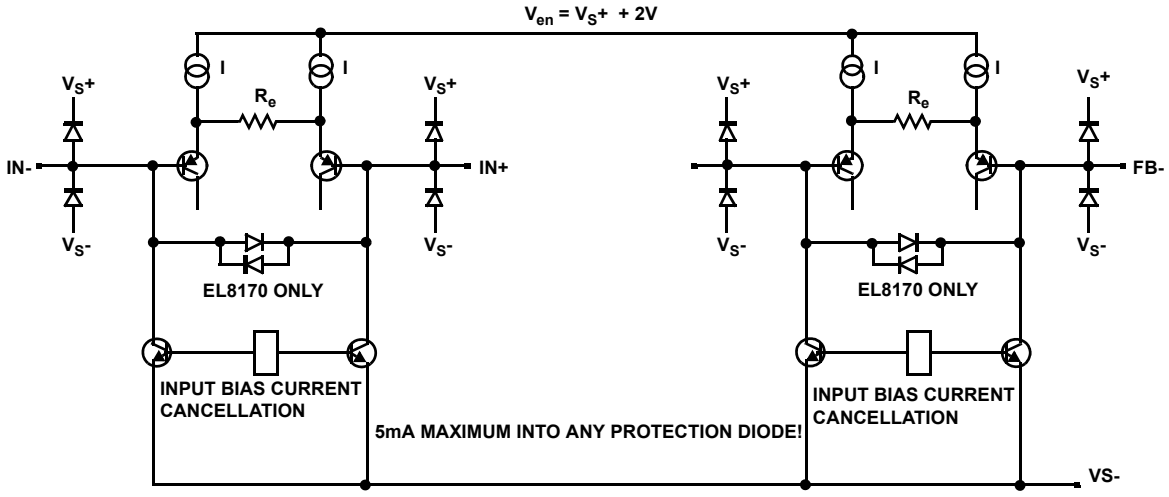

FIGURE 27. INPUT PROTECTION DIODES

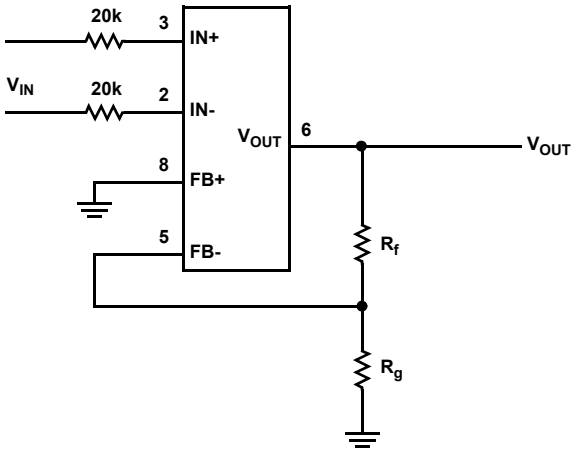

FIGURE 28.

Input bias current from the IN+ and IN- inputs of the Instrumentation Amplifiers must find a DC path to their home (i.e., Ground). While it seems obvious to the casual user, this is an often ignored principle when designing with an Instrumentation Amplifier, and results in many telephone calls to the Applications Engineer. Many voltage sources do not provide a DC path to Ground such as thermocouples, microphones, transformer coupled circuits, and AC coupled circuits. Without a DC return path, the input bias current will accumulate on any stray capacitance on the inputs until they are clamped to the rails by the protection diodes. The output of the Instrumentation Amplifier will slowly increase or decrease until it saturates into the V_S+ or V_S- rail.

A DC return path as shown in the following circuits must be supplied to provide a return path for the input bias current.

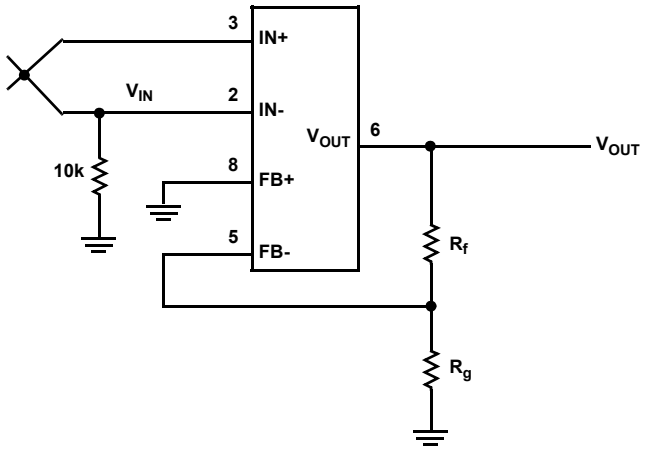

FIGURE 29.

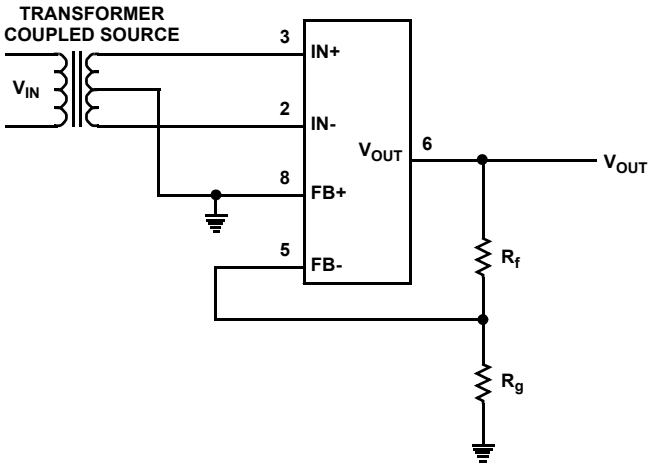

FIGURE 30.

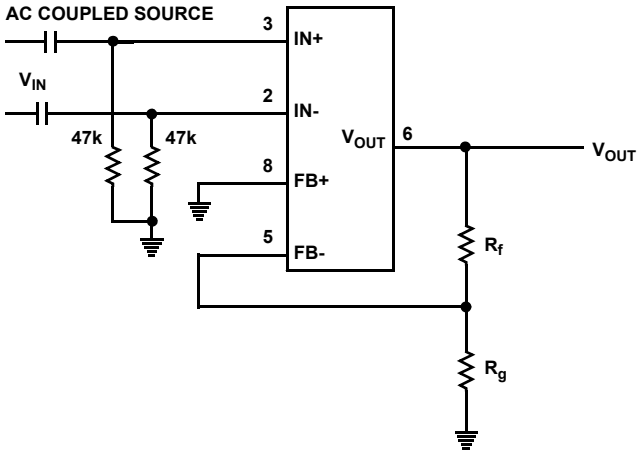

FIGURE 31.

An error budget can be calculated by summing the factors which contribute to the output voltage error. Most of the error sources are referred to the input and multiplied by the Gain to get an output voltage error term as shown in the following.

Offset voltage: Normally instrumentation amplifiers have two offset voltage specifications - an input offset voltage (V_{OSI}) and output offset voltage (V_{OSO}) specification such that the input offset voltage is multiplied by the gain, and the output offset voltage exhibits unity gain to the output voltage. Therefore, the output voltage error from offset voltage is:

$$V_{OUT} = Gain \times V_{OSI} + V_{OSO} \quad \text{(EQ. 45)}$$

Due to the unique architecture of the Instrumentation Amplifiers, there is only one offset voltage specification required. The input offset voltage (V_{OSI}) is the amount of voltage applied the inputs terminals such that the voltage across the FB is zero, or input offset voltage will be the difference between the IN terminals and the FB terminals:

$$(IN+ - IN+) = (FB+ - FB-) + V_{OS} \quad \text{(EQ. 46)}$$

$$V_{OUT}(V_{OSI}) = Gain \times V_{OSI} \quad \text{(EQ. 47)}$$

Offset bias current: Similar to an Op Amp circuit, the input resistance creates an error source that can be modeled the same as offset voltage such that:

$$V_{IB} = R_S \times I_{OS} \quad \text{(EQ. 48)}$$

$$V_{OUT}(I_{OS}) = Gain \times R_S \times I_{OS} \quad \text{(EQ. 49)}$$

Common Mode Rejection Ratio: The error introduced by common mode voltage can be modeled the same as an input offset voltage, V_{CMR}.

$$CMRR = 20 \times \log_{10}(V_{CMR}/V_{CMV}) \quad \text{(EQ. 50)}$$

$$V_{CMR} = V_{CMV} \times 10^{(CMRR/20)} \quad \text{(EQ. 51)}$$

$$V_{OUT}(CMRR) = Gain \times V_{CMR} \quad \text{(EQ. 52)}$$

0.1Hz to 10Hz Noise: The error introduced by voltage can be modeled the same as an input offset voltage, V_n. If noise is required in a wider bandwidth than 0.1Hz to 10Hz, the noise can be calculated by evaluating the Input Noise Voltage Density (e_n) over the desired bandwidth. Multiplying the rms noise by six will give a good approximation for the peak-to-peak noise.

$$V_{OUT}(V_n) = Gain \times V_n \quad \text{(EQ. 53)}$$

Gain Error: Gain error results from two factors. The first is the basic gain deviation from the ideal gain equation, Gain = (1 + R_f/R_g); for the EL8173 this error (E.g.) is typically ±0.2%. Second is the tolerance (ER_f and ER_g) of the R_f and R_g resistors which set the Gain.

$$V_{OUT} = V_{IN} \times (1 + R_f/R_g) \times [1 - (ER_f + ER_g + Eg)] \quad \text{(EQ. 54)}$$

Temperature Drift: The effect of operating over the expected temperature range must be included in all these calculations based on the data sheet specifications.

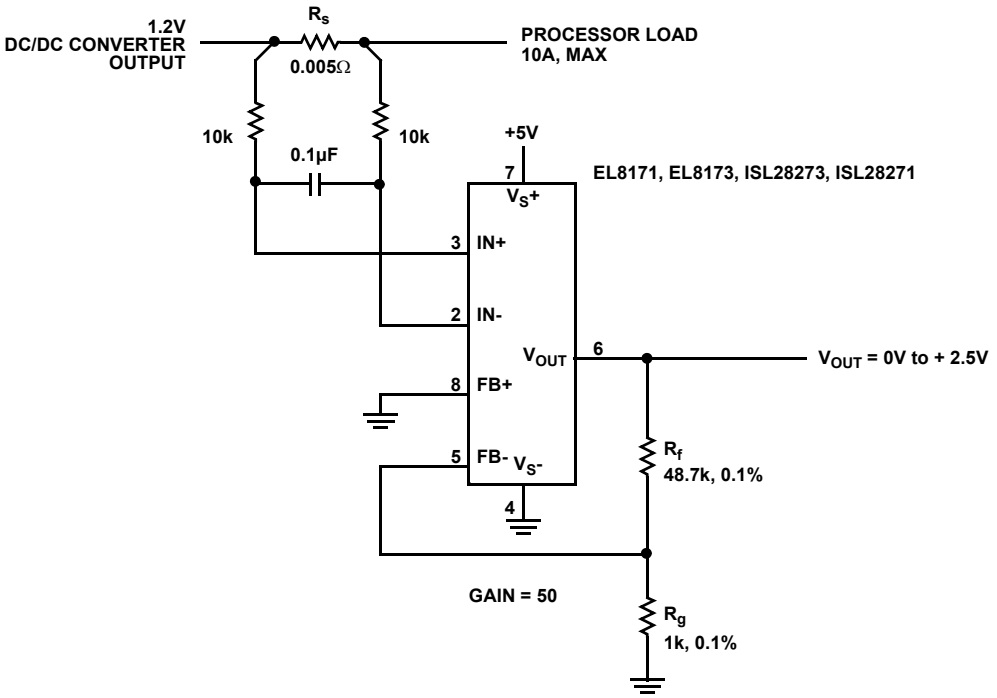

FIGURE 32.

TABLE 4. ERROR BUDGET CALCULATION

ERROR SOURCE	SPECIFIED VALUE	REFEREED TO OUTPUT	% FS ERROR
Offset voltage	400µV	20mV	0.8%
Input Offset Current	0.5nA	0.25mV	0.01%
CMRR	104dB	0.24mV	0.01%
0.1Hz to 10Hz Noise	10µV	0.5mV	0.02%
Gain Error	0.2%		0.2%
R_f, R_g Tolerance	0.1%		0.2%
		Total Error	1.24%

Example of an Error Budget Calculation

Consider the circuit shown in Figure 32 for a CPU core voltage current monitor circuit operating at +25°C.

The importance of an Error Budget as shown in Table 4 is that it is shows the overall accuracy which can be expected and which factors are determining the overall accuracy of the circuit. In this circuit, the Offset voltage is the factor which is driving the Total Error; if tighter accuracy is required for the application, the offset term could be removed by hardware calibration with a digital potentiometer or software calibration. The Total Error could be reduced to 0.5% just by decreasing the offset voltage term by a factor of 10.

Because of the independent pair of feedback terminals provided by Intersil's Instrumentation Amplifiers, the CMRR is not degraded by any resistor mismatches. Hence, unlike a three op amp and especially a two op amp instrumentation amplifier, the Intersil solution will reduce the cost of external components by allowing the use of 1% or more tolerance resistors without sacrificing CMRR performance. The CMRR will be greater than 100dB regardless of the tolerance of the resistors used.

The effects of loading the rail-to-rail output stage must also be considered too since the output stage exhibits an "ON" state resistance. A pair of complementary MOSFET devices with approximately 50Ω ON resistance drives the output V_{OUT} to within a few millivolts of the supply rails. At a 100kΩ load, the PMOS sources current and pulls the output up to 4mV below the positive supply, while the NMOS sinks current and pulls the output down to 4mV above the negative supply, or ground in the case of a single supply operation. As the load current is increased, the maximum output voltage will decrease as a result of the voltage drop caused by the sourced load current times the top MOSFET ON resistance. Likewise, the minimum output voltage will increase as a result of the voltage drop caused by the sink load current times FET ON resistance.

The current sinking and sourcing capability is internally limited to about 26mA with a 5V supply.

Care must be taken with excessive load capacitance, C_{LOAD}. As shown in the following graphs, excessive load capacitance will cause excessive peaking in the frequency response. The result will be ringing in the output voltage under transient conditions, and potentially oscillations resulting from unstable operation. If the Instrumentation Amplifiers are used in applications where there may be large load capacitance (cable driving, filters, FET gates, etc.), a suitable buffer should be used on the output of the Instrumentation Amplifier.

Noise calculations for the Instrumentation Amplifiers are very similar to those for an op amp circuit. The noise model is shown in the following where the Input Noise Voltage and Input Noise Current noise sources are lumped into the IN+ terminal.

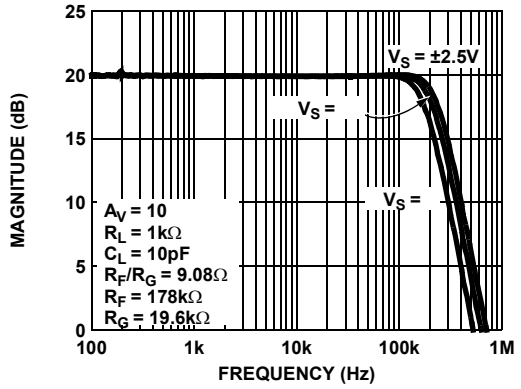

FIGURE 33. EL8171 FREQUENCY RESPONSE vs SUPPLY VOLTAGE

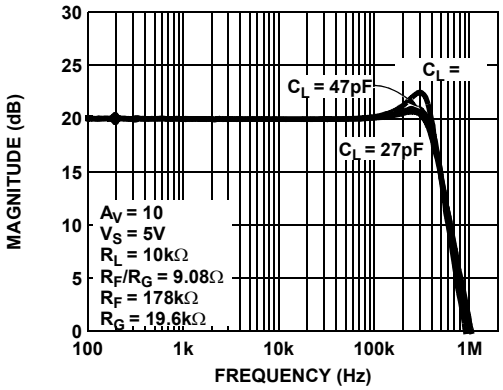

FIGURE 34. EL8171, EL8172 FREQUENCY RESPONSE vs C_{LOAD}

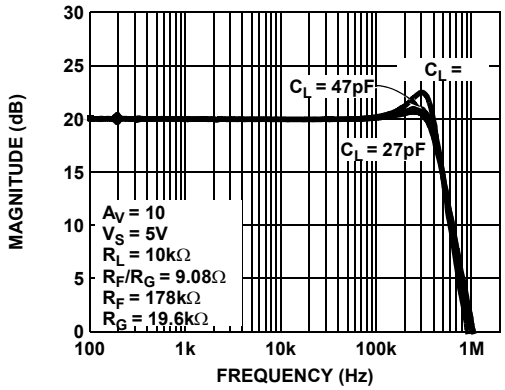

FIGURE 35. EL8171 FREQUENCY RESPONSE vs C_{LOAD}

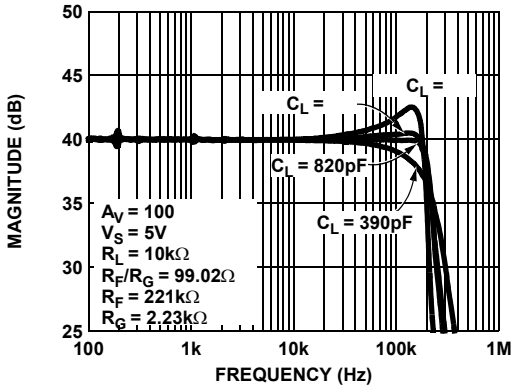

FIGURE 36. EL8172 FREQUENCY RESPONSE vs C_{LOAD}

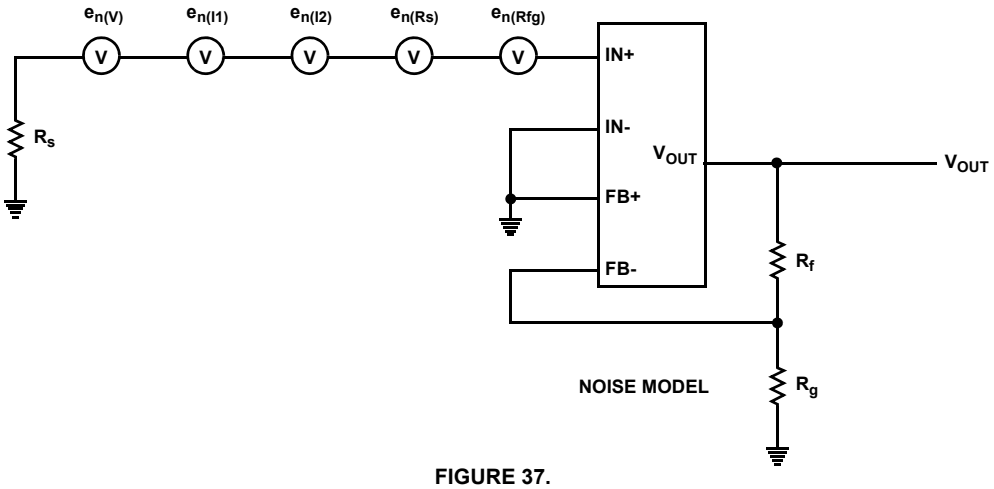

FIGURE 37.

Where: $e_{n(V)}$ is the Input Noise Voltage over the desired bandwidth $e_{n(I1)}$ is the voltage noise generated by the Input Noise Current over the desired bandwidth and the source resistance (R_s):

$$e_{n(I1)} = I_{IN} \times R_s \quad \text{(EQ. 55)}$$

$e_{n(I2)}$ is the voltage noise generated by the Input Noise Current over the desired bandwidth and the feedback and gain resistors ($R_f \parallel R_g$):

$$e_{n(I2)} = I_{IN} \times R_f \parallel R_g \quad \text{(EQ. 56)}$$

$e_{n(Rs)}$ is the thermal noise over the desired bandwidth of R_s.

$en_{(Rfg)}$ is the thermal noise over the desired bandwidth of $R_f \parallel R_g$

R_s is the source resistance

R_f and R_g are the gain setting resistors

To calculate rms noise, N over a desired bandwidth:

$$N = N_O\sqrt{(F_C \times \ln(F_h/F_l) + 1.57 \times F_h - F_l)} \quad \text{(EQ. 57)}$$

where: N_O is the specified noise density in nV/√Hz
F_c is the corner frequency
F_h is the upper frequency of interest
F_l is the lower frequency of interest

To calculate resistor thermal noise over a desired bandwidth:

$$N_r = \sqrt{4kTR \times (1.57 \times F_h - F_l)} \quad \text{(EQ. 58)}$$

where: R is the resistor value
k is Boltzman's Constant, $1.39*10^{-23}$
T is temperature in Kelvins
F_h is the upper frequency of interest
F_l is the lower frequency of interest

The 1.57 term in the equations is the noise equivalent bandwidth representing a 1st order roll-off equivalent as if there is a brick wall filter at $1.57*F_h$. If we have a brick wall filter that cuts off right (infinitely steep) at F_h then this term is 1.

1st order = 1.57
2nd order = 1.11
3rd order = 1.05
4th order = 1.025

To determine the total rms output noise from all the sources, the rms summation is taken multiplied by the gain.

$$e_n = (1 + R_f/R_g) \times \sqrt{(e_{n(V)}^2 + e_{n(I1)}^2 + e_{n(I2)}^2 + e_{n(I2)}^2 + e_{n(Rs)}^2 + e_{n(Rfg)}^2)} \quad \text{(EQ. 59)}$$

The peak-to-peak output noise is typically 6 times the rms value (rule of thumb).

$$e_{n(P-P)} = 6 \times e_n \quad \text{(EQ. 60)}$$

$e_{no(pp)} = 6 * e_{no}$

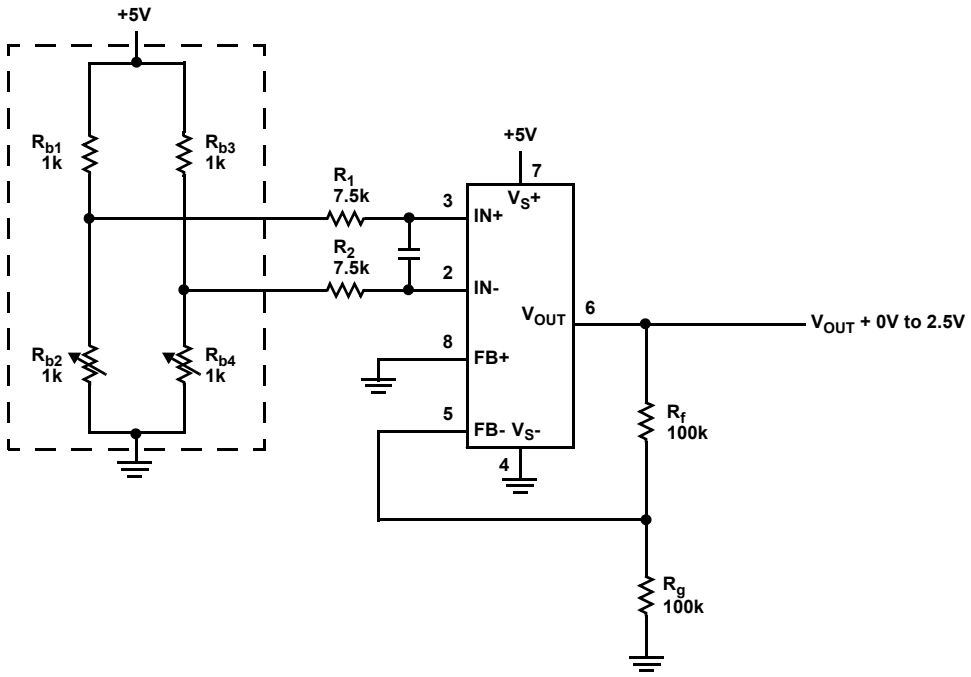

FIGURE 38.

Example of Noise Calculation:

Consider the circuit shown in Figure 38 for a bridge amplifier operating in a 0.5Hz to 100Hz bandwidth with a full scale output voltage of 2.V.

e_N = 50nv/√Hz	From the EL8170 data sheet specifications
F_c = 100Hz	From the EL8170 data sheet performance curves
i_N = 0.1pA/Hz	From the EL8170 data sheet specifications
Fc = 50Hz	From the EL8170 data sheet performance curves
R_s = 8kΩ	Balanced bridge Thevenin resistance + 7.5kΩ resistor
Rfg = 990Ω	Rf || Rg = 90.9k || 1k

$$e_{n(V)} = 50nV/\sqrt{Hz} \times \sqrt{100Hz \times L_n(100Hz/0.5Hz) + 1.57 \times 100Hz - 0.5Hz}$$
$$= 0.81\mu V, rms \quad \text{(EQ. 61)}$$

$$e_{n(I1)} = 0.1pA/\sqrt{Hz} \times \sqrt{50Hz \times L_n(50Hz/0.5Hz) + 1.57 \times 100Hz - 0.5Hz \times 8k}$$
$$= 0.12\mu V, rms \quad \text{(EQ. 62)}$$

$$e_{n(I2)} = 0.1pAnV/\sqrt{Hz} \times \sqrt{50Hz \times L_n(50Hz/0.5Hz) + 1.57 \times 100Hz - 0.5Hz \times 990}$$
$$= 0.0014\mu V, rms \quad \text{(EQ. 63)}$$

$$e_{n(Rs)} = \sqrt{(4 \times k \times 300°K \times 8k \times (100Hz - 0.5Hz))}$$
$$= 0.12\mu V, rms \quad \text{(EQ. 64)}$$

$$e_{n(Rfg)} = \sqrt{(4 \times k \times 300°K \times 990 \times (100Hz - 0.5Hz))}$$
$$= 0.04\mu V, rms \quad \text{(EQ. 65)}$$

$$e_n = (1 + R_f/R_g) \times (e^2_{n(V)} + e^2_{n(I1)} + e^2_{n(I2)} + e^2_{n(Rs)} + e^2_{n(Rfg)})$$

$$= (1 + 90.9k/1k) \times \sqrt{(0.81\mu V^2 + 0.012\mu V^2 + 0.0014\mu V^2 + 0.12\mu V^2 + 0.04\mu V^2)}$$

$$= 100 \times 0.82\mu V$$

$$= 82\mu Vrms \quad \text{(EQ. 66)}$$

To determine the total rms output noise from all the sources, the rms summation is taken multiplied by the gain.

Note that the total output noise is dominated by basic Input Noise Voltage and higher source resistance could be used without degrading the overall error resulting from noise.

$$e_{n(P-P)} = 6 \times 82\mu V = 492\mu V_{P-P} \quad \text{(EQ. 67)}$$

This represents an error of 0.02% for a 2.5V full scale output.

A very unique feature of the Intersil Instrumentation Amplifiers is the ability to put a filter circuit in the feedback network to shape the frequency response of the amplifier. This ability is not possible with other monolithic Instrumentation Amplifiers because they use a single resistor at the input stage to set the gain. Adding filter circuits in the feedback network of an Instrumentation Amplifier implemented with discrete components (op amps and resistors) is very difficult because capacitor mismatch will result in very poor high frequency CMRR.

A complex impedance network can be added as shown in the following for a low pass function. The low frequency gain is set by R_f and R_g using the standard equation:

$$Gain = 1 + R_f/R_g \quad \text{(EQ. 68)}$$

The Instrumentation Amplifiers are not unity gain stable; i.e., they require gains greater than 10 or 100 depending on the device. Therefore, they must never be allowed at unity gain even at high frequencies! If R_x was not included in this circuit, C_x would dominate at high frequencies, and the Instrumentation Amplifier would be unstable and oscillate. Lab tests have shown that C_x >33pF is enough to cause an oscillation. Adding R_x in series with C_x creates a zero in the transfer function so that at higher frequencies R_x parallels R_f so that the new R_f = 10.7k, and the gain at high frequency is 11.7 which is a stable condition. Lab tests have shown that any value can be used for C_x with no oscillations.

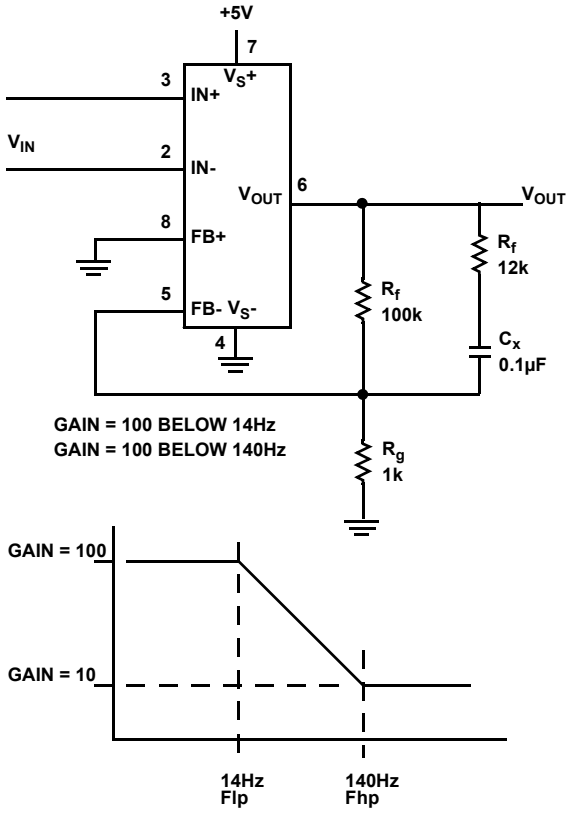

FIGURE 39.

For this circuit, it can be shown that low frequency pole and higher frequency zero are:

$$Flp = 1/(2 \times \pi \times C_x \times (R_f + R_x)) \quad \text{Pole Frequency}$$

$$= 1/(2 \times \pi \times 0.1\mu F \times (100k + 12k))$$

$$= 14Hz \quad \text{(EQ. 69)}$$

$$Flp = 1/(2 \times \pi \times C_x \times R_x) \quad \text{Zero Frequency}$$

$$= 1/(2 \times \pi \times 0.1\mu F \times 12k)$$

$$= 140Hz \quad \text{(EQ. 70)}$$

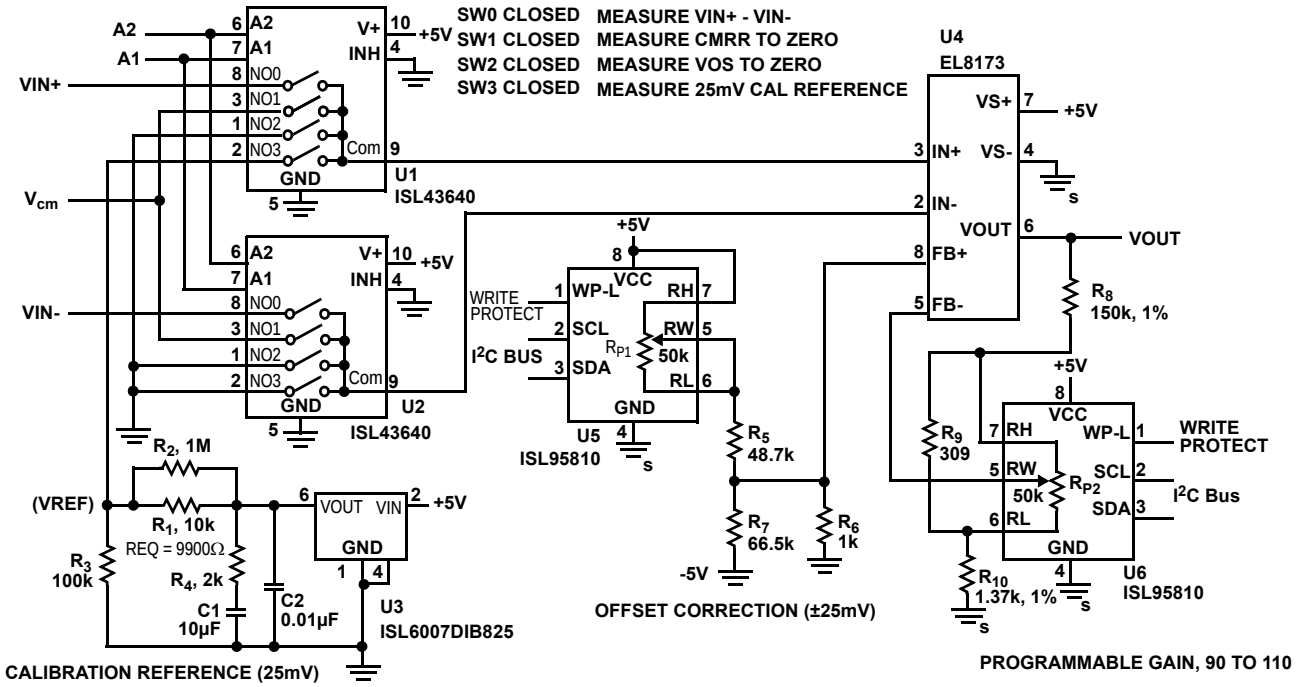

FIGURE 40. ANALOG FRONT-END CIRCUIT

Application Circuits

Instrumentation Amplifier With Auto Zero and Auto Gain Calibration

The circuit shown in Figure 40 shows an analog front-end circuit with an Auto Zero and Auto Gain Calibration to eliminate the offset voltage and gain errors of the EL8173. It is intended to be part of an overall data acquisition system with an A/D Converter and microprocessor to perform an auto zero/gain software routine. Figure 40 does not include the A/D Converter or processor hardware/software.

TABLE 5.

A2	A1	SWITCH CLOSED	MODE
0	0	SWO	Measure the input voltage VIN+ - VIN-
0	1	SW1	Calibrate with external common mode voltage applied
1	0	SW2	Calibrate offset voltage to zero
1	1	SW3	Calibrate gain with 25mV reference voltage applied

During the calibration mode, analog switches S1 and S2 connect the inputs of the EL8173 to calibration source voltages of zero volts, an external common mode voltage, or a 25mV reference voltage. Digital potentiometer (D-Pot) U5 applies a programmable offset voltage of ±25mV to the FB+ pin of the EL8173 to adjust the EL8173 output to zero voltages. Digital potentiometer (D-Pot) U6 programs the gain of the EL8173 from 90 to 110 for a 2.5V output with the +25mV reference voltage applied to the inputs.

Since the offset calibration voltage is operating at very close to zero voltages (±25mV), the driving point impedance is kept very low (1k, R_6) to avoid variations caused by the increasing bias current. The configuration of U5, R_5, and R_7 is carefully selected so that the D-Pot never is operated at a negative voltage.

The ±25mV offset calibration source is obtained by programming U5 with the appropriate digital code in Equation 71.

$$Vcal = \frac{5*\left(\frac{1}{R_1 + R_{pot}}\right) - \frac{1}{R_2}}{\left(\frac{1}{R_1 + R_{pot}}\right) + \frac{1}{R_2} + \frac{1}{R_3}} \quad \text{(EQ. 71)}$$

The +25mV reference voltage is obtained with the ISL6007's 2.5V output voltage divided down by a factor of 100 with R_1, R_2, and R_3. The accuracy of the gain calibration is determined by the accuracy of the ISL6007 and the tolerance of resistors R_1 and R_2. Therefore, it is recommended to use very low tolerance resistors for R_1 and R_2, or use a precision resistor divider network.

The gain of the EL8173 is programmed by D-Pot, U6 according to Equation 72:

$$Gain = \frac{R_8 + R_9 + R_{10}}{R_{10} + \frac{Code}{255} \times R_g}$$

$$Gain = \frac{150000 + 309 + 1370}{1370 + \frac{Code}{255} \times 309}$$

$$Gain = \frac{151.7k}{1370 + 1.2 \times Code} \quad \text{(EQ. 72)}$$

Other nominal gains and gain adjustment range can be made by changing the values of R_8, R_9, and R_{10}.

Pressure Sensor Interface Circuit

Programmable Pressure Transducer Circuit

The silicon piezoresistive-bridge pressure transducer (SPPT) is a dominant technology in automotive, industrial, medical, and environmental pressure sensor applications. All SPPTs share a similar architecture in which a thin (5µm to 200µm) micro machined silicon diaphragm incorporates an implanted piezoresistive Wheatstone-bridge strain-gauge. Applied pressure bends the diaphragm, imbalances the strain gauge, and thereby produces a differential output signal proportional to the product of pressure times bridge excitation voltage.

SPPTs must be supported by appropriate signal conditioning and calibration circuits. Finite elasticity limits the SPPT diaphragm to relatively small deflections which generate only ±1% modulation of the bridge resistance elements and low signal output levels, creating the need for high gain, low-noise, temperature-stable DC amplification. The signal conditioning circuit must also include stable, high resolution, preferably non-interactive, zero and span trims. The automation of the calibration of the sensor circuit is an enormous benefit in the production environment.

Another complication of SPPT application is the large temperature dependence of both total bridge resistance and peizosensitivity (the ratio of bridge output to excitation voltage times pressure). Bridge resistance increases with temperature while peizosensitivity decreases. Some SPPT designs (e.g. the Nova Sensor NPC-410 series) carefully equalize these opposite-sign tempcos. The payoff comes when such SPPTs are excited with constant current because the increase with temperature of bridge resistance (and therefore of bridge excitation voltage) then cancels the simultaneous decrease of peizosensitivity.

A 10mV/psi pressure-proportional strain gauge signal is outputted differentially on pins 2 and 4 of the sensor; this signal is superimposed on a common mode voltage of 1.2V from the bridge excitation voltage. The low level differential output voltage is amplified by the EL8173 with a nominal gain set at 50. The high common mode rejection capability of the EL8173 eliminates the common mode output voltage of the bridge. The bridge is biased from a constant current source (Q_2) and two digitally controlled potentiometers provide for zero (DPOT1) and full scale (gain) adjustments (DPOT2).

In the detailed circuit shown in Figure 41, the U_{2b} and U3 circuit provides for the precision offset adjustment, via DPOT1, of any transducer initial null offset error. To accomplish this, the bridge

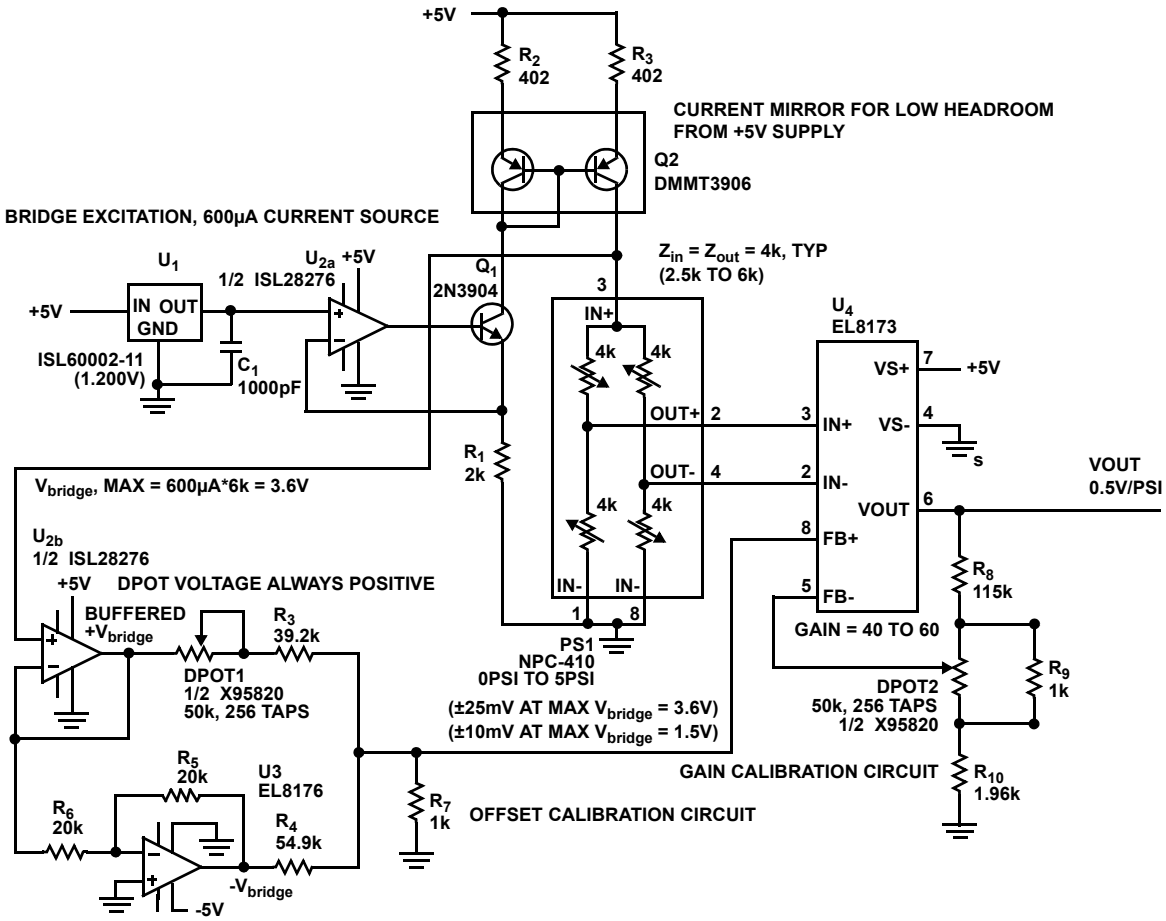

FIGURE 41.

excitation voltage is programmably attenuated by DPOT1 and applied to the FB+ pin of the EL8173. The range for the zero adjustment voltage is from +25mV to -25mV. The resolution is 200µV and is proportional to the bridge excitation voltage, thus improving the temperature stability of the zero adjustment.

The 10mV/psi bridge output signal is amplified by 50x to a convenient 0.5V/psi output level with the EL8173 its feedback and calibration network consisting of R_8, R_9, R_{10}, and DPOT2. The gain of U3 can be varied from 40 to 60 with a resolution of 0.10.

Bridge bias is provided by the constant current circuit (U_1, U_{2a}, and Q_1) which sets a current in Q_1 of 1.2 V/2k = 600µA. A current mirror (Q_2, R_2, R_3) reflects the output current so as to source the 600µA into the top of a grounded bridge (PS1).

The net result of the combination of transducer and the EL8173 circuitry is a signal conditioned precision pressure sensor that is compatible (thanks to DPOT1 and DPOT2) with full automation of the calibration process, is very low in total power draw (<2mA), most of which goes to transducer excitation and current mirror circuit.

Thermocouple Input with A/D Converter Output

Thermocouples are the industry standard temperature sensor for measuring a wide range of temperatures from -250°C to + 2300°C. The four most popular thermocouple types are shown in Table 6; however, any time two dissimilar metals are placed in contact, a thermocouple is created via the Seebeck Effect.

Thermocouples present several unique challenges when interfacing them to a real world measurement system.

1. Thermocouples generate a very low output voltage that must be amplified with a high gain amplifier. Each thermocouple type requires a different gain when interfacing to an A/D Converter with a fixed full scale voltage, V_{FS}/Vo_{MAX}.
2. Thermocouples do not generate an absolute voltage that is proportional to temperature. Instead, they generate a voltage that is a relative voltage that is the proportional to the temperature difference between the “hot” end and the “cold” end. All thermocouple tables showing output voltage vs temperature are for the “cold” end placed in an ice bath at 0°C. Since it is very impractical to place an ice bath on a PCB, electronic cold junction compensation is used. Each thermocouple type requires a cold junction compensation rate, dV_O/dT.
3. The output voltage of a thermocouple is non-linear, and is dependant on the type of thermocouple. Linearization is most often done with diode break-point techniques or via microprocessor software, and is not covered in this Application Note.

The circuit shown in Figure 42 uses the unique features of the Intersil EL8173 Instrumentation Amplifier to simplify the Thermocouple interface to a high resolution A/D Converter (U_5). A programmable gain digital pot (U_3) and programmable temperature sensor (U_2) allows digital selection of the four most popular thermocouple types: E, J, K, and T.

TABLE 6. POPULAR THERMOCOUPLE TYPES

TYPE	TEMPERATURE RANGE		V_O at T_{MIN}	V_O at T_{MAX}	dV_O/dT 0°C to +50°C
	MINIMUM	MAXIMUM	(mV)	(mV)	(µV/°C)
E	-200°C -328°F	+900°C +1652°F	-8.83	68.79	61.00
J	0°C +32°F	+750°C +1382°F	0.00	42.30	51.70
K	-200°C -328°F	+1250°C +2282°F	-5.89	50.64	40.50
T	-250°C -328°F	+350°C +662°F	-5.60	17.82	40.70

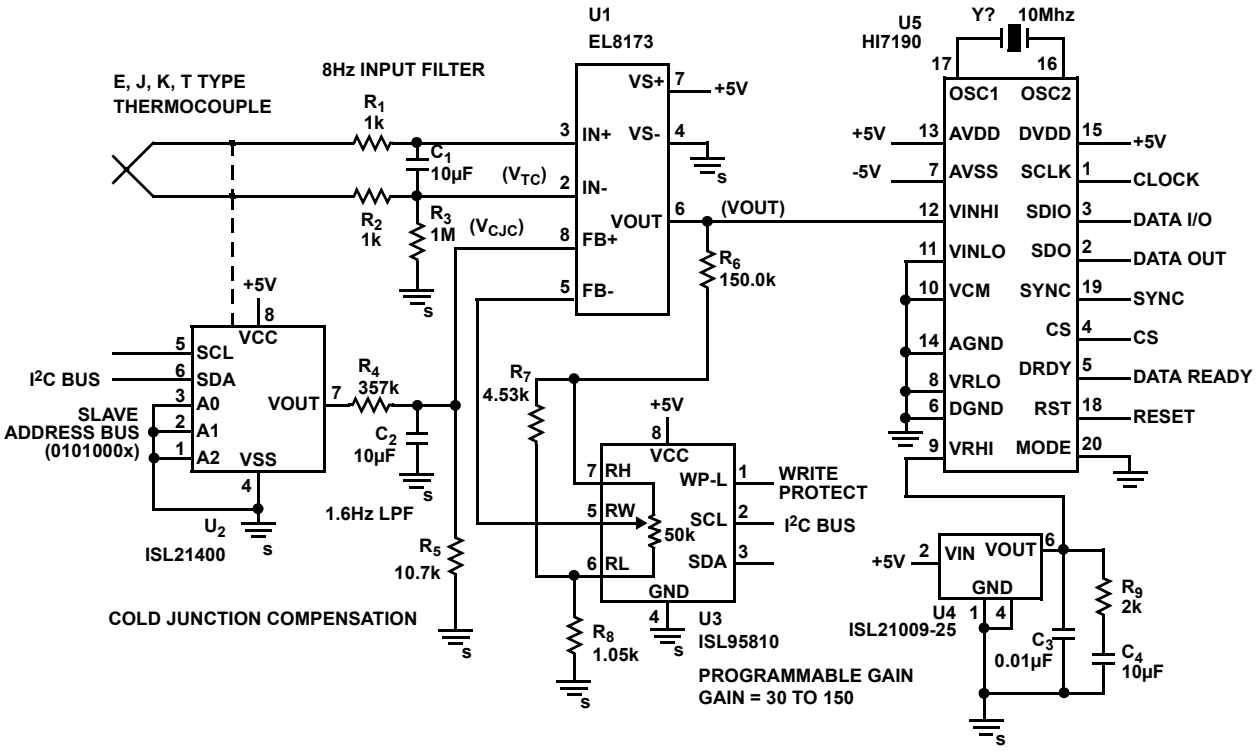

FIGURE 42.

The programmable gain amplifier (U_1, U_3) provide a gain from 30 to 150 that is programmed via the I^2C bus with the digital pot for each of the thermocouple types as shown in Table 7.

TABLE 7. THERMOCOUPLE TYPES

TC TYPE	MAX V_{OUT}	GAIN	D-POT $CODE_{10}$
E	68.97mV	36.34	195
J	42.30mV	59.10	094
K	50.64mV	49.37	126
T	17.82mV	140.3	000

Cold junction compensation is provided by a programmable reference/temperature sensor (U_2) and resistor divider network R_4 and R_5 according to the following table with A_V = 1 and N register = 0.

TABLE 8. COLD JUNCTION COMPENSATION

TC TYPE	V_CJ_C (µV)	M REGISTER
E	61.0	0
J	51.7	20
K	40.5	43
T	40.7	43

Low pass filters (R_1, R_2, C_1) provide noise filtering with a 8Hz cut-off frequency. R_3 is used for a return current path for the EL8173 input bias current. An additional low pass filter (R_4, R_5, C_2) attenuates the ISL21400's output noise voltage with a 1.6 Hz cut-off frequency.

A high resolution (24-bit) Sigma-Delta A/D Converter, HI7190, converts the output of the instrumentation amplifier, EL8173, with a full scale input voltage of 2.5V set by the ISL21009-2.5 voltage reference.

Thermocouple Input with 4mA to 20mA Output Current

Another output option for a thermocouple input circuit is an industry standard 4mA to 20mA current transmitter. The theory of operation for a 4mA to 20mA current transmitter circuit is described in Intersil Application Note AN177 with Figures 33, 34, and 35; this theory of operation applies to the thermocouple circuit shown in Figure 43, and therefore, will not be repeated.

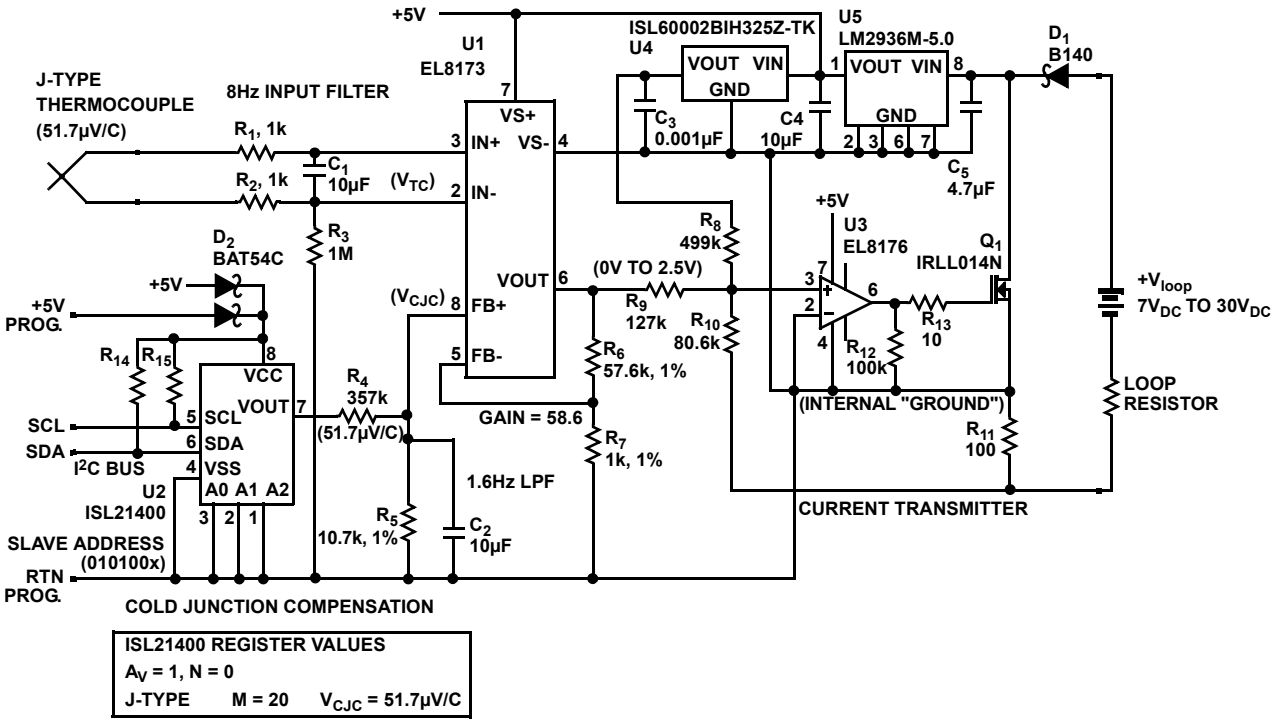

FIGURE 43.

The circuit uses the unique features of the Intersil EL8173 Instrumentation Amplifier to simplify the Thermocouple interface to a 4mA to 20mA Current Transmitter circuit. Since this is circuit is shown for a single J-type thermocouple, a fixed gain of 58.6 is used so that the output voltage of the EL8173 is +2.5V at the maximum thermocouple temperature. The ISL21400 programmable voltage reference/temperature sensor is used for cold junction compensation. Since the ISL21400 has non-volatile storage of the register values, it can be programmed either prior to PCB assembly or programmed via the I^2C bus as shown in this schematic. It must be cautioned that the I^2C programming "ground" is not at the same potential as the "Internal Ground" or loop supply ground; therefore, when programming U_2, the loop supply power supply or associated grounds must not be connected, or the I^2C programming system must be floating off ground.

Low pass filters (R_1, R_2, C_1) provide noise filtering with a 8Hz cut-off frequency. R_3 is used for a return current path for the EL8173 input bias current. An additional low pass filter (R_4, R_5, C_2) attenuates the ISL21400's output noise voltage with a 1.6Hz cut-off frequency.

Since the 4mA to 20mA loop voltage can be as high as 24VDC, a high voltage linear voltage regulator (U_5) is used to generate an internal +5V supply.

RTD Input with A/D Converter Output

Another popular industry standard temperature sensor is the RTD whose resistance varies with temperature, and is typically specified with a nominal resistance at +25°C. For example, a PT100 RTD has a resistance of 100Ω at 0°C. The shape of the resistance vs temperature curve is described by Equation 73, a second order equation, with a unique alpha value as defined by DIN EN 60751. For a PT100 RTD with alpha = 0.385%/ °C:

$$RTD = R_0(1 + A*T + B*T^2 + C*(T - 100)*T^3) \quad \text{(EQ. 73)}$$

Where: A = 3.9083 E-3, B = -5.775 E-7, C = -4.183 E-12 below 0°C and zero above 0°C.

RTDs are typically biased with 1mA to 5mA to minimize self-heating effects; this low operating current generates very low voltage levels shown in Table 9.

TABLE 9. TYPICALLY BIAS RTD's

TEMPERATURE (°C)	RTD (Ω)	V_{RTD} @ 1mA (mV)
-40	84.3	84.3
0	100.0	100.0
+100	138.5	138.5
+200	175.8	175.8

Since the RTD is often operated a great distance from receiving electronics, the use of differential voltage sensing is used to reduce the errors generated by high mode voltage induced noise.

The circuit in Figure 44 shows an RTD interface to a high resolution A/D Converter using an EL8173 Instrumentation Amplifier to differentially sense the RTD output and provide the proper gain for the input to the A/D Converter. Ratiometric mode operation of the A/D Converter eliminates the error introduced by variations in the RTD excitation current.

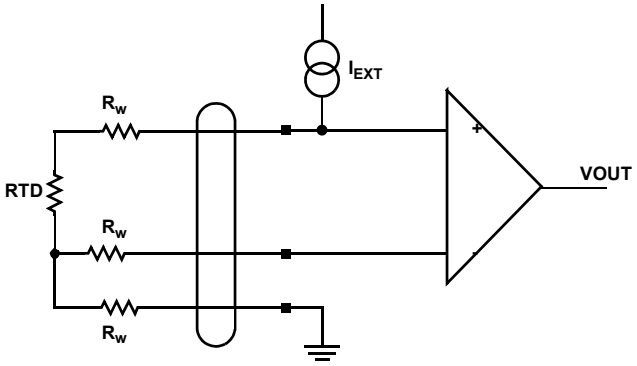

FIGURE 44.

In the circuit shown in Figure 44, RTD excitation current is supplied by R_1 and R_2 operating from +5V. It would appear that this current is not accurate enough for a high precision temperature measurement. And, that is true except for the trick that is played by utilizing the ratiometric mode of operation with the A/D Converter.

TABLE 10.

TEMP. (°C)	RTD (Ω)	I_{EXT} (mA)	V_{RTD} @ 1mA (mV)	CODE OUT_{10}
-40	84.3	1.22	84.3	7 778 756
0	100.0	1.22	100.0	9 227 469
+100	138.5	1.21	138.5	12 780 044
+200	175.8	1.20	175.8	16 240 345

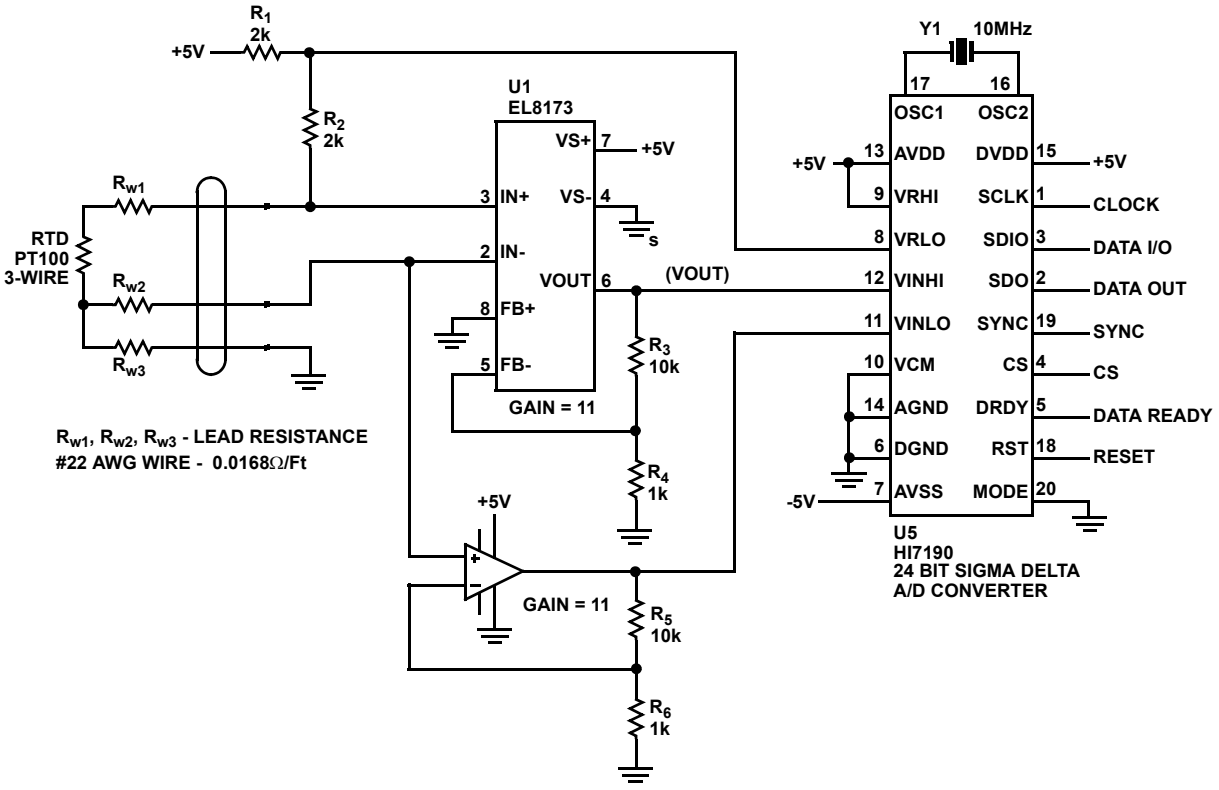

FIGURE 45.

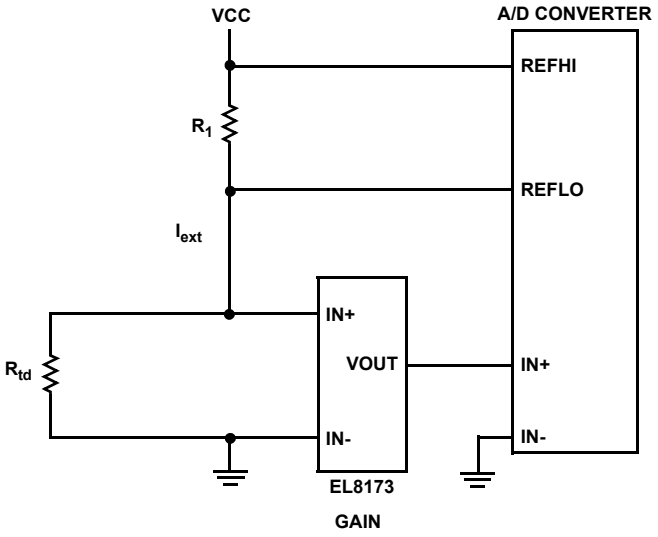

FIGURE 46.

In the simplified circuit shown in Figure 46, $I_{EXT} = V_{CC}/(R_1 + RTD)$ and $V_{RTD} = I_{EXT}*RTD$, $V_{OUT} = Gain*I_{EXT}*RTD$

For the A/D Converter, the digital output code,

$$CODE = \frac{2^N \times (IN+ - IN-)}{REF_{HI} - REF_{LOW}} \quad \text{(EQ. 74)}$$

Where N = Resolution

$REF_{Hi} - REF_{Lo} = I_{EXT}*R_1$

$Code = 2^N*(V_{OUT} - 0)/(I_{EXT}*R_1)$

$Code = 2^N*Gain*I_{EXT}*RTD/(I_{EXT}*R_1)$

$Code = 2^N*Gain*RTD/R_1$

Now, the output code is only dependant on the gain of the EL8173 and value of R_1, and the variations of I_{EXT} are cancelled out by the ratiometric operation of the A/D Converter.

Also, there is an error created by the wire resistance from the RTD leads from the RTD to the voltage sensing point. Therefore, RTDs are often connected with 3-wire and 4-wire lead configurations to reduce the effect of wire resistance. By far, the most common configuration is the 3-wire connection, and many general purpose 3-wire RTDs are available. Three different configurations for RTD wiring are summarized in the following.

However, even with a 3-wire configuration, there is still an error associated with the voltage drop caused by the wire resistance. The RTD circuit incorporates a technique which provides 4-wire accuracy with a 3-wire RTD, and the effect of wire resistance is eliminated completely.

The voltage drop created by the wire resistance, R_w, is multiplied by the same gain as the EL8173, and then the differential input of the A/D Converter (U_5) subtracts off the effect of the wire resistance, Rw.

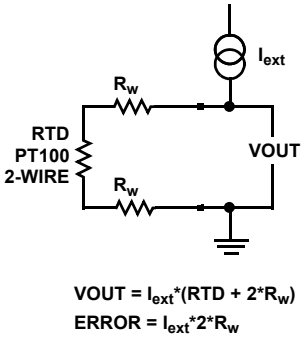

FIGURE 47A. 2-WIRE CONNECTION

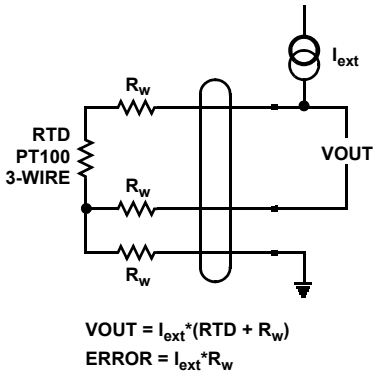

FIGURE 47B. 3-WIRE CONNECTION

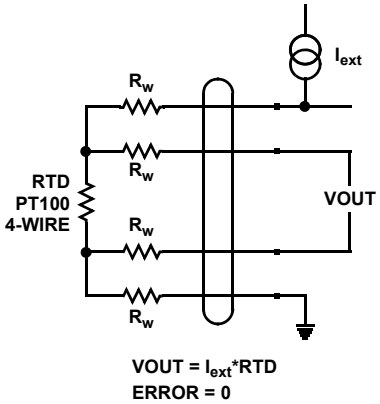

FIGURE 47C. 4-WIRE CONNECTION

FIGURE 47.

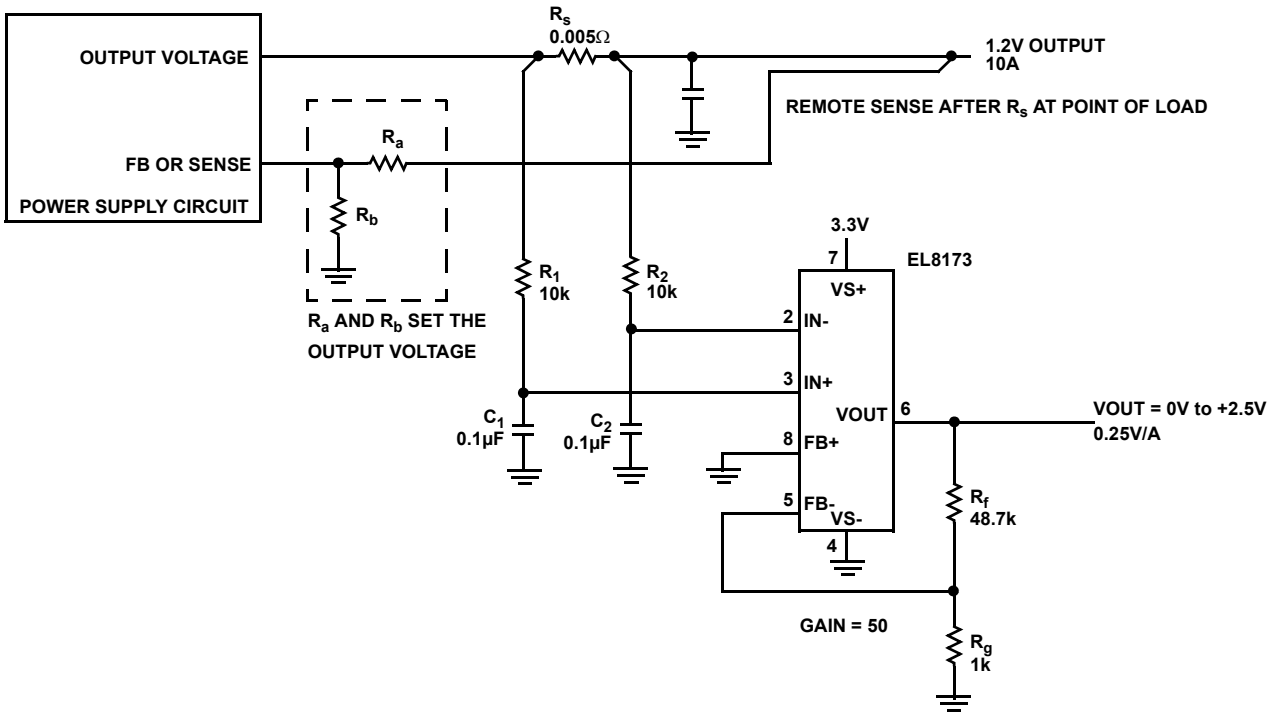

FIGURE 48.

Low Voltage High Side Current Sense

Due to the rail-to-rail input stage of the EL8173, high side current sensing is very easy to implement, as shown in Figure 48.

This circuit is appropriate for any power supply circuit with or without remote sense capability. The output current is measured by a current sense resistor, R_s that is scaled for the desired output voltage and resistor power rating. R_1, R_2, C_1, and C_2 are a simple low pass filter to attenuate the power supply output ripple and noise. Resistors R_f and R_g set the gain of the EL8173 for the desired full scale output voltage.

$$V_{OUT} = I_{OUT} \times R_S \times 1 + \frac{R_f}{R_g} \quad \text{(EQ. 75)}$$

In this circuit, Equation 76 shows a full scale voltage of 2.5V.

$$V_{OUT} = I_{OUT} \times 0.005 \times \left(\frac{1 + 48.7K}{1K}\right)$$
$$V_{OUT} = 0.25 \times I_{OUT} \quad \text{(EQ. 76)}$$

An accurate output voltage is obtained since remote sense is used by connecting R_a after the sense resistor, R_s. If remote sense is not possible, care should be exercised to minimize the voltage drop across R_s.

The previous circuit uses an external sense resistor to monitor the output current. If the DC/DC is a buck converter which uses an internal controller with current mode control, there is often a current sense resistor used to monitor the inductor current. If this is the case, the output current can be measured with that current sense resistor since the average value of the inductor current is equal to the load current in a buck regulator.

The circuit shown in Figure 49 is an example of using the current sense resistor, R_s, that is already a part of the current mode control loop to sense load current. There is a ripple voltage across R_s that is the inductor ripple current * R_s. The inductor ripple current is usually 30% to 50% of the load current and is set by the switching frequency and inductor value. This ripple voltage is essential for the current mode control loop, but must be filtered to obtain the output load current; this filter is performed by R_1, R_2, C_1, and C_2. Notice that even though the input voltage of the DC/DC converter is +12V, the common mode voltage that is applied to the EL8173 is the output voltage; in this case, 1.2V. As long as the output voltage is <5V, the input voltage can be much higher.

If the inductor current is sensed by using the switching FET's ON resistance as a current sense element, this method is not possible with the EL8173 circuit.

The output current can also be sensed by using the inductor's DCR (DC Resistance) as a current sense element as shown in the following circuit. This example in Figure 50 shows using the EL7566, but this method applies to any buck mode switching regulator.

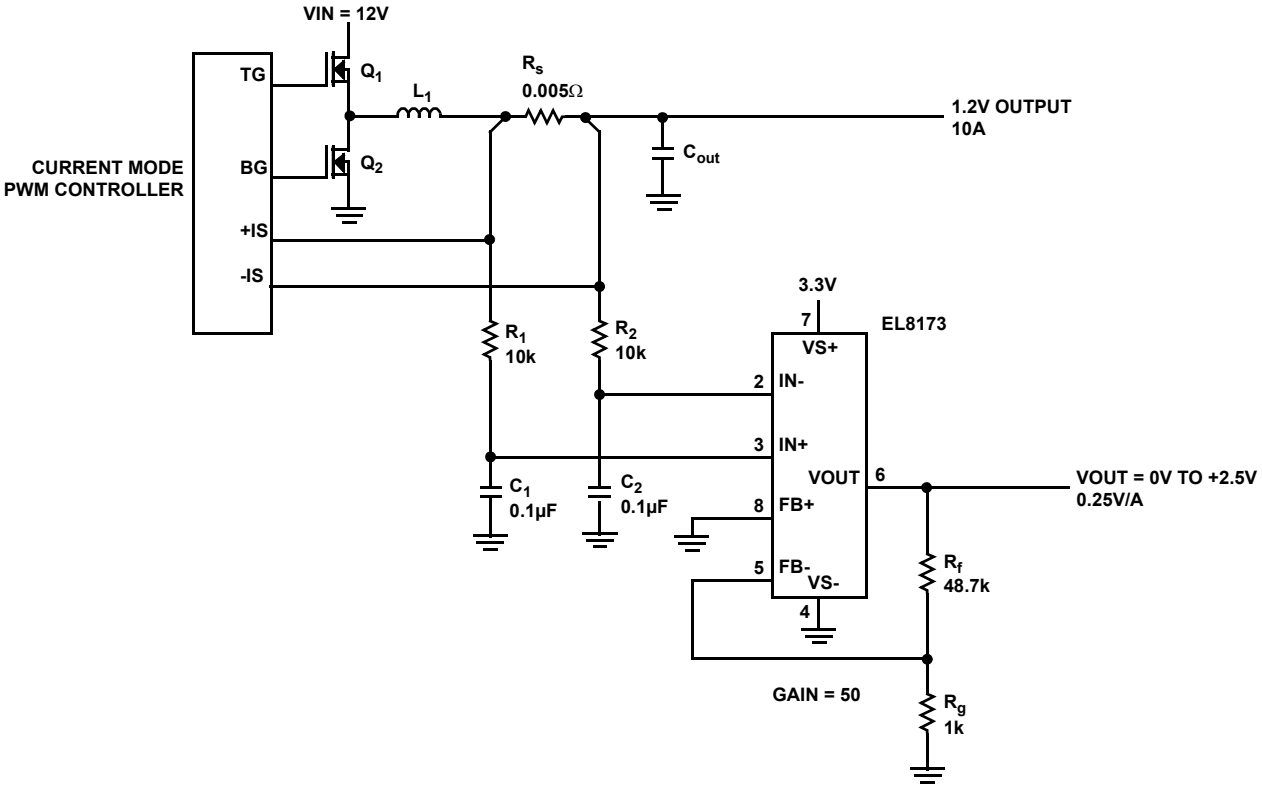

FIGURE 49.

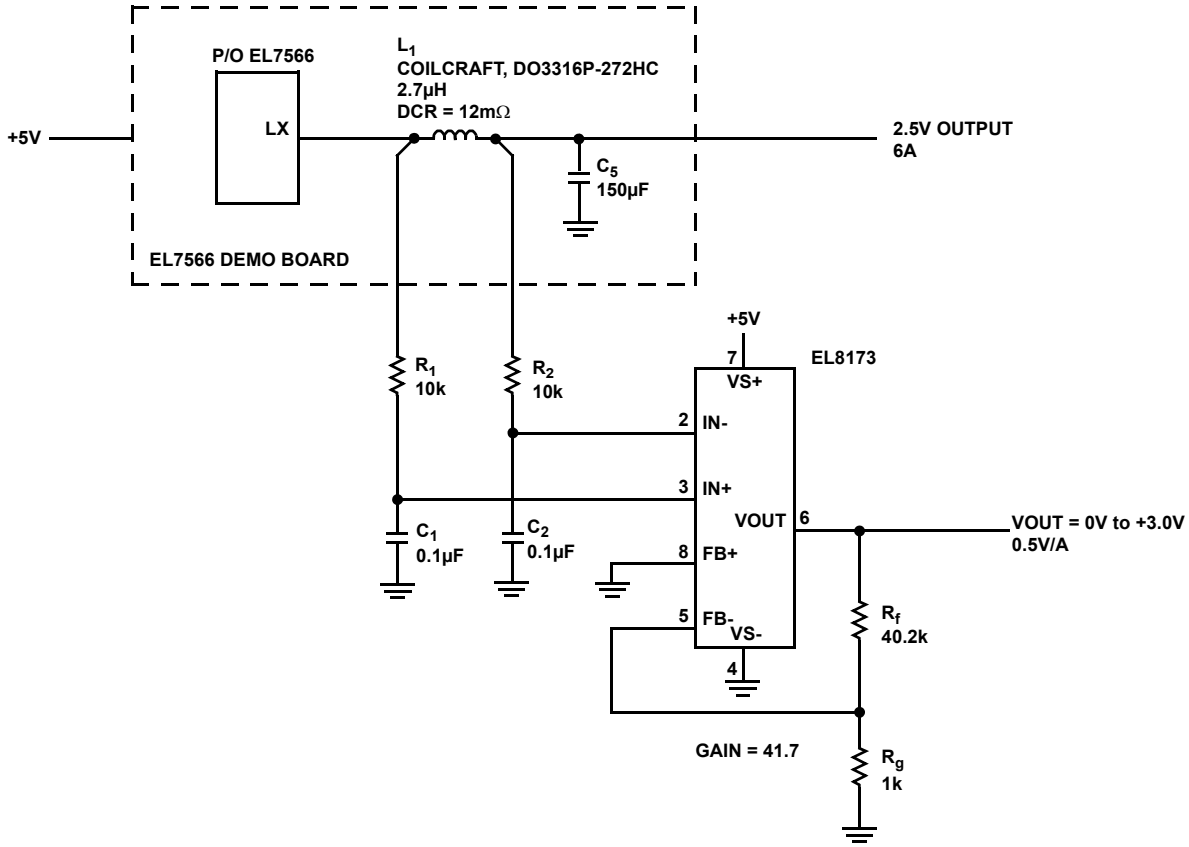

FIGURE 50.

In the circuit shown in Figure 50, the R_1 and C_1 filter is extremely important because it remove the voltage square wave (swinging between the input voltage and ground) that is applied to the inductor. The values for R_1 and C_1 should be selected to attenuate the signal to a level that is appropriate for the V_{OUT} noise that is acceptable.

Since the DCR of the inductor is being used as a current sense resistor, there are several factors which degrade the accuracy of this approach. First, most inductors are specified for only maximum DCR; for example, the Coilcraft DO3316P-27HC shown above is specified for a DCR of 12mΩ, maximum. Actual lab measurements should the DCR to be 9mΩ. Vishay offers a product line of inductors with a specified tolerance on the inductor DCR; for example, IHLP2525CZ-07 product family guarantees a DCR with ±5% tolerance.

Second, the inductor's internal winding's have a temperature coefficient of +0.393%/°C (copper wire) which can be a large error source if the inductor is allowed to get hot from ambient temperature or self-heating due to core losses and DCR power loss. If the error from this source is critical to the application, a thermistor could be mounted in close proximity to the inductor and be used to compensate the temperature coefficient of the copper windings.

High current (>30A) DC/DC converter outputs for microprocessor cores present very unique challenges for sensing the output current. Due to the high currents, the use of current sense resistors become very impractical due to their low values to minimize their power dissipation. For example, with a 50A output current, the current sense resistor must be <400µΩ to keep the power dissipation <1W. In addition, it is very difficult from a PCB layout viewpoint to break a high current power plane to insert a current sense resistor, and that forces the plane to neck-down to a very narrow current flow path.

High current DC/DC converter outputs now take advantage of advances in multi-phase DC/DC converters where a multiple lower current DC/DC conversion stages are connected in parallel to obtain the necessary high output current. Rule of thumb operates each phase at 15A to 20A so that for a 40A output current either 2- or 3-phases can be operated in parallel.

With multi-phase DC/DC converters the output current of each phase can be measured with a current sense resistor or DCR current sensing. The output from each current sense circuit is summed together to get the total load current. An additional feature of this scheme is that the current balance of each phase can be monitored. The circuit using a ISL28273 (dual EL8173) current sense circuit is shown in Figure 51 for a 30A, two phase circuit.

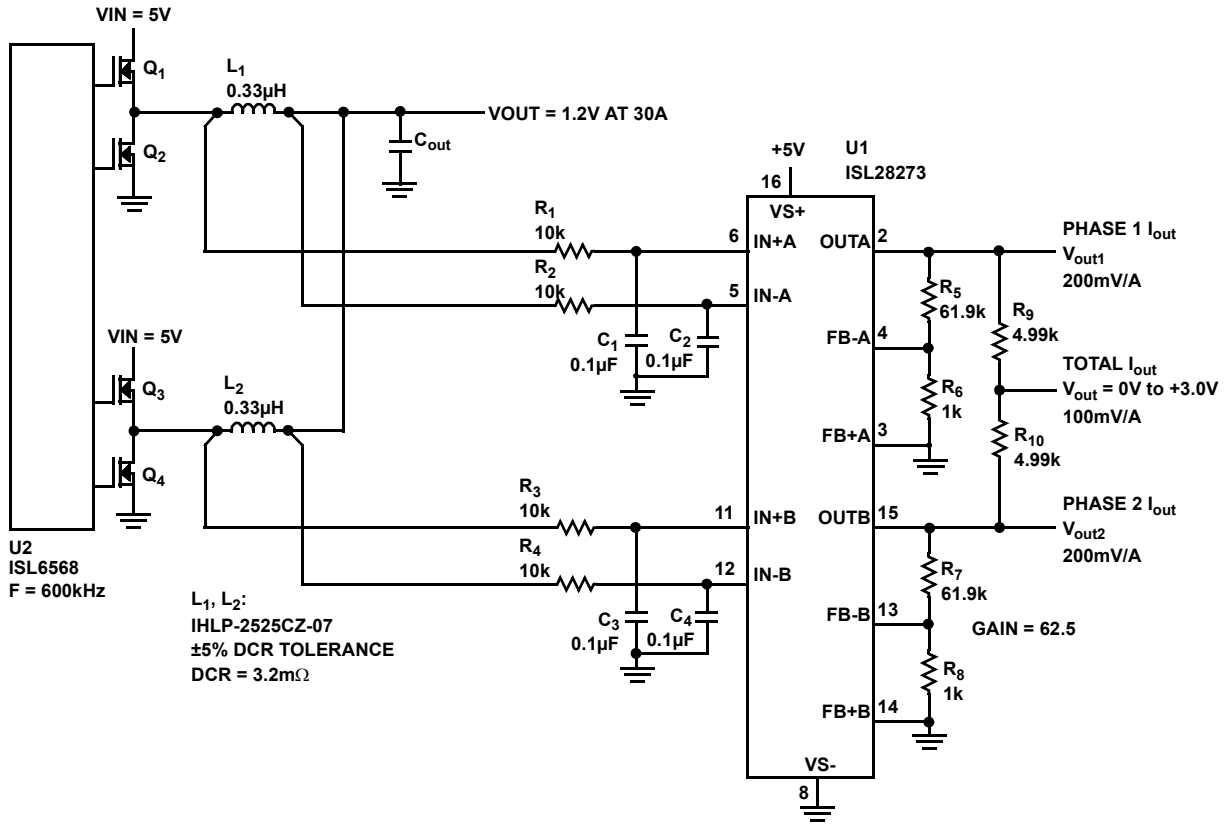

FIGURE 51.

The output current of each phase is measured by the DCR of L_1 and L_2 as explained in the previous example. V_{OUT1} and V_{OUT2} are proportional to the output current of each phase with a scale factor of 200mV/A. The two outputs, V_{OUT1} and V_{OUT2}, are summed together with R_9 and R_{10} to give a total output current, Total I_{OUT}, with a scale factor of 100mV/A.

This basic scheme can be extended to any number of phases for extremely high output currents exceeding 100A.

Multiplexed Low Voltage Current Sense

In a multiple voltage computer power supply, it is often necessary to monitor the output current from each DC/DC converter with an A/D Converter. When the EN pin of the ISL28271 and ISL28272 are enabled (i.e., device shutdown), the output stage goes into a high impedance state. This allows multiple VOUT pins to be connected together for multiplexed output applications. Since the output stage is in a high impedance state, only one set of feedback resistors (R_f, R_g) are required if all the amplifiers are operating with the same gain. Likewise, if different gains are required for each amplifier, separate feedback resistors can be used to set a unique gain on each amplifier.

Figure 52 demonstrates the multiplexing scheme for a power system with four output voltages; 1.2V at 20A, 1.8V at 10A, 3.3V at 4A, and 5.0V at 7.5A.

The dual instrumentation amplifier, ISL28271, is used to minimize parts count and circuit size. Each power supply load current is monitored with a low value current sense resistor (R_{S1}, R_{S2}, R_{S3}, and R_{S4}) to minimize voltage drop across the resistor. Input protection resistors (R_1 to R_8) limit the input fault current to <5mA in case of a short circuit on the OUT connection.

For this application, it is assumed V_{OUT} would be measured with a microprocessor A/D Converter with a full scale voltage of 2.5V. Each channel is scaled for an output voltage, V_{OUT}, equal to 2.0V at maximum load current to provide an overload measurement capability of 25%.

For each amplifier,

Sensed voltage, $V_s = I_{OUT}*R_s$

$V_{OUT} = Gain*V_s$

$V_{OUT} = Gain*R_s*I_{OUT}$

TABLE 11. SENSED VOLTAGE

EN	I_{OUT}(AMPS)	V_{OUT} SENSITIVITY (V/A)	VOUT AT MAX LOAD CURRENT (V)	GAIN
1	20	0.10	2.0	100
2	10	0.20	2.0	100
3	4.0	0.50	2.0	100
4	7.5	0.27	2.0	134

The gains of the two amplifiers of U_1 are both set to 100 by a single feedback resistor divider network, R_9 and R_{10}. The gains of U_2 are different in order to get the same V_{OUT} sensitivity using standard current sense resistor values. Gain A is set to 100 by R_{11} and R_{12}, and Gain B is set to 134 by R_{13} and R_{14}.

The EN lines (EN1, EN2, EN3, EN4) select the desired measurement channel.

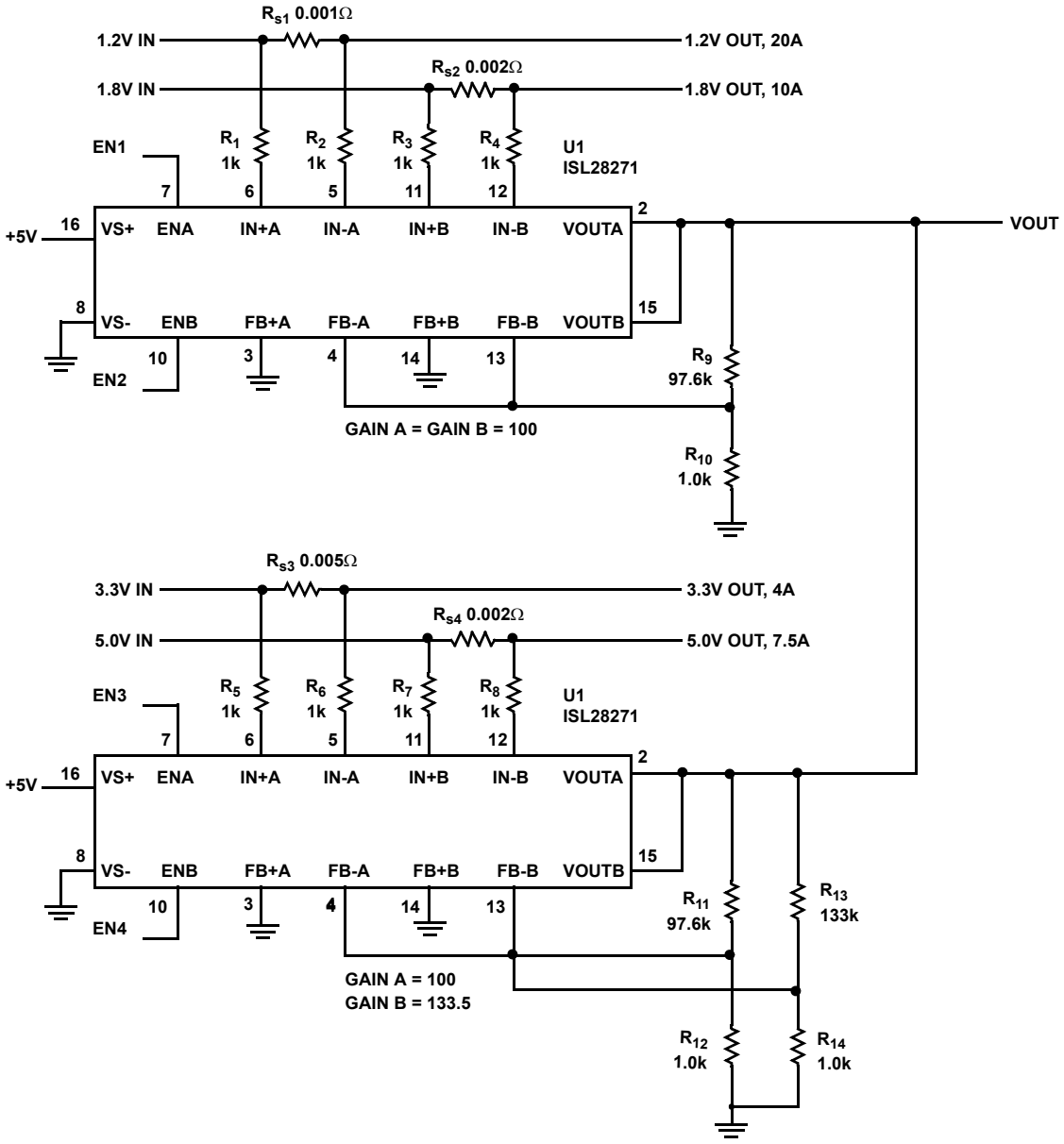

FIGURE 52. MEASUREMENT OF POSITIVE AND NEGATIVE CURRENT FLOW

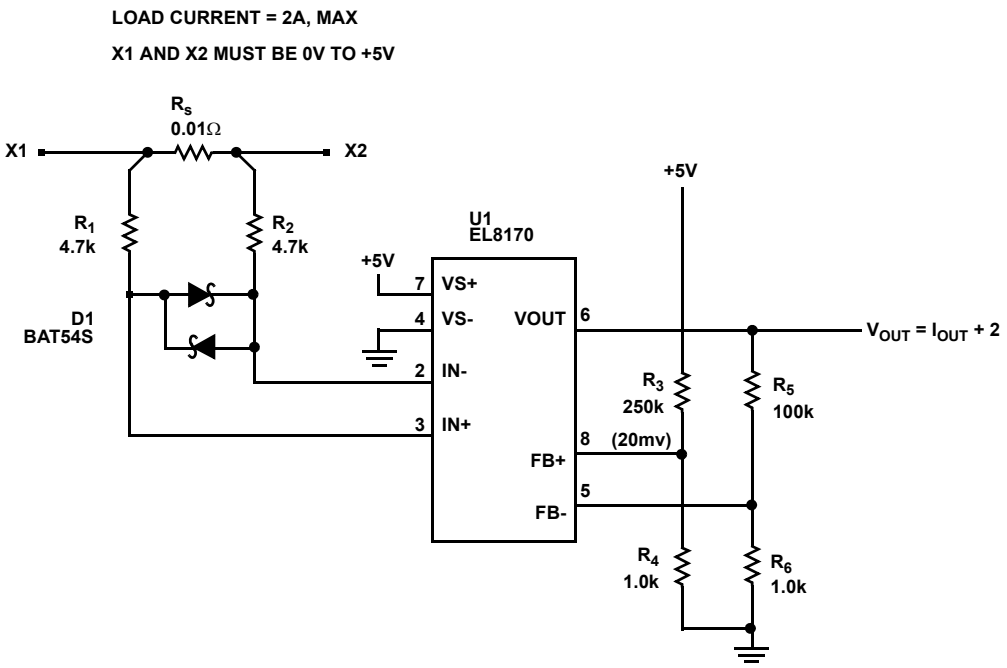

FIGURE 53. CURRENT MONITORED WITH LOW VALUE RESISTOR

Bi-Directional Current Sense

The use of the FB pins of the EL8170 make it an ideal choice for a bi-directional current sense circuit for battery gas gauging or current monitor in a H-bridge configuration as shown in the following circuits.

In Figure 53, current is monitored with the use of a low value resistor R_S. R_1, R_2, and D_1 protect the EL8170 from overvoltage which would be applied with excessive load current or a short circuit on the output, X1 or X2. The amplifier is set for a gain of 100 with R_5 and R_6. R_4 and R_5 offset the FB+ pin at 20mV to center 0A at mid-range of the output voltage V_{OUT}.

Sensed voltage is shown in Equation 77.

$$V_S = I_{LOAD} * R_S$$

$$V_{OUT} = Gain * (V_S + V_{FB+})$$

$$V_{OUT} = Gain * (I_{LOAD} \times R_S + V_{FB+})$$

$$V_{FB+} = \frac{+5 \times R_4}{R_4 + R_5}$$

$$V_{OUT} = 100 * (I_{LOAD} \times 0.01 + 0.02)$$

$$V_{OUT} = (I_{LOAD} + 2) \qquad \text{(EQ. 77)}$$

TABLE 12.

LOAD CURRENT (I_{LOAD})	V_{OUT}
-2A	0.0V
0A	+2.0V
+2A	+4.0V

The range of the measured current can easily be changed by proper selection of R_S, Gain and FB+ voltage.

The circuit in Figure 54 shows the EL8170 set-up as a battery gas gauge to monitor both charging current and discharging current.

In this circuit, when the battery is charging, the current in R_S will be negative (i.e., flowing from X2 to X1). The EL8170 output voltage will be between 0V and +2V. When the battery is being discharged, the current flow will be from X1 to X2, and the EL8170 output voltage will be between +2V and +4V.

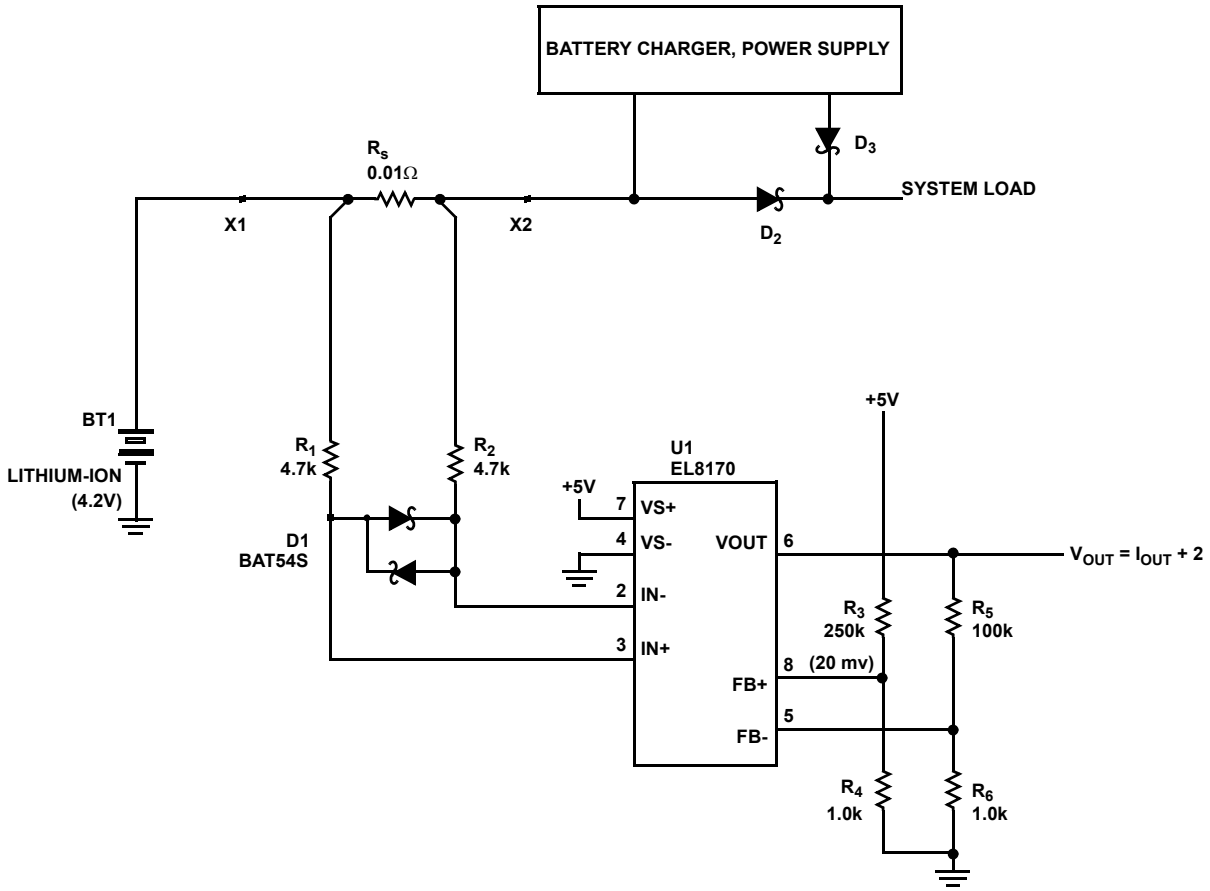

FIGURE 54. EL8170 SETUP AS A BATTERY CHARGER

If a more direct measurement for the current polarity and increased output voltage sensitivity is required, the circuit shown in Figure 55 can be used.

In Figure 55, U_1 is used to measure positive current flow (X1 to X2) and U_2 is used to measure negative current flow (X2 to X1). The polarity of the current is detected by U_3 which is being used a zero crossing detect comparator. The EN pins of the EL8170 (U_1, U_2) are used to turn on the proper amplifier depending if the current flow is positive or negative. In the above circuit, current is monitored with the use of a low value resistor R_s. R_1, R_2, and D_1 protect the EL8170's from over-voltage which would be applied with excessive load current or a short circuit on the output, X1 or X2. When this bi-directional current sense circuit is used in a PWM application such as a H-bridge, C_1 and C_2 can be added to filter the PWM signal for an average current value.

The amplifiers are set for a gain of 100 with R_5 and R_6. The minimum sensed current is set by the EL8170 offset voltage.

$$I_{MIN} = \frac{V_{OS}}{R_S}$$

$$I_{MIN} = \frac{0.25mV}{0.01\Omega}$$

$$I_{MIN} = 25mA \qquad \text{(EQ. 78)}$$

Figure 56 shows the bi-directional current source circuit configured to monitor the motor current in a H-bridge circuit. The direction of the motor (CW, CCW) is monitored by the polarity bit depending on the direction of current flow in the motor. The rail-to- rail input capability of the EL8170 allows current sensing at ground level (Q_1 and Q_4 ON) or at +5V (Q_3 and Q_2 ON). If pulse width modulation is used to control the speed of the motor, filter capacitors C_1 and C_2 should be used to obtain the average value of the motor current. The value of the capacitors should be selected based on the PWM frequency and desired overall accuracy.

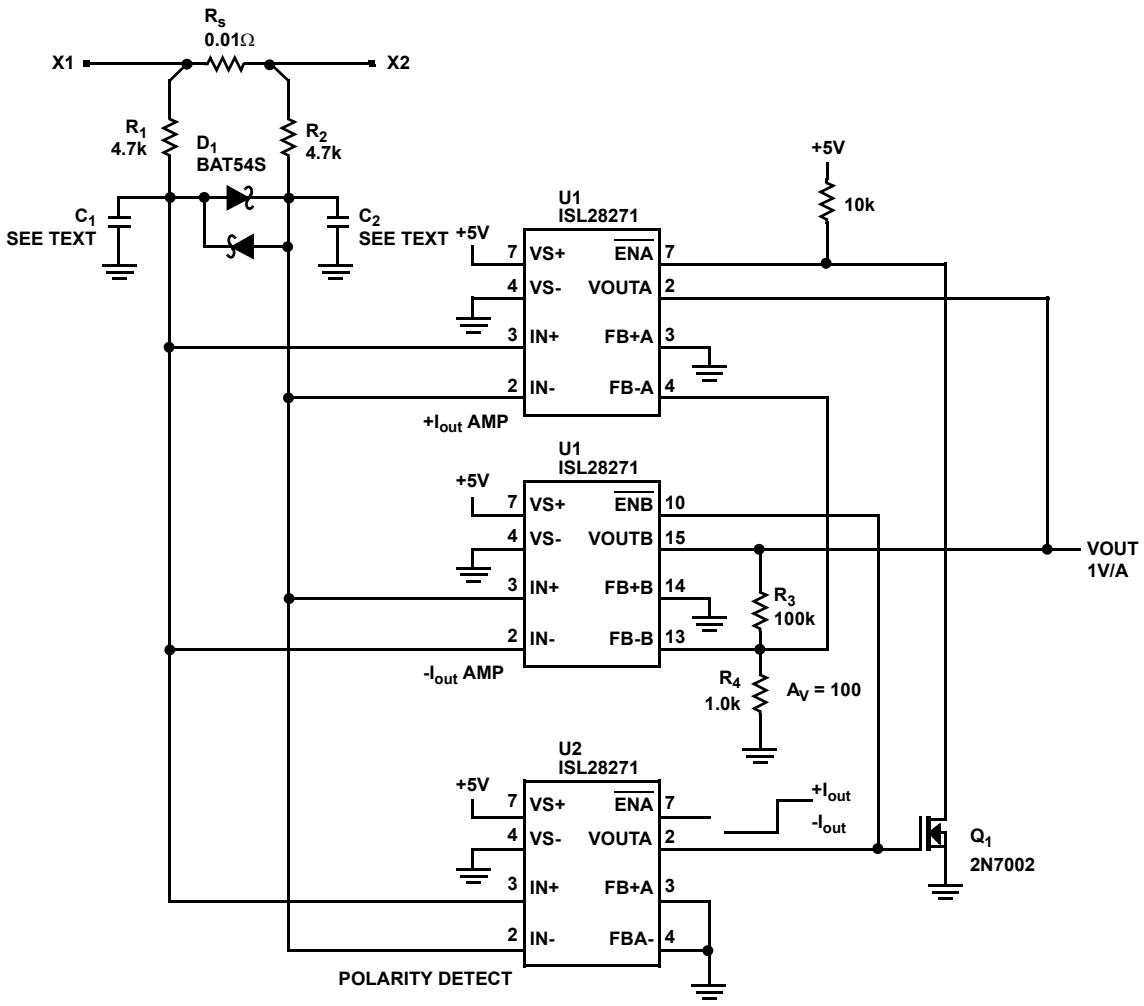

FIGURE 55. MEASUREMENT OF POSITIVE AND NEGATIVE CURRENT FLOW

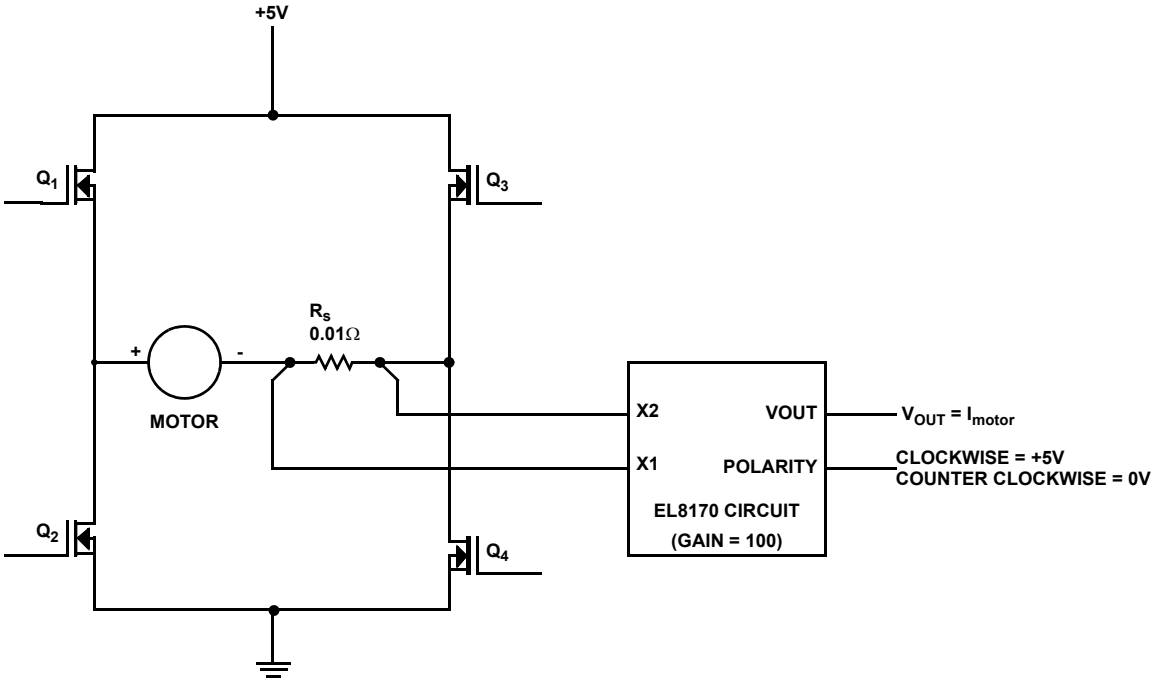

FIGURE 56. BI-DIRECTIONAL CURRENT SOURCE CIRCUIT

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