To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

NP60N04HLF,NP60N04ILF

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The NP60N04HLF and NP60N04ILF are N-channel MOS Field Effect Transistors designed for high current switching applications.

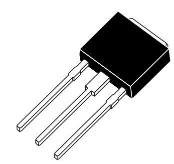
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP60N04HLF	TO-251 (MP-3)
NP60N04ILF	TO-252 (MP-3Z)

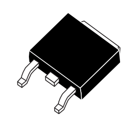
FEATURES

- Super low on-state resistance
  $R_{DS(on)1}$ = 6.5 mΩ MAX. (V_{GS} = 10 V, I_D = 30 A)
  $R_{DS(on)2}$ = 9.1 mΩ MAX. (V_{GS} = 4.5 V, I_D = 30 A)
- Low C_{iss}: C_{iss} = 2600 pF TYP. (V_{DS} = 25 V, V_{GS} = 0 V)
- Built-in gate protection diode

(TO-251)



(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C) Note1	$I_{D(DC)}$	±60	A
Drain Current (pulse) Note2	$I_{D(pulse)}$	±240	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	100	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	−55 to +175	°C
Repetitive Avalanche Current Note3	I_{AR}	32	A
Repetitive Avalanche Energy Note3	E_{AR}	100	mJ

Notes 1. Calculated contact current according to MAX. allowable channel temperature.

2. PW ≤ 10 μs, Duty Cycle ≤ 1%

3. V_{DD} = 20 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, $T_{ch(peak)}$ ≤ 150°C

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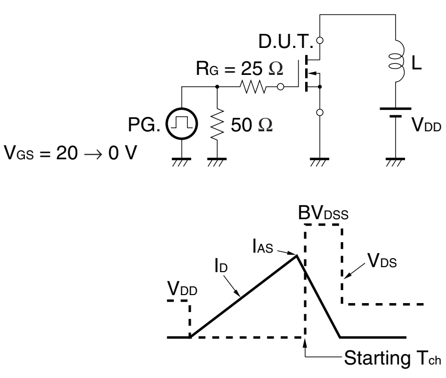
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

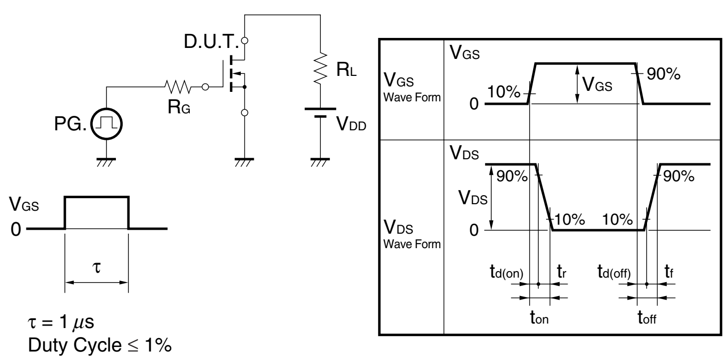
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 30 A	22	43		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 30 A		5.2	6.5	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 30 A		6.6	9.1	mΩ
Input Capacitance	C_{iss}	V_{DS} = 25 V		2600	3900	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		480	720	pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		180	330	pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20 V, I_D = 30 A		11	23	ns
Rise Time	t_r	V_{GS} = 10 V		13	32	ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		69	138	ns
Fall Time	t_f			14	34	ns
Total Gate Charge	Q_G	V_{DD} = 32 V		50	75	nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		9		nC
Gate to Drain Charge	Q_{GD}	I_D = 60 A		13		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 60 A, V_{GS} = 0 V		0.94	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, V_{GS} = 0 V		40		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		42		nC

Note Pulsed

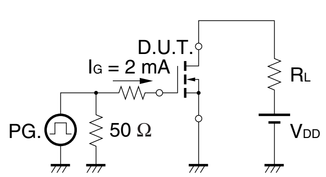
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

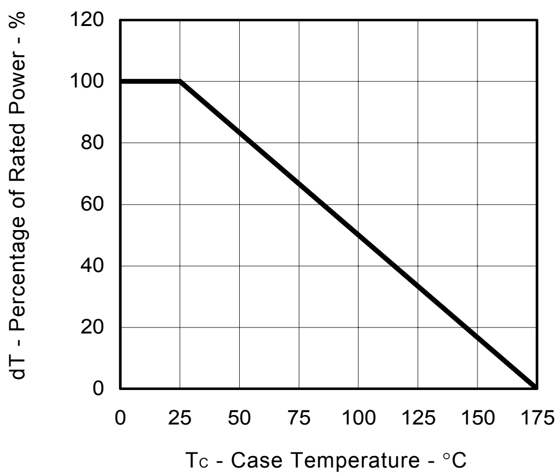


TEST CIRCUIT 3 GATE CHARGE

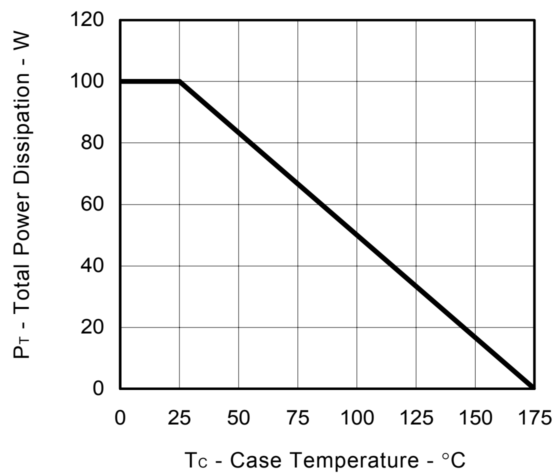


TYPICAL CHARACTERISTICS (TA = 25°C)

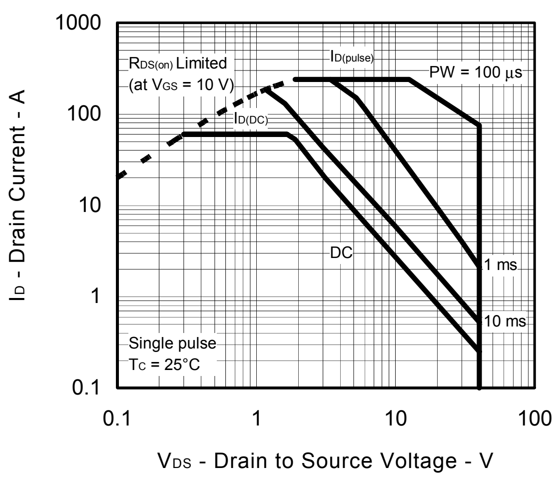
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



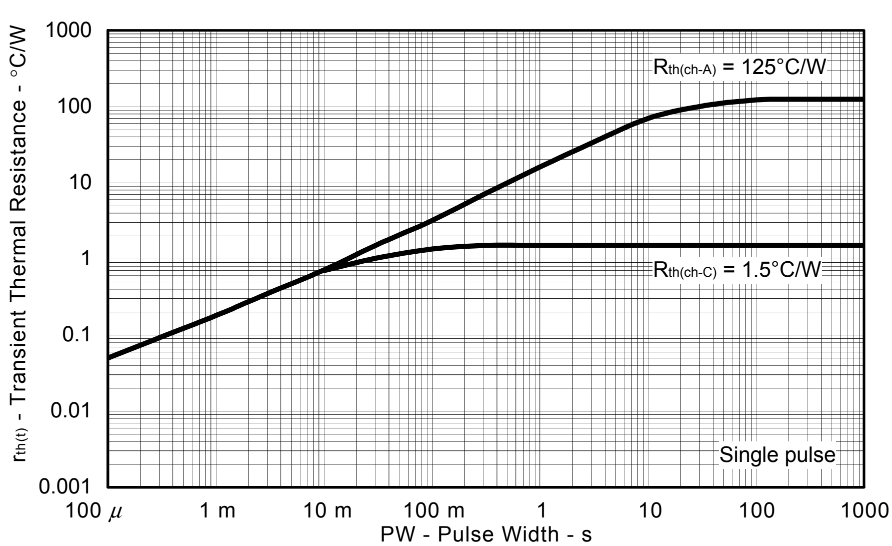
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



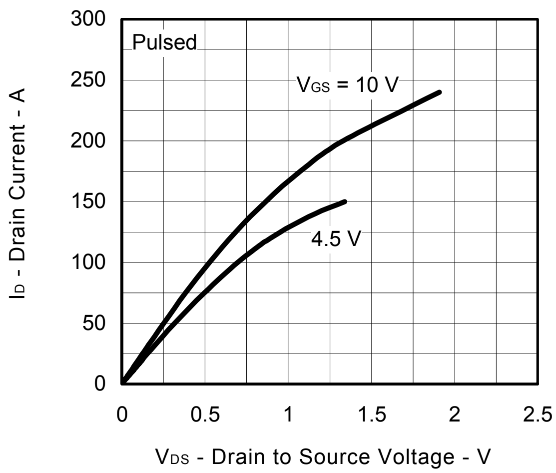
FORWARD BIAS SAFE OPERATING AREA



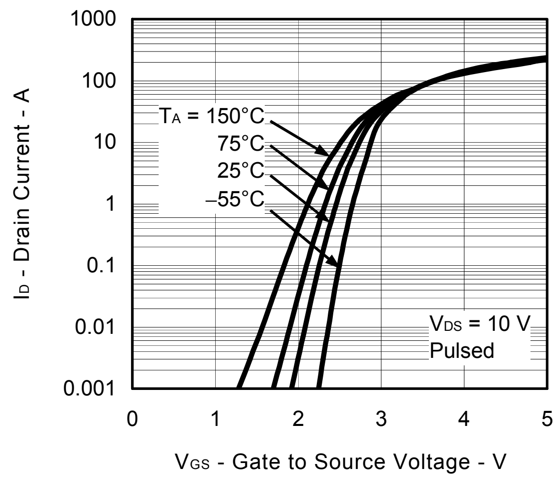
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



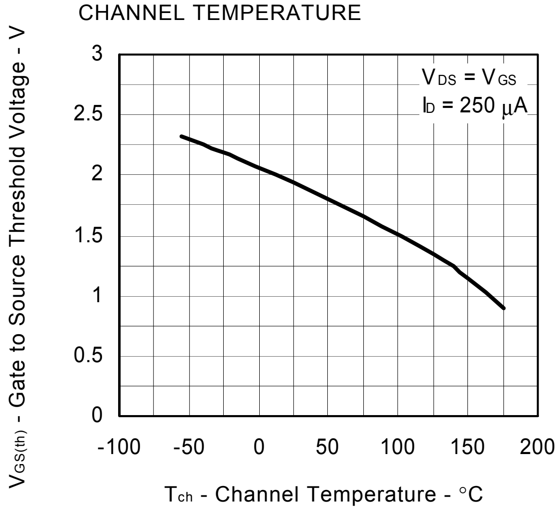
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



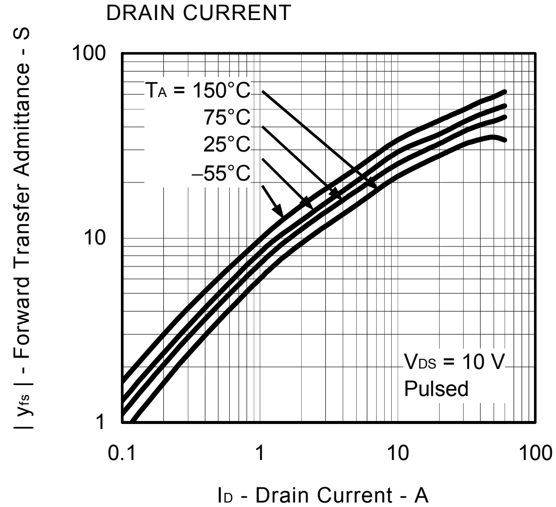
FORWARD TRANSFER CHARACTERISTICS



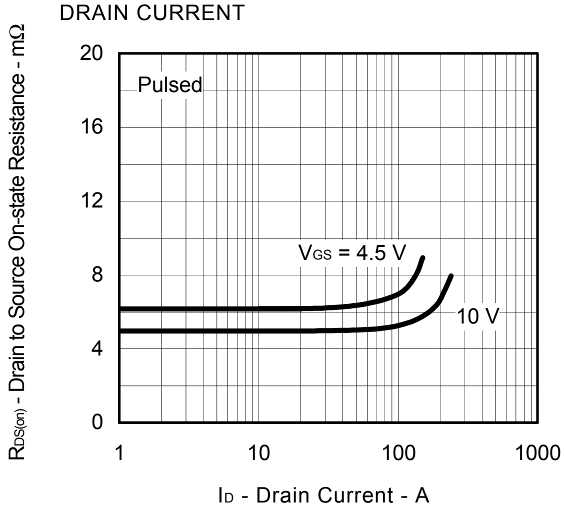
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



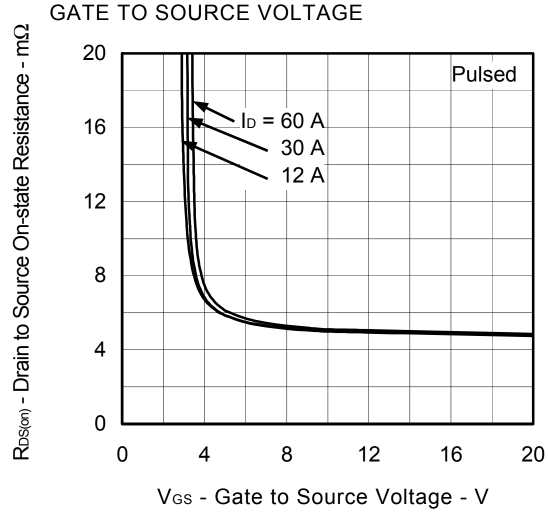
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



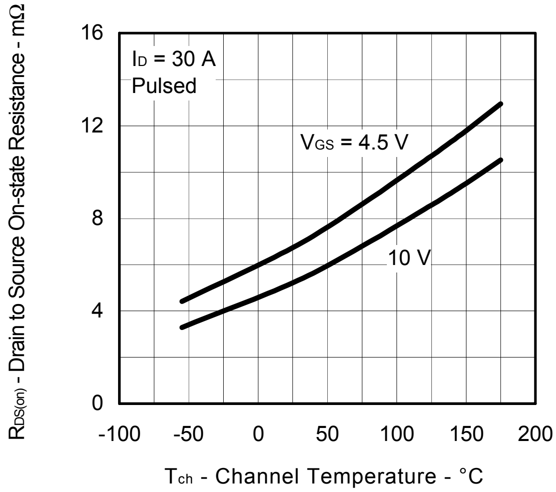
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



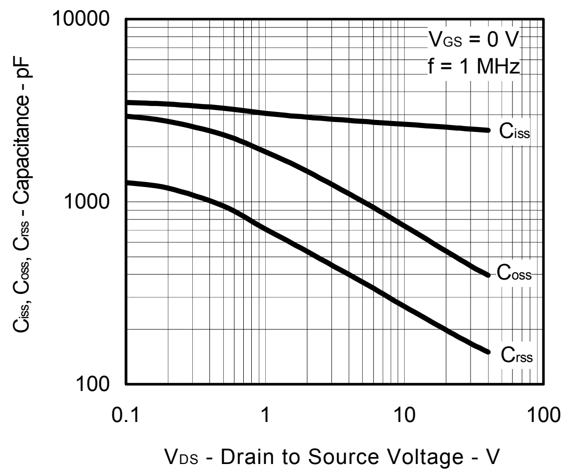
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



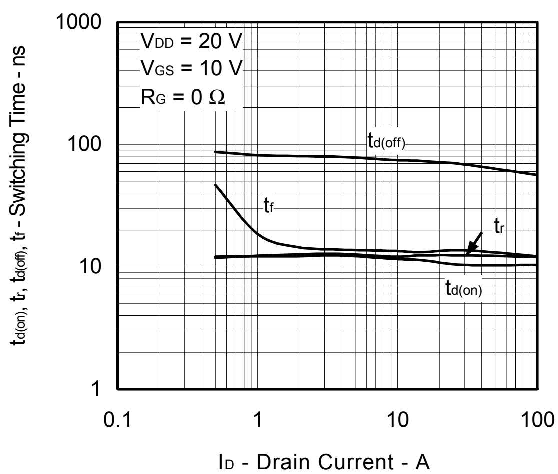
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



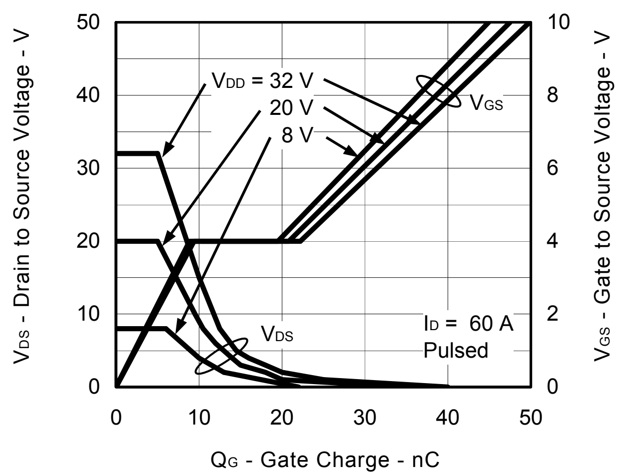
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



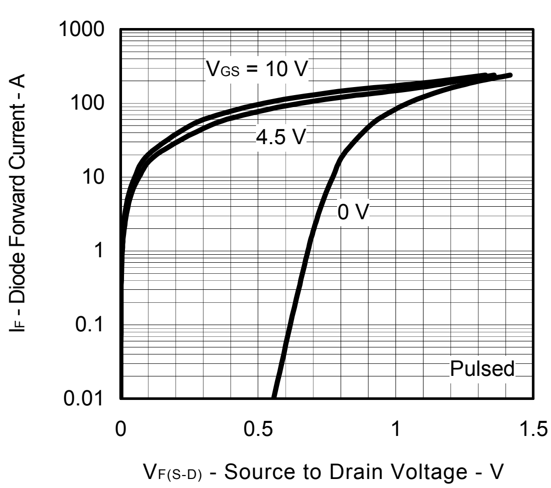
SWITCHING CHARACTERISTICS



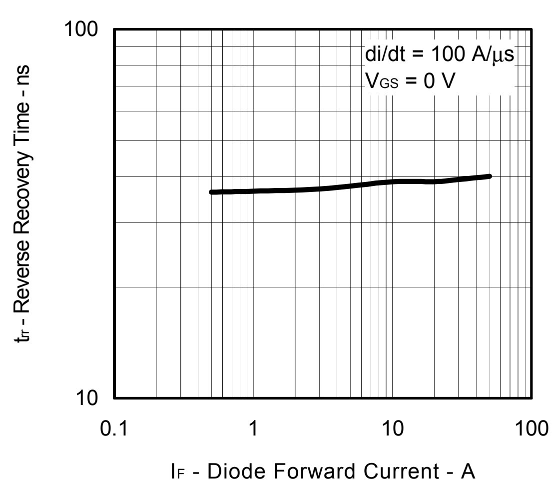
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

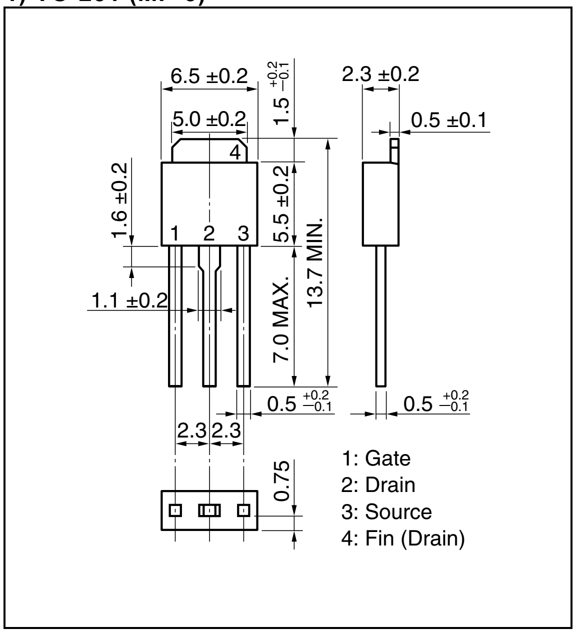


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

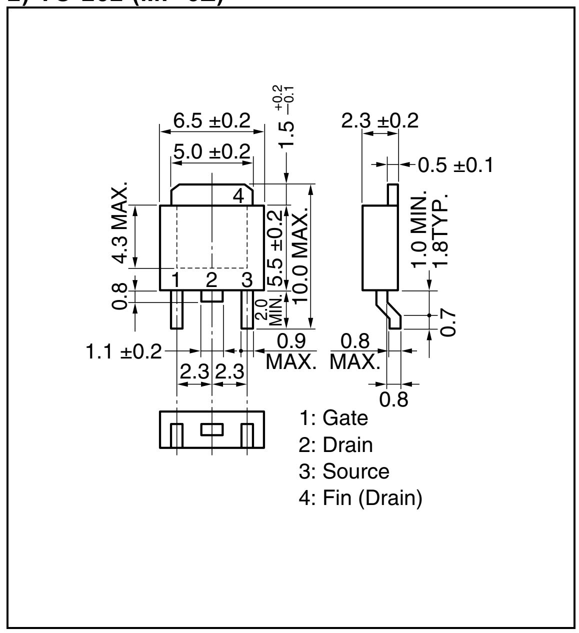


PACKAGE DRAWINGS (Unit: mm)

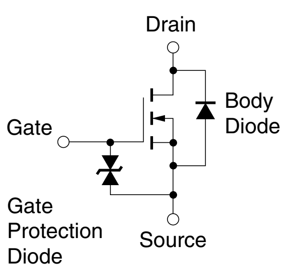
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.