Ground Bounce Noise in TTL Logic

High-speed TTL octal drivers such as the FCT244 can generate ground bounce noise when driving capacitive loads at high-speed. On the FCT244, ground bounce occurs when seven of the eight outputs are switching HIGH-to-LOW with a high capacitance load, and the eighth output is held a constant LOW. In this case, the HIGH-to-LOW transition of the outputs causes capacitive current (I = CdV/dt) to flow in the single ground lead of the FCT244. This current pulse causes a voltage pulse to appear (V = Ldi/dt) across the package inductance of the ground lead. This voltage pulse on the unchanging LOW output is called ground bounce noise. This voltage pulse will appear on the output that is held LOW, since it shares the common ground pin.

Ground bounce noise is a concern of the system designer because it can affect other circuits in a design. Ground bounce is a chip design problem with system implications. The chip designer tries to achieve the highest speed with an acceptable level of ground bounce. The system designer needs to understand the limits of the combination of chip and package technology represented by ground bounce to know what to expect from future designs. A ground bounce model is a useful tool for achieving these goals. In this paper, we will study ground bounce using an RLC resonant circuit model.

Ground Bounce Example

Figure 1 shows a test setup which allows ground bounce to be measured, and Figure 2 shows typical results.

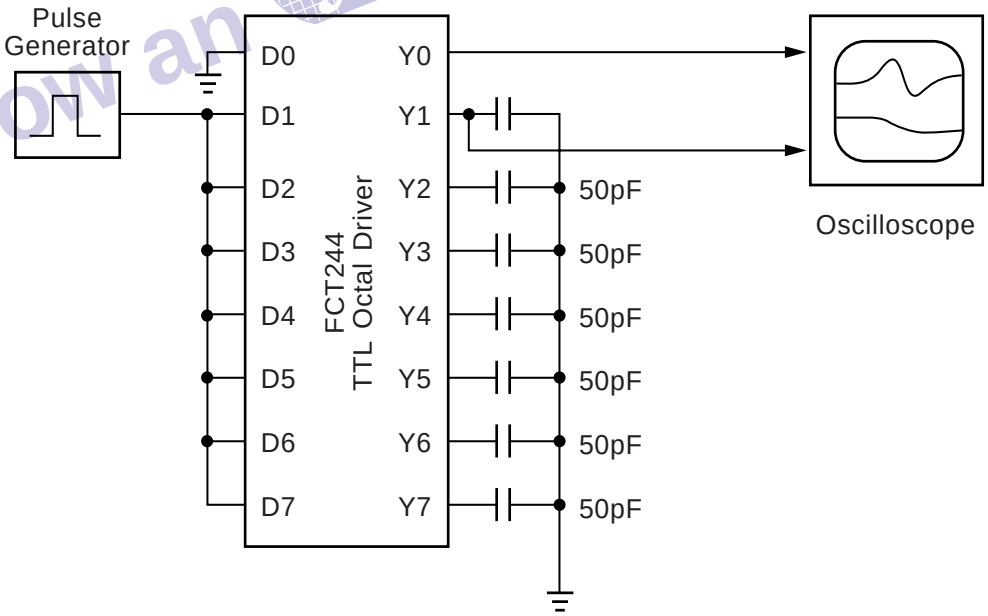


Figure 1. Ground Bounce Test Setup

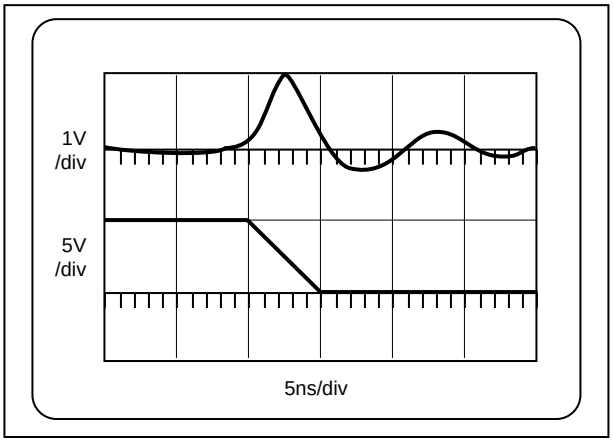


Figure 2. Ground Bounce Noise Oscilloscope Trace

Problems Caused by Ground Bounce in TTL System Designs

Ground bounce noise is a problem when it couples into other circuits or when it upsets the operation of the IC that generates it. Ground bounce noise is a problem in bus driver chips when the unswitched output is a control signal used to enable or clock other circuits. Ground bounce is not a problem in data or address bus driver circuits where all outputs switch and settle at the same time and their associated circuitry waits until the signals are settled before sampling them. Ground bounce is an indirect problem in these cases to the extent that it increases system noise and corresponding settling times in general.

Ground bounce noise is a problem only if it affects the circuits it drives. Whether driven circuits are affected is determined by the difference between the ground bounce pulse size and duration and the dynamic (AC) noise margin of the driven circuit. Dynamic noise margin is a function of the logic family of the driven circuit: i.e., LS, AS, F, HCT, etc. A plot of dynamic noise margin for various TTL logic families and showing typical ground bounce pulses is shown in Figure 3.

Ground bounce is associated with HIGH-to-LOW switching in TTL designs. In the HIGH-to-LOW (ground bounce) case, the unswitched output is connected directly to ground. The ground bounce spike from the internal ground is coupled directly to the output. In the LOW-to-HIGH (V_{CC} bounce) case, the unswitched output is either connected directly to the internal V_{CC} in a CMOS output or buffered from V_{CC} by a source- or emitter-follower transistor in the TTL output case. In the CMOS output case, the V_{CC} bounce noise margin is (5-1.5) = 3.5V, more than twice the ground bounce margin. In the TTL output case, the source/emitter-follower buffer isolates the V_{CC} bounce from the actual output.

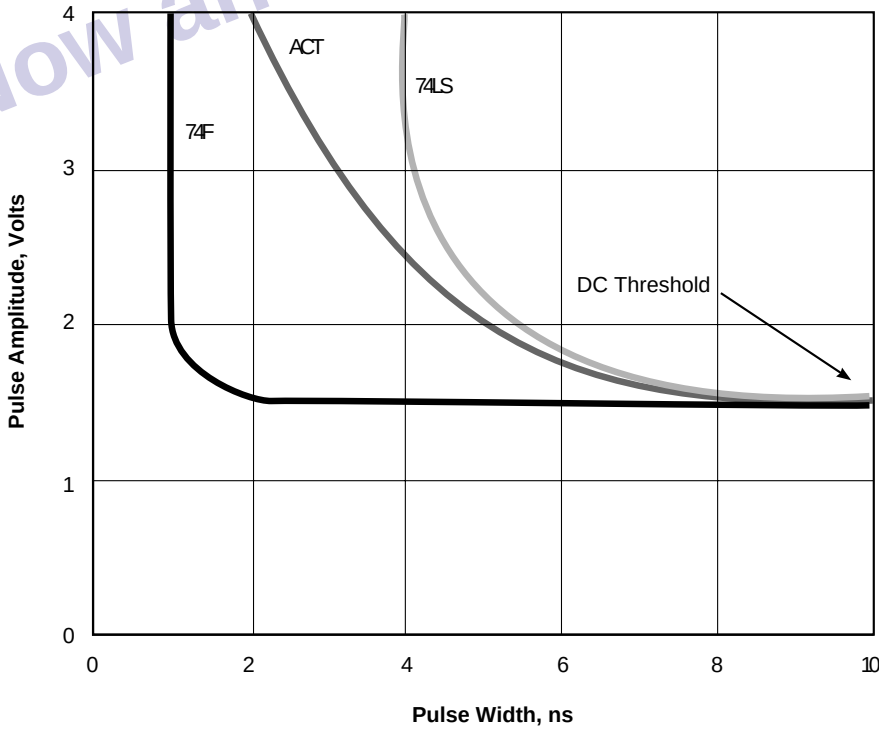


Figure 3. Dynamic Noise Margin of Various TTL Logic Families

Problems Caused by Ground Bounce in TTL Chip Designs

Ground bounce has significance for the chip as well as the system. When a ground bounce pulse is generated, the chip ground voltage is changed relative to the outside, system ground. Since the inputs to the chip are referenced to system ground, they appear to change relative to the chip ground as a result.

During the positive portion of the ground bounce pulse, the internal ground is raised. This makes the inputs appear as though they have a negative pulse added to them equal to the ground bounce pulse. If the ground bounce pulse is large enough and the driving circuit has a LOW V_{OH}, the HIGH inputs would be pulsed below their thresholds. This can cause false clocking on register parts such as FCT374, etc. and false clocks and reset pulses on FIFOs such as 512 x 9 devices. It can also cause noise pulse injection on RAM address lines. This can result in longer access times because of disturbance of the address decoders and reactivation of the address transition detect circuitry.

After the positive portion of the ground bounce pulse, there is a negative, undershoot portion approximately equal in size to the ground bounce pulse. This makes the internal ground fall and causes logic LOW inputs to appear as though they have a positive pulse on them. This can cause false clocking on latch devices such as FCT373 which require their latch inputs to remain LOW to retain data. This undershoot pulse can also cause double clocking on registers and FIFOs during the time the clock pulse is held LOW. The undershoot pulse causes an effective positive spike on the clock line, resulting in a second clock pulse. Undershoot can also cause noise pulse injection on RAM address lines.

Specifying Ground Bounce in TTL System Designs

Ground bounce is the result of an interaction of high-speed TTL circuits with their packages. It has become significant because of increased TTL speed. Because ground bounce is a result of speed, there is an inherent tradeoff between speed and ground bounce. Ground bounce can be optimized but not eliminated. For this reason, high-speed TTL logic should have a ground bounce specification.

A ground bounce specification should balance the need for speed against the need for noise margin. Defining an acceptable level of ground bounce must take both speed and the driven logic family into consideration. Speed and ground bounce are related. Lower ground bounce means lower speed for a given logic family, so ground bounce should not be arbitrarily set at some LOW value. However, once a ground bounce noise problem enters a design, it can be at least as difficult as other system noise problems to diagnose and solve.

Ground bounce can be “designed around” if necessary. In a typical system design, perhaps 2% of the design will be sensitive to ground bounce. For example, address and data bus drivers and receivers will not be directly sensitive to ground bounce, except for the additional system noise that ground bounce generates. A good system designer can avoid and/or compensate for potential ground bounce problems. This, however, is not desirable. Good system designers are too scarce and valuable to spend their time compensating for chip vendors’ problems unless there is no other choice. Also, designers implementing engineering changes may not have access to the original designer’s thinking on how to avoid ground bounce problems in the design.

Referring to Figure 3, a ground bounce peak value of 1.5V for nominal pulse widths in the 3-5ns region is a reasonable ground bounce specification for many designers. This pulse will be below the threshold of CMOS TTL logic families and just at the threshold for bipolar TTL such as 74F devices. If the ground bounce pulse is 1.5V or below, it should not propagate through bipolar TTL devices.

Ground Bounce RLC Simulation Model

Ground bounce can be modeled for SPICE analysis as shown in Figure 4. This diagram represents an octal device such as an FCT244, with 7 of 8 outputs switching HIGH-to-LOW and the 8th output unswitched. Seven of the eight load capacitors have been charged to V_{OH} and are discharged through the ground lead inductance when their respective transistors switch. The eighth transistor remains on as the unswitched output.

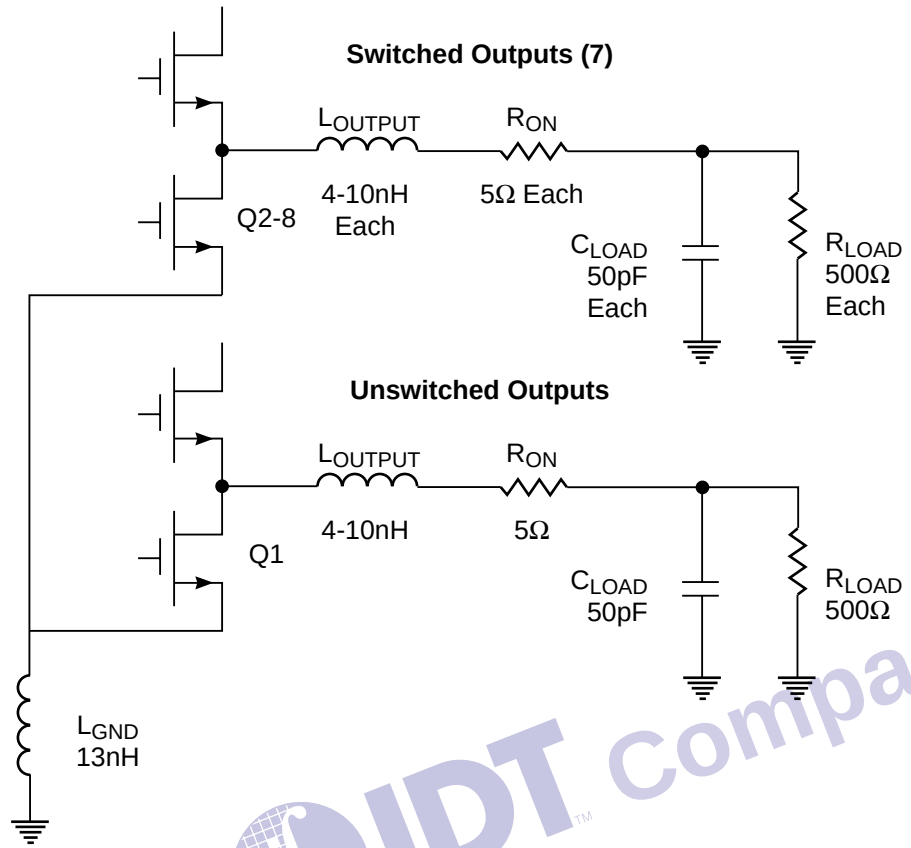


Figure 4. Ground Bounce Circuit

A simplified RLC model of the circuitry of Figure 4 is shown in Figure 5. In this figure, all eight outputs are assumed to be switching for maximum ground bounce. Since the load capacitors, load resistors, and lead inductances are effectively in parallel, their nominal values per pin are divided by eight. The ground inductance is in common with all, its value remains unchanged. Ground bounce appears across the ground lead inductance, L_{GND}. The series inductances per pin have been eliminated. This is done to simplify the model. It can be done because their paralleled value is small with respect to L_{GND}, and ignoring them will result in ground bounce values at least as bad (generally 2-5% worse) as if they were included.

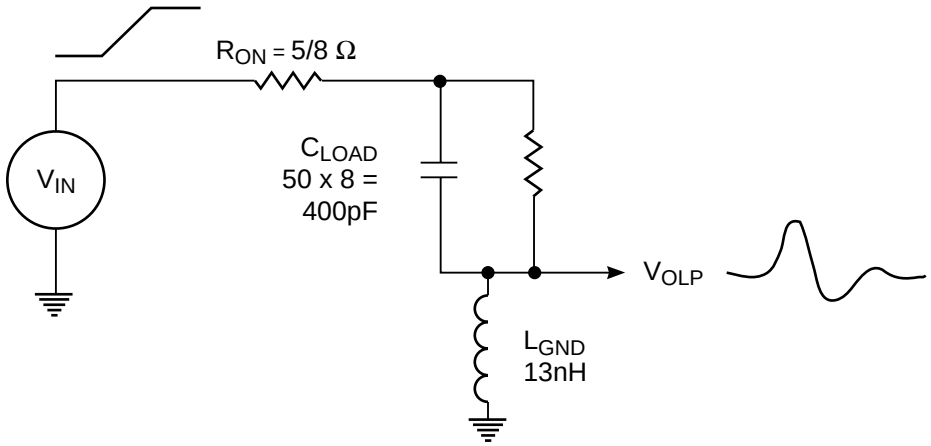


Figure 5. RLC Ground Bounce Model

Output Switching Transistor as a Voltage Ramp Generator

In the RLC model above, the HIGH-to-LOW switching action of the output transistors has been replaced by a voltage ramp generator, V_{IN}. This is one of several simplified models, such as modeling the switch as a current ramp generator or a simple switch with a variable series resistance. Voltage ramp generators are easy to model in SPICE, and node voltages are the usual variables that are observed and controlled by the designer. The most important consideration, however, is that when high current capability CMOS outputs are modeled as voltage ramp generators in the RLC model, the results correspond very well with observed data.

High speed CMOS based TTL devices act like voltage ramp generators. Their output fall time does not vary appreciably over the range of 5-50pF. If they were current sources or current limited voltage sources, one would expect the fall time to be proportional to the capacitance, at least above some value. Examining the current required to drive ground bounce in these high drive (typically above 100mA) CMOS devices is instructive.

To verify whether the outputs are current limited during the ground bounce, consider the current built up in the ground inductance at the peak of the ground bounce pulse. This current is the integral of the ground bounce pulse divided by the inductance. If we consider the ground bounce pulse to be a half-sine wave, the inductor current at its peak is:

I_{VPEAK} = (GB peak voltage)(1/2 GB Pulse Width) (Average Value of a half-sine wave) / (L_{GND})

= 0.319(GB peak voltage)(GB Pulse Width) / (L_{GND})

= 0.319(1.5)(5.0)/(13) = 0.184 /8 = 23mA per output for a 1.5V, 5ns pulse

We are not particularly interested in the current after the voltage peak because it can cause no further increase in ground bounce. Knowing the peak current, we can calculate the maximum ground bounce pulse width where the outputs can still be considered to be voltage ramp controlled. If the saturation current is given by I_{OL}, this will be given by:

I_{OL} = I_{VPEAK} = 0.319(GB peak voltage)(GB Pulse Width) / (L_{GND})

GB Pulse Width = I_{OL} / 0.319(GB peak voltage) = 3.14 (I_{OL})(L_{GND}) / GB peak voltage

For high-speed CMOS parts such as the FCT series, the outputs are rated at 64mA, and are typically capable of more than twice this rating in order to guarantee DC specifications over the temperature range. Using a value of 128mA per output as the current limit and 13 nanohenries as the ground lead inductance gives the following values for the maximum ground bounce pulse width before current limit.

GB Pulse Width = 3.14 (8 x 0.128) (13) / (GB peak voltage)

= 41.82 / (GB peak voltage)

= 41.8ns @ 1.0V peak ground bounce

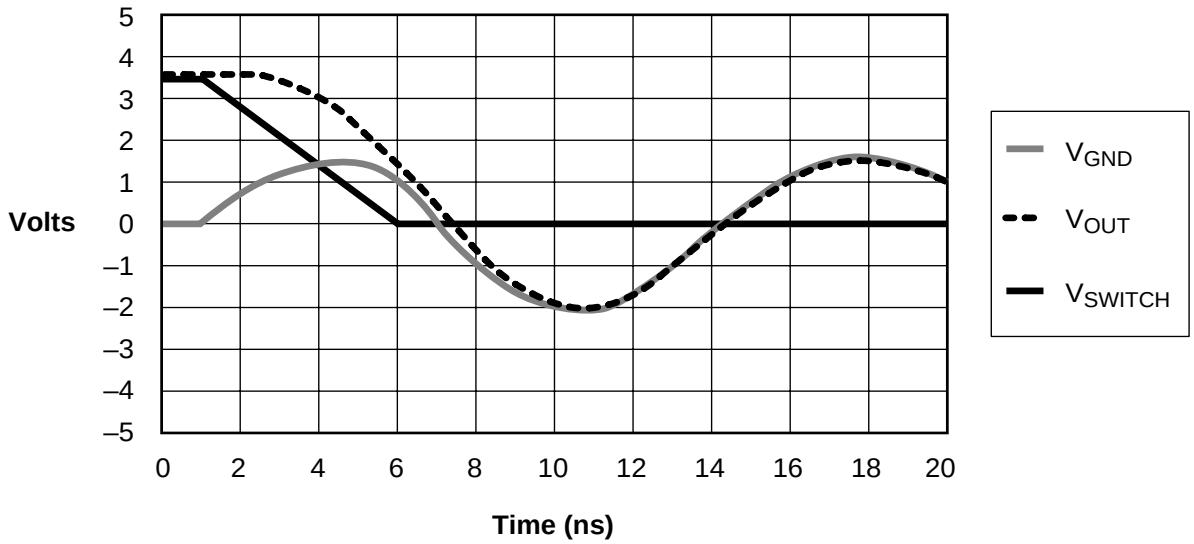
= 27.8ns @ 1.5V peak ground bounce

= 13.9ns @ 3.0V peak ground bounce

These values are significantly above typical ground bounce pulse widths, which are in the 3-5ns range. This tends to support the voltage ramp model for the high-speed, high current devices used in TTL devices with significant ground bounce.

RLC Model vs. Actual Waveforms

The validity of the RLC model can be determined by comparing a plot of the model output for appropriate values of R, L, C, and fall time versus results measured in the laboratory. Figure 6 shows a plot of the RLC model output using nominal values for nominal CMOS circuit resistance and fall time for an FCT244 in a 300 mil plastic DIP package. The ground bounce results shown are for all eight outputs switching; for 7 of 8 switching, the ground bounce values are multiplied by 7/8.



Values Used:		
	Inductance	13 nanohenries
	Capacitance	50pF/output
	Resistance	5Ω/output
	V_{OH}	3.50V
	Fall Time	5ns, 3.5V to 0V

Figure 6. RLC Model Ground Bounce Waveforms

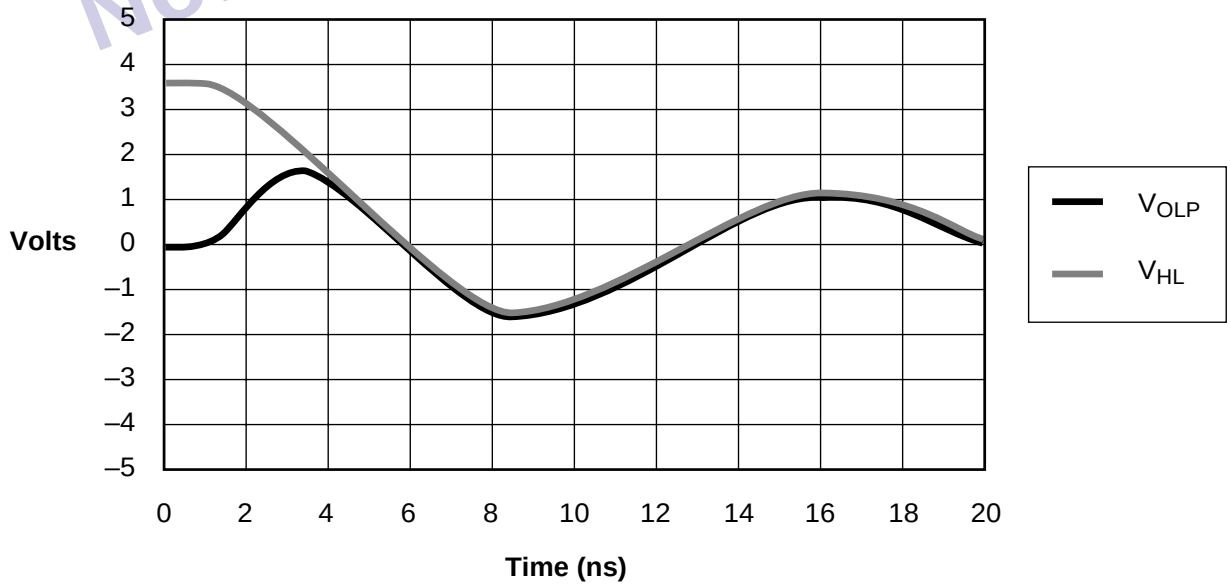


Figure 7. Measured Ground Bounce Data for QSFCT244

Figure 7 shows a plot of laboratory data recorded for a commercially available FCT244 device using the configuration of Figure 1. A high performance ground bounce test jig was used and the results recorded and plotted using a 1GHz bandwidth sampling oscilloscope. The RLC model data in Figure 6 compares reasonably well with the recorded data in Figure 7.

RLC Model Simulation Study

Using the RLC model, a simulation study was performed using various values of R, L, C, and output fall time (t_F) to reveal their effect on ground bounce and propagation delay. Given the RLC model, several useful observations can be made before simulations are begun. These are as follows.

Ground Bounce Is Proportional to V_{OH}.

Ground bounce is the result of discharging the load capacitance through the package inductance. Since the load capacitance is charged to V_{OH}, the ground bounce will be directly proportional to V_{OH}.

t_{PHL} Reduces with V_{OH}

Reducing V_{OH} reduces the voltage swing required to reach threshold as a percentage of the total logic swing. For a given total fall time, the time to go from V_{OH} to threshold is reduced as V_{OH} is reduced. An extreme example would be if V_{OH} were 1mV above threshold, yielding a t_{PHL} of nearly zero.

Ground Bounce Proportional to the Number of Outputs Switching

Ground bounce is the result of discharging the load capacitance through the package inductance. If all outputs switch, ground bounce reaches its full value. If some of the outputs switch and some are held low, there will be charge sharing between the capacitors at the beginning of the switching interval with the capacitors charged to V_{OH} sharing charge with those that are not. After charge sharing, the effective V_{OH} is equal to the actual V_{OH} times the ratio of the number of outputs switching to the total number of outputs, i.e., if only half the outputs switch, the effective V_{OH} will be half the nominal V_{OH}.

Ground Bounce Is a Non-linear Function of t_F, R, L, C

The RLC circuit forms a two pole HIGH pass RLC filter for ground bounce. The typical fall time of the CMOS circuits of interest (3-5ns) is similar to the RLC resonant time constant (70MHz ≥ 2.28ns). Ground bounce will therefore be a function of the fall time relative to the resonant frequency as determined by R, L, and C. Changes in the resonant frequency are generally proportional to the square root (i.e., nonlinear) of changes in L and C, with R providing an additional term under the square root sign. Simple linear approximations can therefore be misleading.

t_{PHL} Has a Lower Limit Determined by the Resonant Frequency of the RLC Circuit

The output of the TTL device appears across the load capacitor, not across the switch. Since the load capacitor is part of a resonant circuit, its rise and fall time will be limited by the resonant frequency of the RLC circuit. The minimum fall time as seen by the load will be the time required for the capacitor to reach (V_{OH}-$V_{THRESHOLD}$). If the threshold is half the logic swing (V_{OH} = 3.0V), this will correspond to $COS^{-1}(0.5) = 60°$. The minimum propagation delay will therefore be (60/360)*(1/70MHz) = 2.38ns.

Ground Bounce vs. Fall Time and Resonant Frequency

Figure 8 shows a plot of ground bounce voltage, V_{OLP}, as a percentage of V_{OH} versus fall time as a fraction of the resonant time constant, i.e. t_F vs $1/2\pi\sqrt{LC}$. This is a plot for various values of package inductance (L), load capacitance (C) and fall time (t_F) with R = 5Ω for the on resistance of the CMOS switch. Using the resonant frequency of the load capacitance and the package inductance allows the graph to be normalized for these various values.

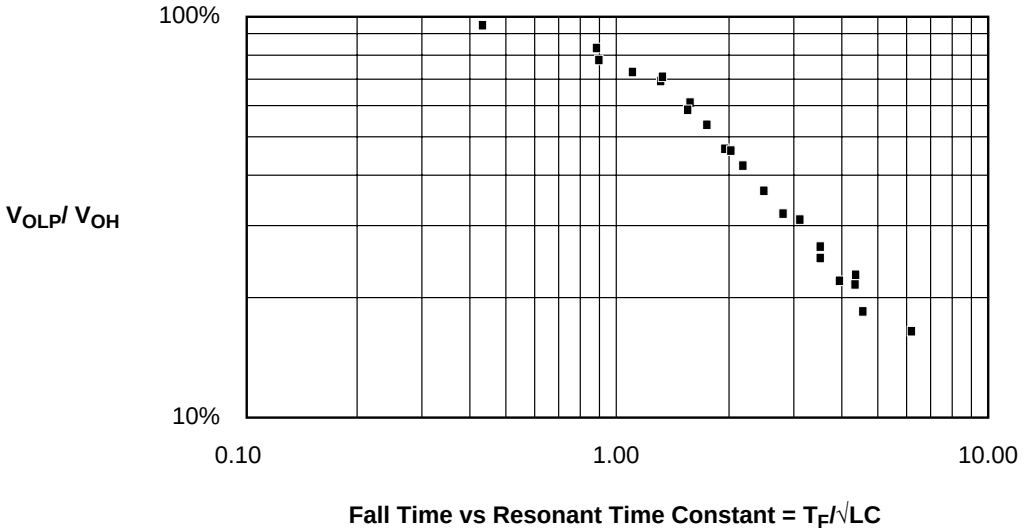


Figure 8. Ground Bounce vs. Fall Time Relative to Resonant Time Constant

The plot of the data shows a HIGH pass filter function with the ground bounce decreasing as the fall time increases. When the fall time is small relative to the resonant time constant, the ground bounce approaches V_{OH} as an asymptote.

Ground Bounce vs. Package Inductance

Figure 8 is instructive as an overview, but it is more instructive to examine how we can affect ground bounce by varying specific parameters such as package inductance, etc. Figure 9 shows a plot of ground bounce versus package inductance for a fixed fall time of 5ns and a fixed load capacitance of 50pF per output.

As the chart shows, ground bounce goes up with inductance. Increasing inductance decreases the resonant frequency. This increases the resonant time constant, decreases the ratio of fall time to this time constant, and therefore increases the ground bounce. Since resonant frequency is a function of the square root of the inductance and capacitance, cutting the inductance in half does not cut the ground bounce in half, as some simpler models show.

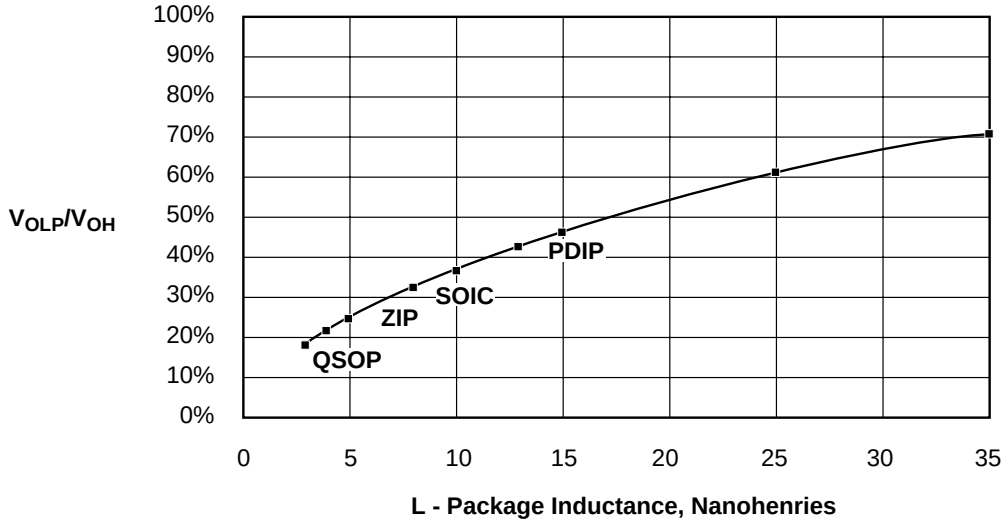


Figure 9. Ground Bounce vs. Package Inductance

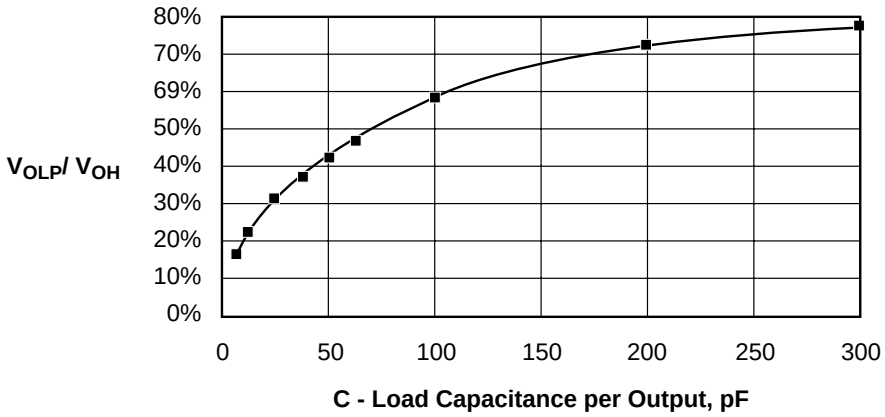


Figure 10. Ground Bounce vs. Load Capacitance

Ground Bounce vs. Load Capacitance

Figure 10 shows a plot of ground bounce versus load capacitance for a fixed package inductance of 13 nanohenries, a fixed fall time of 5ns, and a series resistance of 5Ω.

As the chart shows, ground bounce goes up with capacitance. Increasing capacitance decreases the resonant frequency. This increases the resonant time constant, decreases the ratio of fall time to this time constant, and therefore increases the ground bounce. Since resonant frequency is a function of the square root of the inductance and capacitance, cutting the capacitance in half does not cut the ground bounce in half, as some simpler models show.

Ground Bounce vs. Series Resistance

Adding series resistance will reduce ground bounce. The added series resistance increases the total impedance in the RLC current loop, reducing the current in both L and C. This causes the decrease in ground bounce. It also causes an increase in propagation delay because increasing the resistance increases the damping factor of the resonant circuit, lowering its resonant frequency. If the added resistance is less than the critical damping resistance a significant decrease in ground bounce can be traded for a small increase in propagation delay.

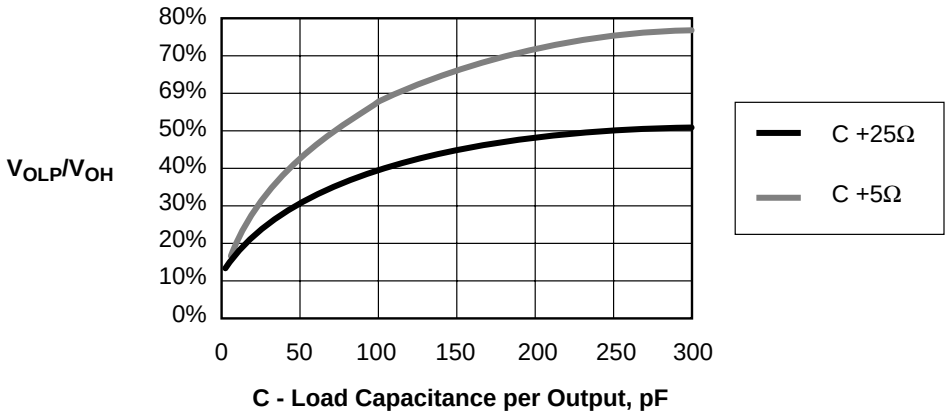


Figure 11. Ground Bounce vs. Load Capacitance with Series Resistance

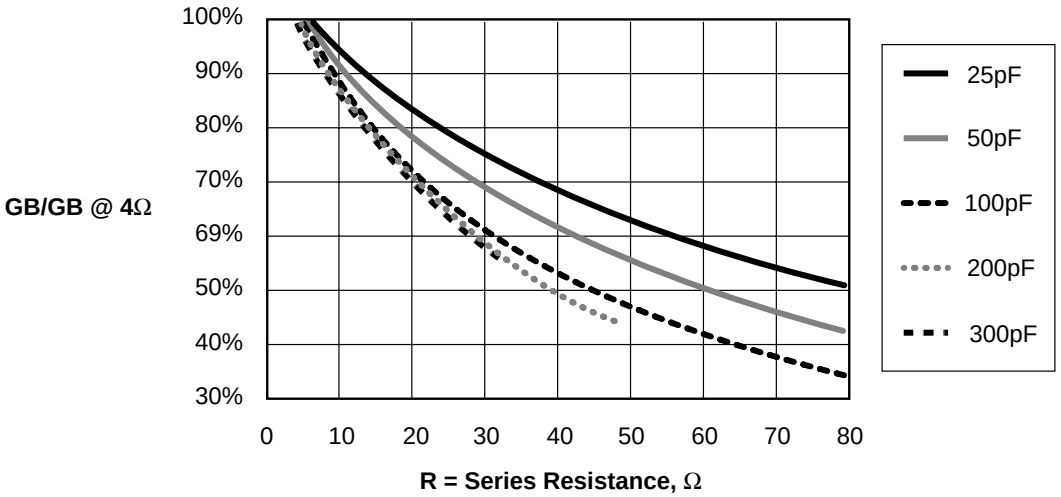


Figure 12. Ground Bounce vs. Series Resistance

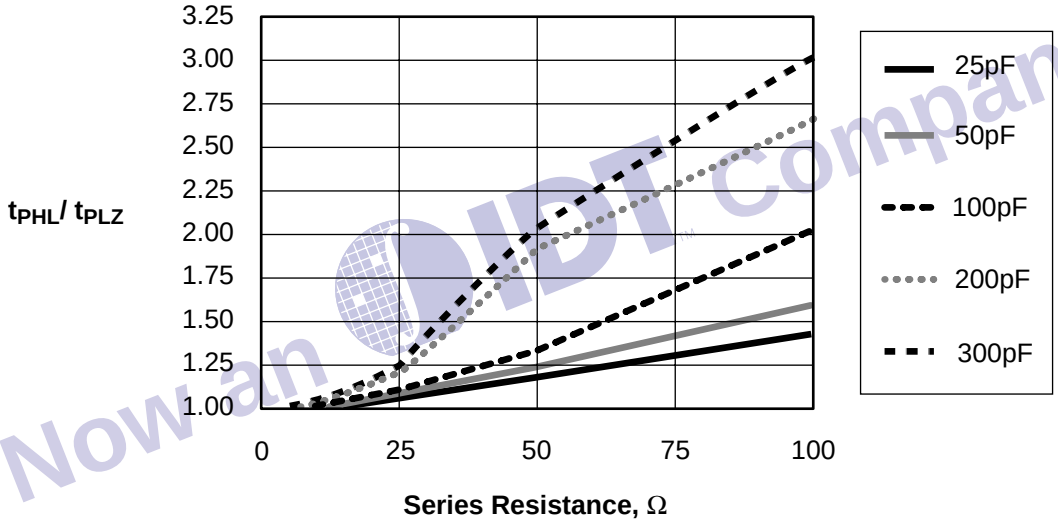


Figure 13. Propagation Delay vs. Series Resistance

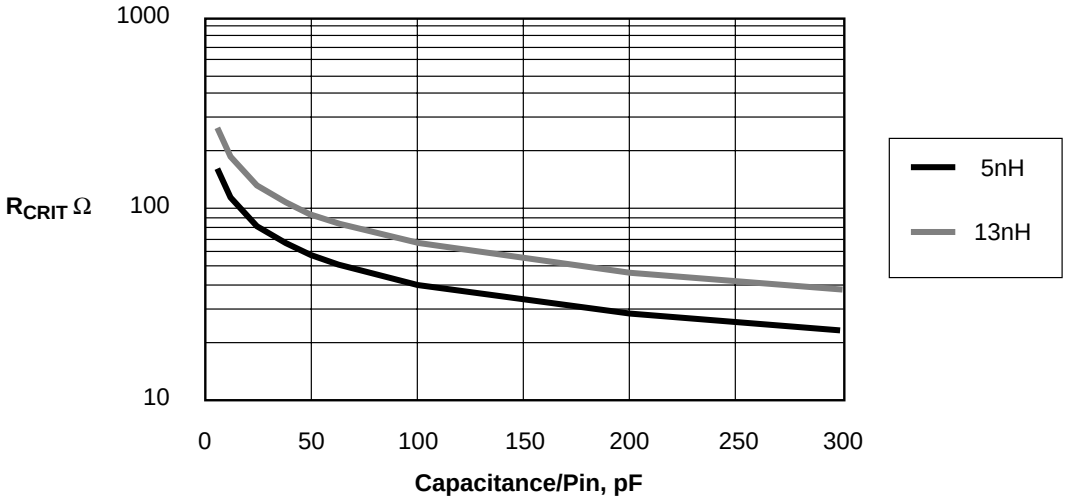


Figure 14. Critical Damping Resistance vs. Load Capacitance

The preceding figures show the results of adding series resistance. Figure 11 shows a plot of ground bounce versus load capacitance for L = 13 nanohenries, t_F = 5ns, and series resistances (R) of 5Ω and 25Ω. Figure 12 shows a plot of relative ground bounce reduction versus series resistance.

Figure 13 shows a plot of propagation delay versus series resistance for various values of capacitance and for L = 13 nanohenries and t_F = 5ns. This is a minimum propagation delay and is the delay associated with the resonant RLC circuit, as derived from the simulations.

As can be seen from the figure, the propagation delay rises slowly with damping resistance below 50Ω, above which it rises rapidly for high capacitance loads. This is because the resistance has risen above the critical damping resistance for the resonant circuit for these loads. Above the critical damping resistance, the circuit is no longer resonant, ground bounce becomes proportional to the L/R time constant and propagation delay becomes proportional to the RC time constant. To determine this point, Figure 14 shows a plot of critical damping resistance versus load capacitance.

Propagation Delay vs. Ground Bounce

Given the data if Figure 14, we can plot propagation delay versus ground bounce. Figure 15 shows such a plot for the case of V_{OH} = 3.5V, L = 13 nanohenries and C = 50pF/pin. In this figure, the main curve plots a relationship between ground bounce and propagation delay for various combinations of fall time (t_F) and series resistance (R).

Note that below the critical damping resistance of 91Ω for 50pF & 13nH, either series resistance or fall time can be used to trade ground bounce for propagation delay.

We can use the data in Figure 15 to show the tradeoff of ground bounce versus propagation delay as a function of the series resistance. The curves of Figure 16 plot the slope of the ground bounce versus propagation delay curve; i.e. the percent decrease in ground bounce divided by the percent increase in propagation delay as a function of series resistance relative to the critical damping resistance.

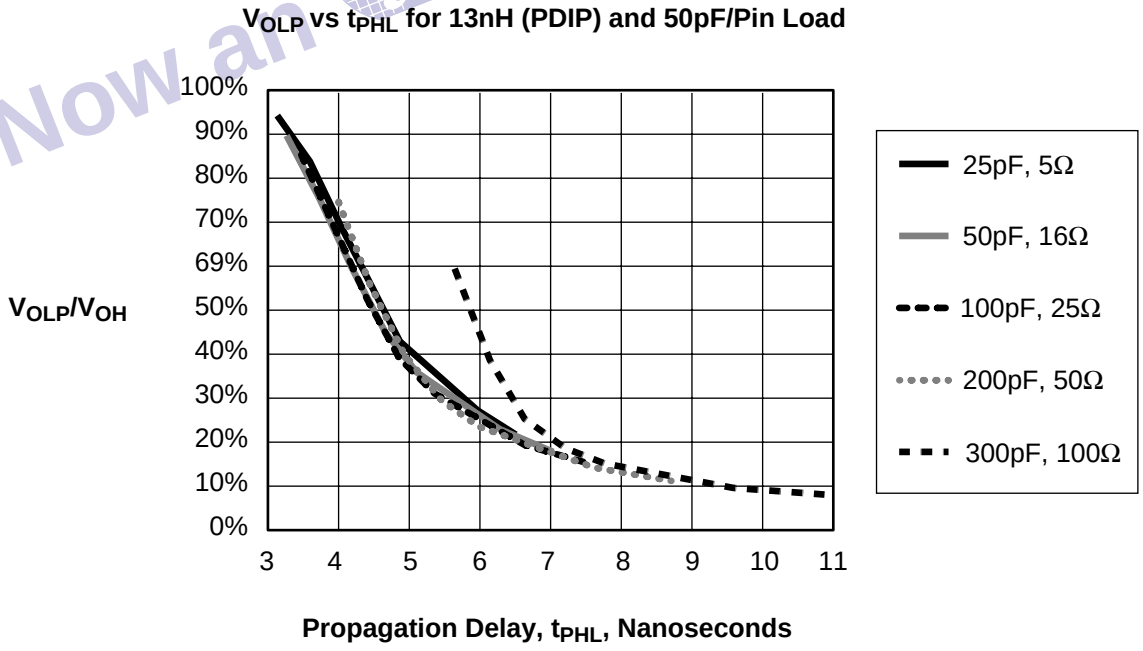


Figure 15. Propagation Delay vs Ground Bounce

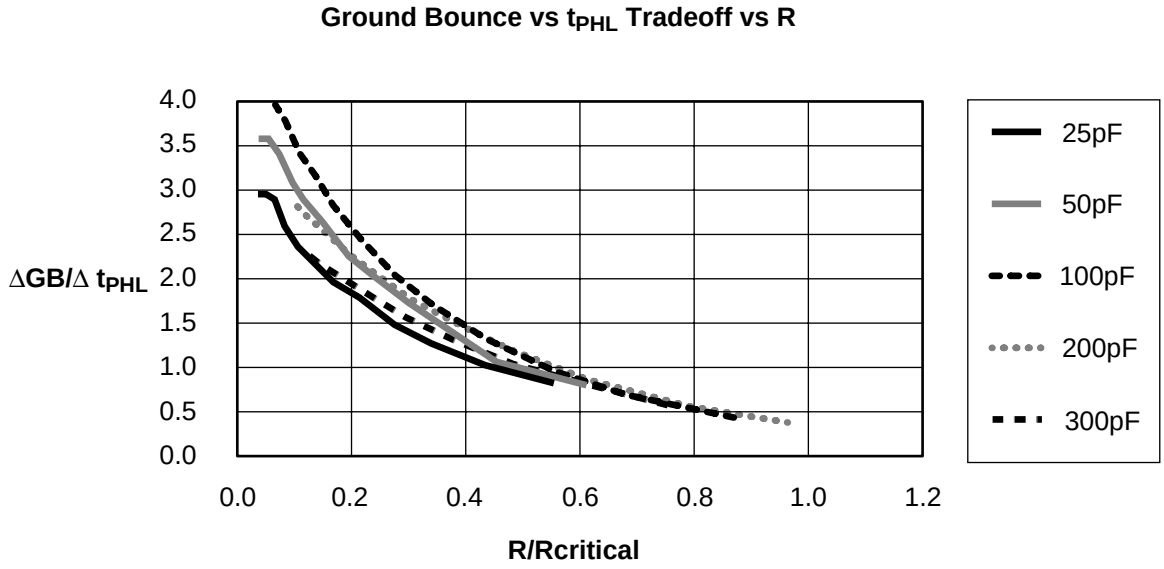


Figure 16. Ground Bounce vs. Propagation Delay Tradeoff versus Resistance

For small values of series resistance, ground bounce decreases faster than propagation delay increases. For values in the 5-10Ω range at 50pF loading, a 1% increase in propagation delay can be traded for a 3.5% decrease in ground bounce. One-half the critical damping resistance is the break-even point. For resistance values above this value, propagation delay increases relatively faster than ground bounce decreases. This implies that the series resistance should be less than half the critical damping resistance for the largest expected capacitive load.

Propagation Delay and Ground Bounce vs. V_{OH}

Propagation delay increases with V_{OH} because the output must travel a larger voltage difference between V_{OH} and the TTL threshold. Ground bounce is directly proportional to V_{OH}. This is shown in the plot of ground bounce versus HIGH-to-LOW propagation delay for three values of V_{OH} shown in Figure 17. The plot in Figure 16 is for L = 13 nanohenries, C = 50pF/pin, and various values of t_F.

Note that the HIGH-to-LOW propagation represents the minimum delay associated with the RLC resonant circuit. Propagation delay for other circuitry must be added to this for actual delays.

Propagation delay for other values of L and C for a given ground bounce can be calculated using this chart and multiplying the t_{PHL} value by the square root of the ratio of L or C to 13nH and 50pF, respectively.

Propagation Delay and Ground Bounce for Shaped Drive Pulses

Propagation delay for a given ground bounce can be improved if a shaped drive pulse other than a linear ramp is used. Propagation delay is determined by the rate of voltage build up on the load capacitor, which is determined by the rate of current build up in the ground inductor. To improve the propagation delay, you increase the ramp rate of current in the inductor.

The maximum possible current ramp rate in the inductor is determined by the inductance and the ground bounce by the rule V = L dI/dt. This could be achieved by using a current ramp instead of a voltage ramp and adjusting the ramp rate for the allowed ground bounce. The current ramp is adjusted so that the ground bounce pulse rises immediately to the desired ground bounce value and stays there until the output has achieved the HIGH-to-LOW transition.

The propagation delay time for a current ramp equal to V_{OLP}/L is determined by the capacitance and the difference between V_{OH} and the 1.5V TTL threshold by the relationship:

$$V = (V_{OH}–1.5) = Q/C$$

$$Q = \iint dI/dt = \iint (V_{OLP}/L)dt = (1/2)(V_{OLP}/L)t_{PHL}^2$$

$$t_{PHL} = SQRT(2*L*C*(V_{OH}–1.5)/V_{OLP}).$$

This represents the best possible propagation delay for a given RLC circuit and required ground bounce. A plot of ground bounce versus propagation delay for these conditions is shown in Figure 18. Ground bounce values were limited to 1.5V, the threshold voltage, for ease of analysis.

As in Figure 17, propagation delay for other values of L and C for a given ground bounce can be calculated using this chart and multiplying the t_{PHL} value by the square root of the ratio of L or C to 13nH and 50pF, respectively, as indicated by the above equation.

V_{OLP} vs t_{PHL} for 13nH (PDIP) and 50pF/Pin Load

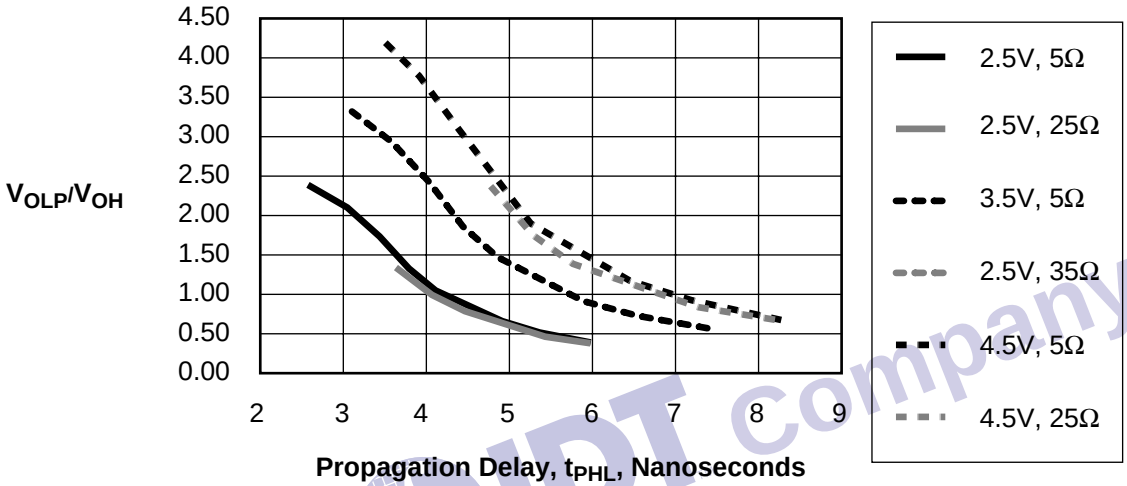


Figure 17. Ground Bounce vs Propagation Delay and V_{OH}

V_{OLP} vs t_{PHL} for 13nH (PDIP), pF/Pin Load, dI/dt Drive

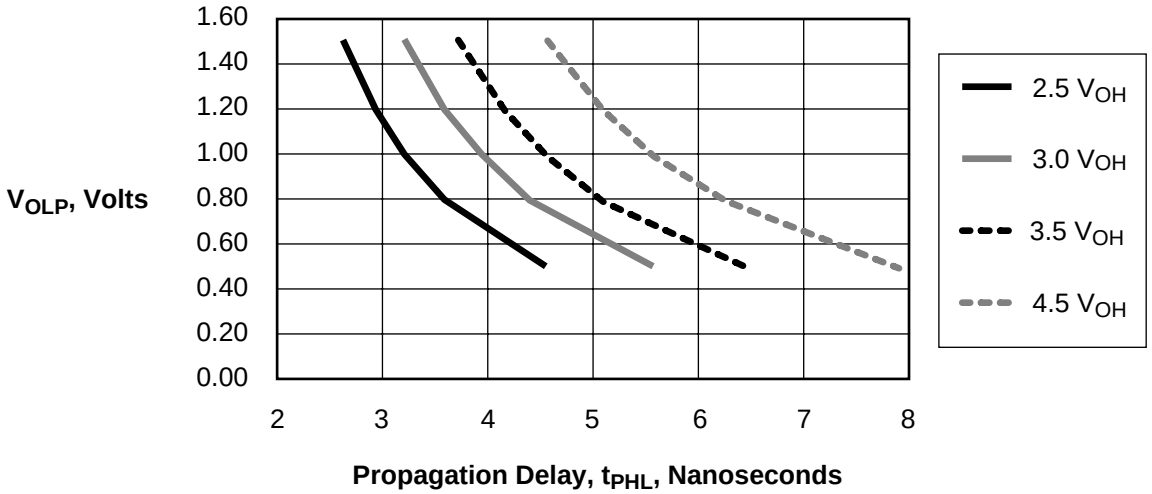


Figure 18. Ground Bounce vs t_{PHL} and V_{OH} for Ground Bounce Determined dI/dt