RZ/T1

Guidelines for Hi-Speed USB2.0 Board Design

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Summary

This document describes the guidelines for Hi-Speed USB 2.0 board design.

Operation Check Devices

The application explained in this document applies to the following .

· RZ/T1

Note: The contents in this document are provided as a reference example based on USB specification, and the signal system quality is not guaranteed. When implementing this example into an existing system, the overall system should be thoroughly evaluated, and the user should integrate at their own discretion.

Contents

1. Introduction

This document is described by using the pin names of RZ/T1 USB 2.0 host/Peripheral module. Table 1 lists the outline of host/Peripheral module pin.

Table1 Outline of RZ/T1 Host/Peripheral Module Pin

Pin Name	I/O	Function
USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus.
USB_VBUSIN	I	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. Whether VBUS is connected or disconnected can be detected during operation as a function controller.
USBA_RREF	I	Connect to VSS_USB via 200Ω ±1% resistor
USB_VBUSEN	O	VBUS(5V) supply enable signal for external power supply chip.
USB_OVRCUR	I	External overcurrent detection signal s should be connected to these pins.
VDD33_USB	I	3.3V digital power supply.
VSS_USB	I	Digital ground.
DVDD_USB	I	1.2V digital power supply.

2. USB Transmission Line

The USB transmission line indicates the wiring pattern that connects the USB connector and the RZ/T1 embedded USB transceiver.
USB 2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed (RZ/T1 not support) modes. The Hi-Speed mode has a 480 Mbps communication speed. Therefore, the USB transmission lines must be designed as a high-frequency circuit. Impedance control is required for the USB transmission lines.
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Notes on designing the wiring pattern of USB transmission lines are described below.

- The characteristic impedance required for the USB transmission lines is the differential impedance 90Ω ±15%.
- The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more details.
- The wiring pattern length of USB transmission lines from the RZ/T1 to the USB connector must be designed not to exceed the maximum delay time which is regulated by the USB specification. Table 2 lists the recommended values for the wiring pattern length of USB transmission lines for host and Peripheral.

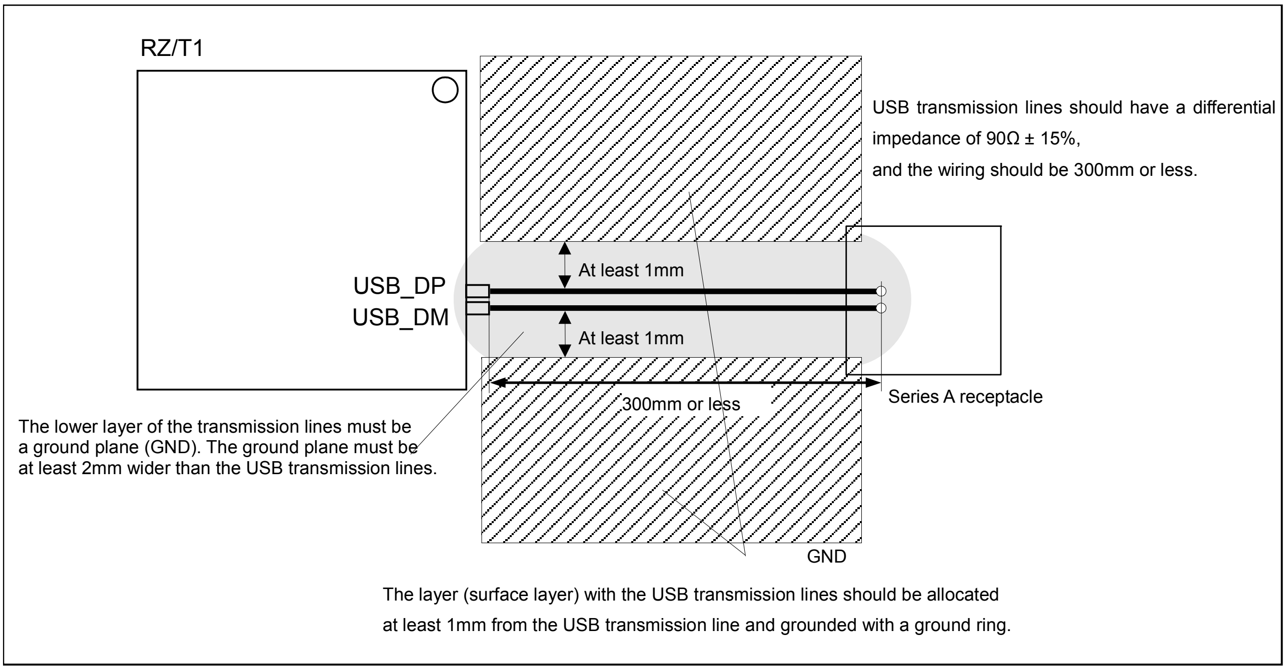
Table 2 Recommended Value for the Wiring Pattern Length of USB Transmission Line

	Maximum Delay Time (USB Specification)	Wiring Length	D+ and D- Wiring Length Differential
Host Controller	3ns	300mm or less	2.5mm or less
Peripheral Controller	1ns	100mm or less	2.5mm or less

- The lower layer of the USB transmission lines must be a ground plane. The ground plane must be at least 2mm wider than the USB transmission lines. The power supply for the ground plane is GND
- Do not allocate other signal lines near the USB transmission lines. Particularly lines of heavily fluctuating signals, such as clock and data bus lines must be allocated far from the USB transmission lines. Moreover, the USB transmission lines and other lines must not cross.
- The same layer (surface layer) as the USB transmission lines should be allocated 1mm from the USB transmission lines, and grounded with a guard ring.
- USB transmission lines should be allocated on the same layer without passing through a hole. In addition, wiring should not be divaricated.
- The USB transmission lines should be wired with uniform spaces.
- The USB transmission lines should be allocated far from the oscillator, power supply circuit, and other I/O connectors.
- The USB transmission lines should be wired with straight lines. If they are bent, they should be bent gently in an arc or up to 135 degrees, and not bent at acute angles (right angles).

Figure 1 shows a design example of a Host controller USB transmission line pattern, and figure 2 shows a design example of a Peripheral controller USB transmission line pattern.

Figure 1 Design Example of a Host Controller USB Transmission Line Pattern



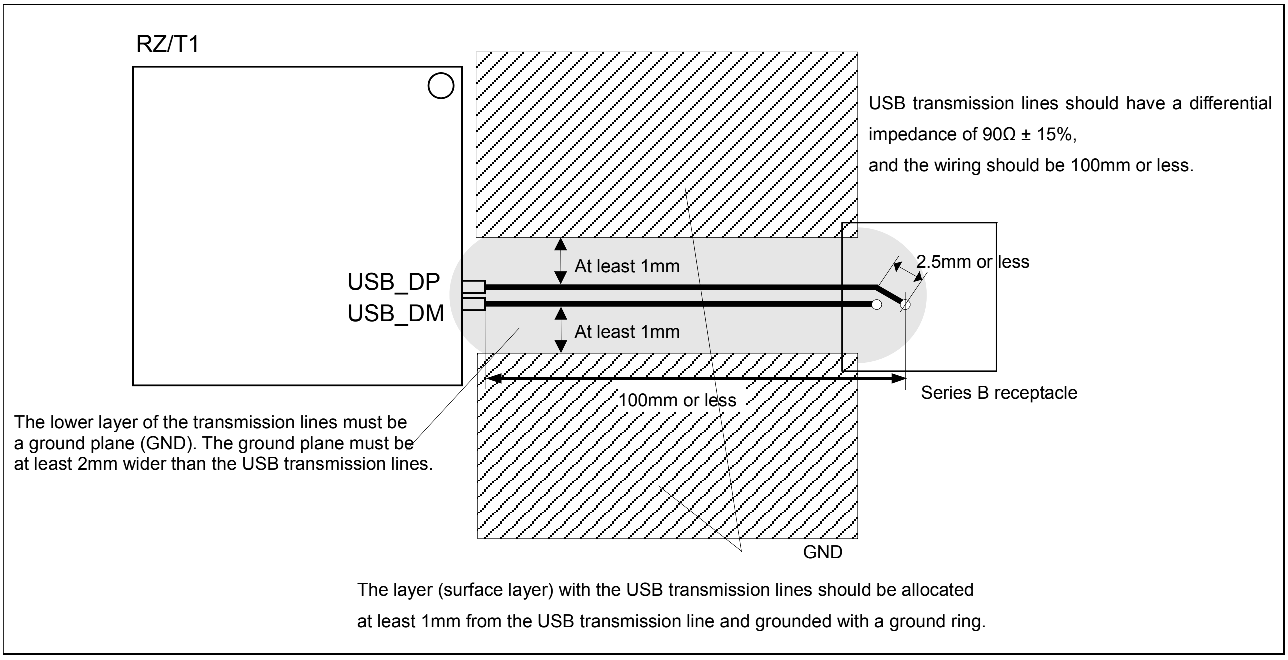


Figure 2 Design Example of a Peripheral Controller USB Transmission Line Pattern

3. Power Supply and Ground Pattern

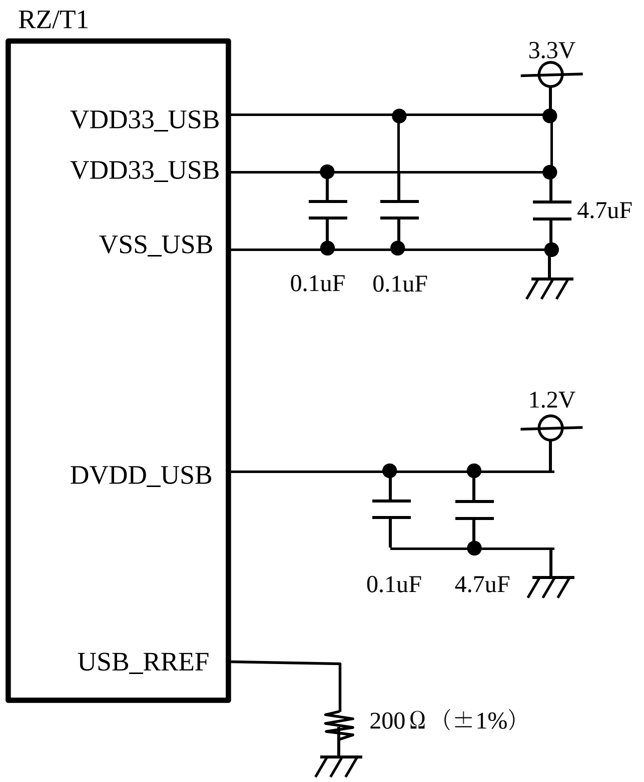
Notes on designing a power supply/ground pattern are described below.

- The patterns of power supplies and grounds should be designed with as wide a surface layer as possible.

- Tantalum capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as power supply capacitors.

- Aluminum electrolytic capacitors affect the jitter value when measuring the EYE pattern. The capacitors should be thoroughly designed and tested before use.

- As the capacitance value of decoupling capacitor, it is recommended that the capacities for 0.1uF, and 4.7uF are allocated closest to the USB power supply pin (It is possible only also by 0.01uF when used low ESR/ESL.). Figure 3 shows an example of decoupling capacitor allocation.



- The resistor connected to USB_RREF should be layout near the USB_RREF pin.
- The GND of resistor should be connect near the USB_VSS pin.

Figure 3 Example of Decoupling Capacitor Allocation

4. VBUS Power Supply Circuit

Notes on designing the VBUS power supply circuit are described below.

- When the RZ/T1 is used as a host controller, the additional capacity of the VBUS line should be designed to be 120uF or more.

- When the RZ/T1 is used as a Peripheral controller, the additional capacity of the VBUS line should be designed to be within 1.0uF to 10uF.

- The VBUS line should include a filter circuit as an overshoot may be caused by inconsistent impedance when the USB cable is connected. The 1.0uF capacitor and 100Ω to 1kΩ resistor should be added as a filter circuit. The constant should be defined after confirming that an overshoot has not occurred on the board. Also, a resistor of more than 1kΩ should not be added.

- When the RZ/T1 is used as a host controller, the VBUS power should be supplied to the Peripheral devices. A power supply switch IC with over-current protection for the USB power bus (hereinafter called “USB power supply switch IC”) is recommended for the VBUS power supply control. Make sure to consider the limitation value of the current of VBUS power supply line based on the current value used by the system power supply applied and the USB Peripheral devices communicated. In addition, refer to the USB power supply switch IC datasheet used for VBUS power supply control circuit.

Figure 4 shows an example of the VBUS power supply circuit when it is used as a host controller and Figure 5 shows an example of the VBUS power supply circuit when it is used as a Peripheral controller.

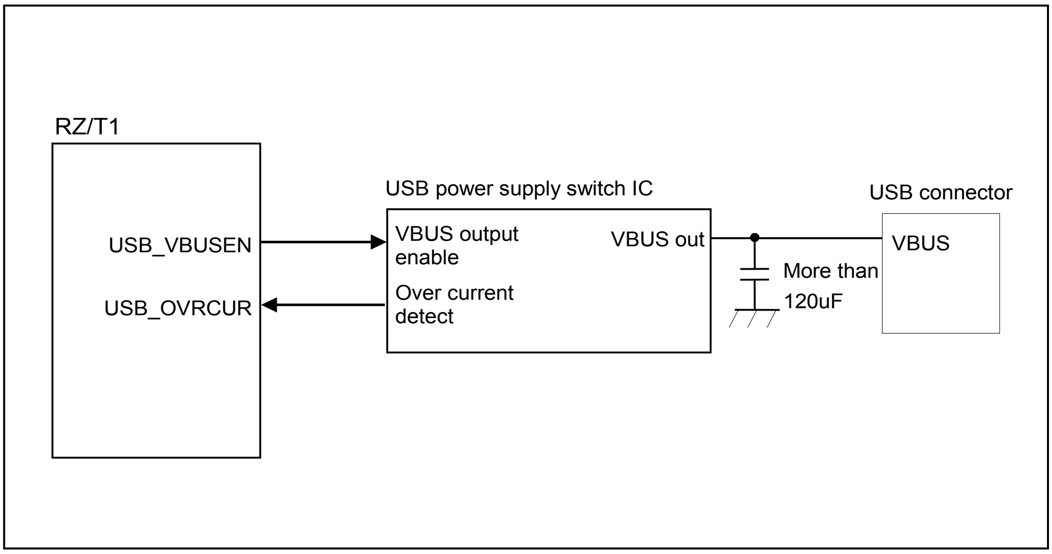


Figure 4 Example of Host Controller VBUS Power Supply Circuit

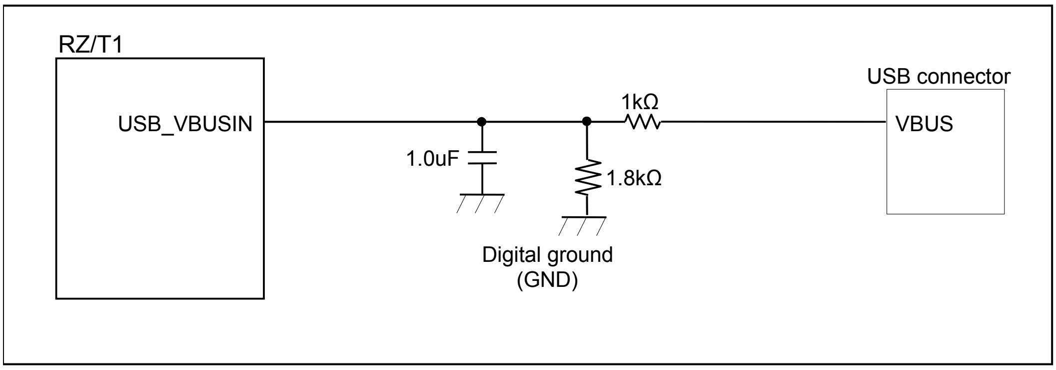


Figure 5 Example of Peripheral Controller VBUS Power Supply Circuit

5. EMI/ESD Workarounds

Notes on EMI/ESD workarounds are described below.

- When components for EMI/ESD workarounds such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.

- The components for the EMI/ESD workarounds must be USB 2.0 compliant. Also, by mounting EMI/ESD workaround components, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure 6 shows the block diagram of a connection example when the components for EMI/ESD workarounds are used.

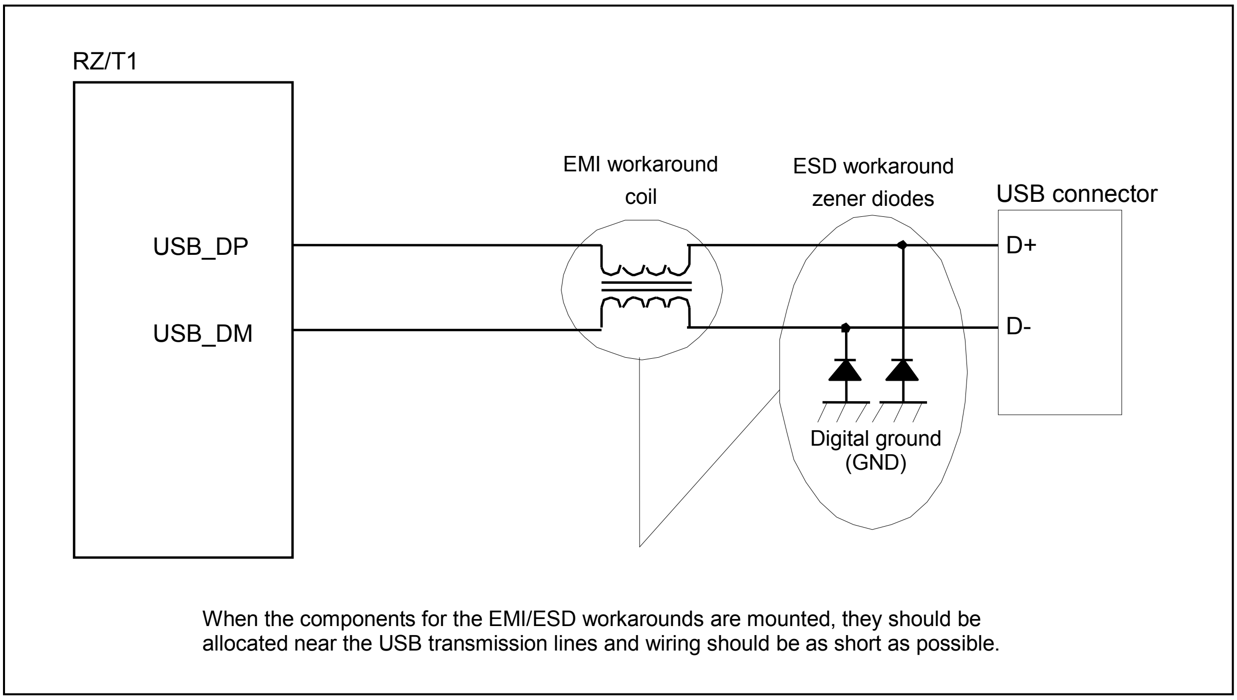


Figure 6 Connection Example When Components for EMI/ESD Workarounds are Used

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Revision Record

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		Page	Summary
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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