IDT80HSPS1616 PCB Design Application Note - 557

Notes

Introduction

This document is intended to assist users to design in IDT80HSPS1616 serial RapidIO switch. IDT80HSPS1616 based on S-RIO 2.0 spec offers 5Gbps and 6.25Gbps lane rates in 1x, 2x or 4x port configuration. This document is also a good reference for IDT's Central Packet Switch (CPS) family of devices, pre-processing switch and TSI family which are serial RapidIO switches with packet processing capabilities. These devices (CPS-8/12/16, CPS-10Q, CPS-6Q) based on S-RIO 1.3 spec offer 1.25, 2.5, and 3.125Gbps lane rates in 1x or 4x-port configurations in S-RIO 1.3 spec Note the S-RIO interface is a full duplex, point-to-point interface using differential signaling

A fundamental knowledge of high-speed design techniques is assumed. Details concerning PCB layout and differential impedance design are provided. The critical issues of controlled impedance of traces and connectors, differential routing, termination techniques, and DC balance must all be considered to get the best performance from the IC. This application note will help users to get the best possible performance from the IC and ensure first time success in implementing a functional design with optimal signal quality. It is intended that this document will be used in conjunction with the IDT switch device's Data Sheet.

Board Material

Printed Circuit Board (PCB) dielectric construction material controls how much noise and cross-talk is contributed from the fast switching I/O signals. This dielectric material can be assigned a dielectric constant (ε r), which affects the impedance of a transmission line, and signals can propagate faster in materials that have a lower ε r.

Proper dielectric material selection enables the PCB designer to minimize the dielectric loss because at frequencies above 1 GHz, dielectric loss is dominant compared to conductor loss. The dielectric loss is dependent on the loss tangent/dissipation factor for a given dielectric material. Smaller loss tangent values offer lower high-frequency attenuation to the high-speed signals. The dielectric constant and the loss tangent information for the various dielectric materials typically used in the PCB design are shown in *Figure 1.*.

Performance	Name	Dielectric Constant (Dk)	Loss Tangent/ Dissipation Factor (Df)	Cost
Low	Standard FR4	4.1 – 4.4	0.019 – 0.024	Low
	Nelco N4000 - 6	4.0	0.022 @ 2.5GHz	
	Isola FR 370 HR	4.04	0.021 @ 2GHz	
Medium	GETEK	3.5	0.010 @ 10GHz	Medium
	Isola FR 408	3.75	0.012 @ 10GHz	
	Nelco 4000 – 13 EP	3.6	0.009 @ 10GHz	
	Nelco 4000 – 13 EPSI	3.2	0.008 @ 10GHz	
High	Rogers RO4350B	3.48	0.0037 @ 10GHz	High
	Arlon 25N	3.38	0.0025 @ 10GHz	

Figure 1. Dielectric materials used in PCB design

The most widely used dielectric material for PCBs is FR-4, a glass laminate with epoxy resin that meets a wide variety of processing conditions. It is suggested to work closely with the PCB vendor to design the high-speed channels with the correct impedance and meeting the loss targets.

Notes

Layers Stackup

Multi-layer boards are a must in both daughter board and backplane design. The multiple metal layers facilitate high connection density, minimum crosstalk, and EMI performance. These factors are keys to achieving good signal integrity for all the signal interconnections. When determining a layer stackup, it is suggested to consider all board layout issues (e.g., simultaneous switching output noise (SSN), decoupling, trace layout, vias, etc.). Ideally, all signal layers should be separated from each other by ground or power planes (metal layers). This minimizes crosstalk and provides homogeneous transmission lines, with properly controlled characteristic impedance, between devices and other board components. Best performance is obtained when using dedicated ground and power plane layers that are continuous across the entire board area. When it is not feasible to provide ground or power planes between signal layers, great care must be taken to ensure signal line coupling is minimized. Orthogonal routing on adjacent signal layers minimizes coupling and should be used.

The stackup shown in *Figure 2.* will be used to demonstrate some parameters that affect the impedance of the board while designing transmission lines. It is shown in the eight-layer stackup that 12mil of trace on the top layer will achieve around 53.4ohms of impedance when separated by a dielectric of 7mils from the plane. It is also shown that 7mil of trace on an internal signal layer will achieve 50.1ohms of impedance when separated by 8mils of dielectric on both sides. These parameters are taken from the Hyperlynx Signal Integrity Line SIM tool. During the design of differential transmission lines, both traces have to be coupled, weakly coupled or strongly coupled. Coupling will depend on the distance between two traces forming a differential transmission line.

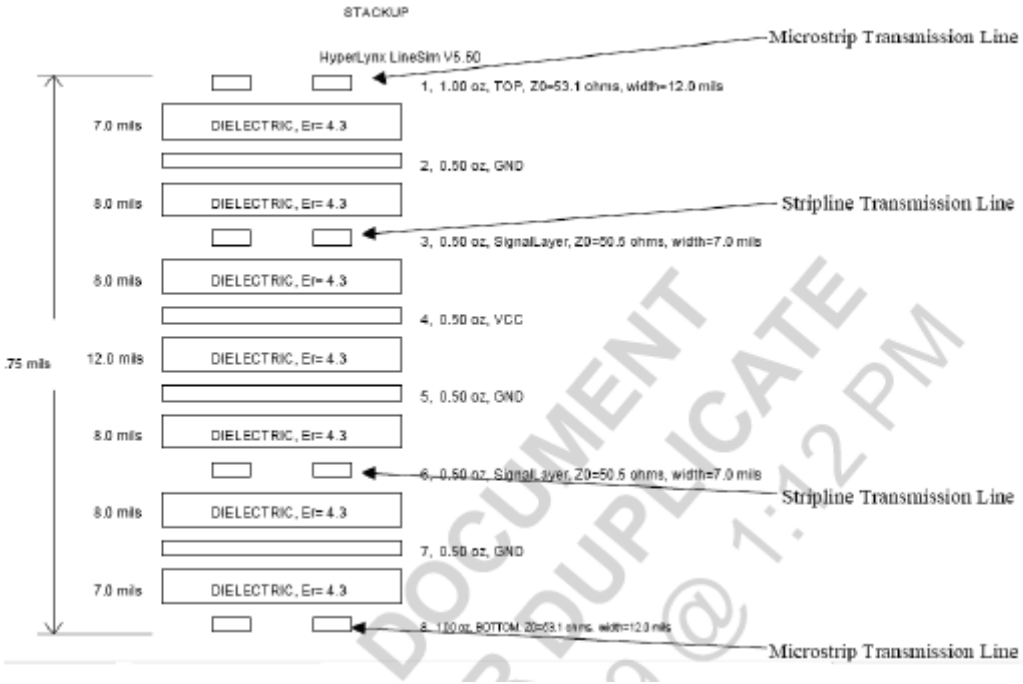

Figure 2. Board Stackup for Eight Layers

Notes

Differential Pair Trace Design

Transmission Line

The high speed interconnects of S-RIO SerDes are differential signals so these traces should be designed as a differential pair. These signals have very fast rise / fall times on the order of pico seconds, so these interconnects should be treated as transmission lines rather than simple wire connections. The characteristics of transmission lines determine the layout practice. One of the fundamental properties of a transmission line (a mathematical model for a trace on a PCB with power/ground planes) is characteristic impedance, Zo.

Transmission line effect and modeling is another factor to affect signal performance and noise separation. Transmission line is a trace, and has a distributed mixture of resistance (R), inductance (L), capacitance (C) and conductance (G). There are two types of transmission line layouts: Microstrip and Stripline. *Figure 3.* shows the two types of transmission line layouts.

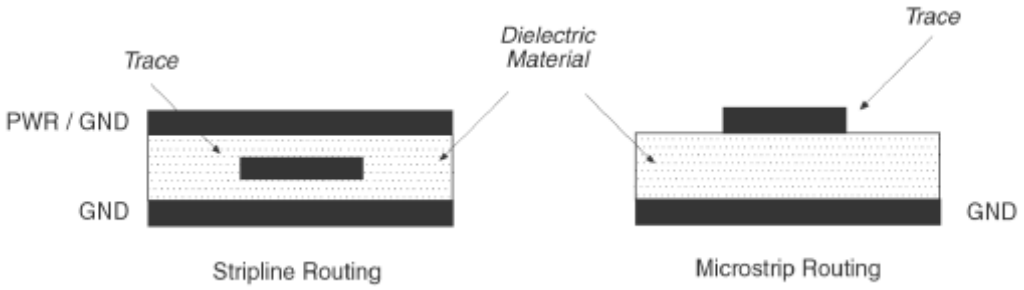

Figure 3. Stripline & Microstrip Signal Routing

The impedance requirement of the Serial RapidIO interface is **100 ohms differentia**l. 100 ohm characteristic impedance has become an industry standard value for differential signaling. This impedance level lends itself well to PCB structures and other components designs where controlled transmission line impedance must be provided. A 100 ohm differential line can be constructed with two 50 ohm single-ended lines of equal length.

Microstrip

A differential circuit routed on an outside layer of the PCB with a reference plane below it, constitutes a microstrip layout. *Figure 4.* shows the construction of the differential microstrip topology. Equations in *Figure 5.* are used to calculate the impedance of differential microstrip trace pair.

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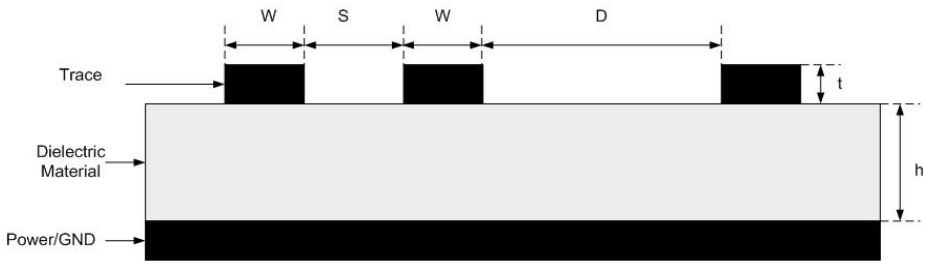


Microstrip Transmission Line Layout

W = Width of trace
t = Thickness of trace
h = Height between trace and reference plane
S = Space between two traces of a differential pair
D = Space between two adjacent differential pairs

Figure 4. Differential Microstrip Construction

Notes

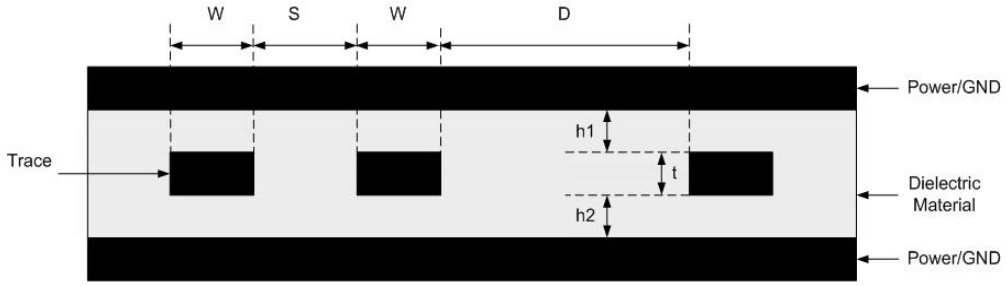
$$Z_o = \frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67(0.8w+t)}\right] ohms$$

$$Z_{diff} \cong 2Z_o\left(1 - 0.48e^{-0.96\frac{s}{h}}\right) ohms$$

Figure 5. Equations for the Differential Microstrip Impedance (in Ohms)

Stripline

A differential circuit routed on an inside layer of the PCB with two low-voltage reference planes (such as, power and / or GND) constitutes a stripline layout. *Figure 6.* shows the construction of the differential stripline topology. Equations in *Figure 7.* are used to calculate the impedance of a stripline trace pair.



Stripline Transmission Line Layout

W = Width of trace
t = Thickness of trace
S = Space between two traces of a differential pair
D = Space between two adjacent differential pairs

Figure 6. Edge Coupled Differential Stripline Construction

$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \times \ln\left(\frac{1.9(2(h1 + h2) + t)}{0.67\,\pi(0.8w + t)}\right)$$

$$Zdiff = 2 \times Zo\left(1 - 0.374\, e^{-2.9\left[\frac{s}{h1+h2}\right]}\right)$$

Figure 7. Equations for Differential Stripline Impedance (in Ohms)

High-speed signal applications perform best with stripline board configurations rather than microstrip configurations. The stripline board configuration provides better protection from crosstalk and has significantly reduced EMI.

Notes

Tracking Topologies

The tracking topologies required to maintain a consistent differential impedance of 100 ohms to the signal placed on the transmission line are limited to Stripline and Microstrip types. The designer must decide whether the signaling must be moved to an outer layer of the board using a Microstrip topology, or if the signaling may be placed on an inner layer as stripline where shielding by ground and power planes above and below is possible.

- *The edge side coupled differential pair geometry, also known as side-to-side, designed for Microstrip or Stripline configurations are suggested.*
  - Edge-coupled microstrip or stripline will allow the thinnest total PCB thickness while optimizing the via stub length
  - High-differential impedance is easily achievable
  - Control length matching and routing through fine pitch holes
- *Tight coupling is suggested. It gives higher interconnect density, allows fewer layers, and provides better noise immunity, but requires a certain dielectric thickness for impedance matching. Looser coupling is acceptable if density is not an important driver of a signal layout.*
- *The two traces should be identical. This means each trace of the differential pair should have the same cross sectional dimensions and must be surrounded by the same type or types of dielectric materials. The spacing between the two traces should also be the same for the entire length of the trace.*
- *Skew or time delay between the two traces of the differential pair should be zero.*
  - In order to prevent consuming received eye margin, +/- track skew of a lane should be constrained to a maximum of 10ps.
  - Lane-to-lane skew at the input to the receiver shall not exceed 11ns.
- *Instead of 90^O bends, use mitered 45^O bends. Mitered 45^O bends reduce reflection on the signal by minimizing impedance discontinuities.*
- *Do not route pairs on adjacent layers co-parallel in broadside topology. Instead, use orthogonal routing on signal on different layers to avoid crosstalk. Figure 8. shows an example.*

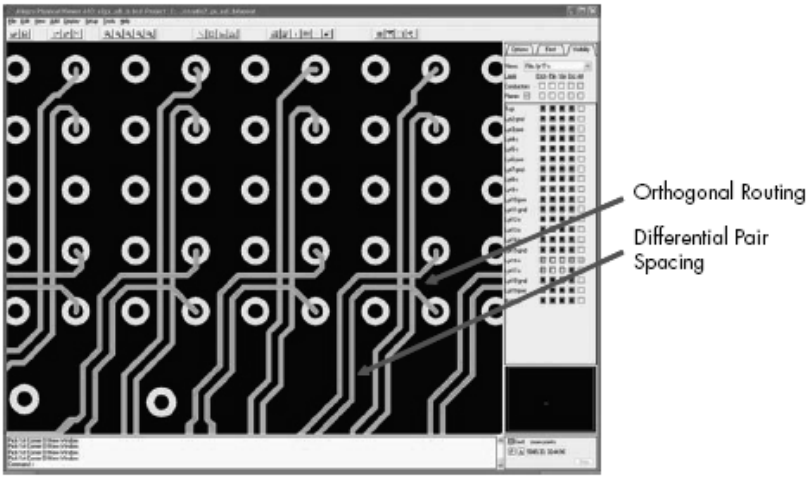


Figure 8. Layout Example of How to Avoid Crosstalk

- *Make sure D (Space between two adjacent differential pairs) > 3S (Space between two trace of a differential pair) to minimize the crosstalk between the two differential pairs.*
- *Widen spacing between signal lines as much as routing restrictions will allow. Try not to bring traces closer than three times the dielectric height (S > 3h).*

Note: please see *Figure 4.* for the definition for "D", "S" and "h".

Notes

Via

Vias generally provide two purposes. One is used for mounting a through-hole component on a PCB. The second is to interconnect traces on different metal layers. Electrically, vias are often modeled as having an inductive and capacitive parasitic value. As more designs move toward high-speed serial links with pico-seconds edge rates, any impedance discontinuity in the channel can adversely affect signal quality. One commonly overlooked source of channel discontinuity is the signal via. Vias can add jitter and reduce eye openings that can cause data misinterpretation by the receiver.

Via Construction and Lumped pi Model

Figure 9. shows via construction. Vias can appear as capacitive and/or inductive discontinuities. These capacitive and inductive parasitics contribute to the degradation of the signal as it passes through the vias. *Figure 10.* shows a simple lumped LC pi model to illustrate via capacitance and inductance effects. Although this model is only applicable if the delay through the via is less than 1/10th of the signal rise time, it is still useful to understand its capacitance and inductance effects.

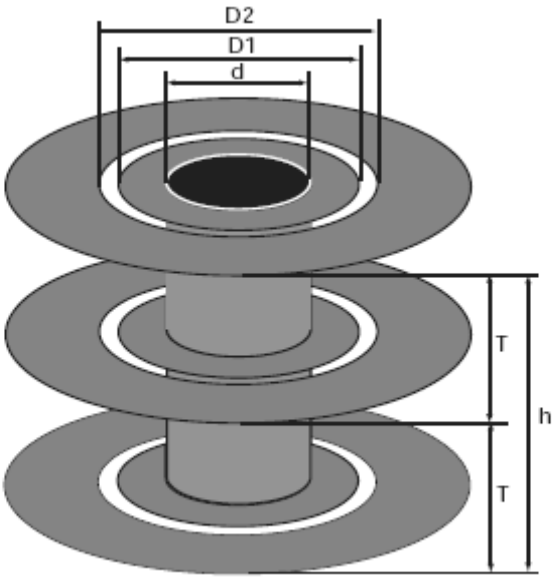


Figure 9. Via Construction

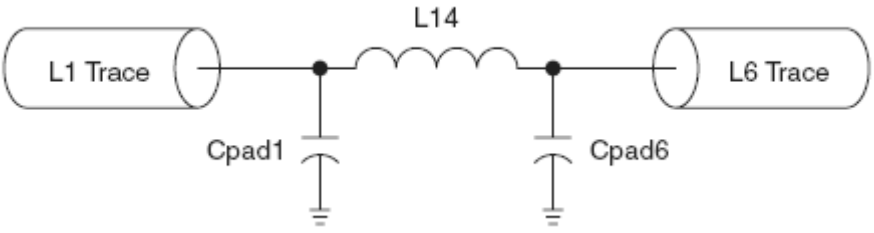


Figure 10. Lumped pi Model of a Via

Figure 11. shows the empirical formula for capacitance and inductance of vias when vias are modeled as a lumped LC pi model. Here ε_r is the relative dielectric constant, D1 is the diameter of the via pad, D2 is the diameter of the anti-pad, T is the thickness of the PCB, h is the via length, and d is the via barrel diameter.

Notes

$$Cvia \approx \frac{1.41\varepsilon_r D_1 T}{D_2 - D_1}\text{pF}$$

$$Lvia \approx 5.08h\left[\ln\left(\frac{4h}{d}\right) + 1\right]\text{nH}$$

Figure 11. Capacitance and Inductance Equations of via

Via capacitance can be minimized by making the capacitance of via pad small and increasing the diameter of via anti-pad. Similarly, minimizing the length of via barrel and placing a return via close to the signal via will reduce the via loop inductance.

Two cases (signal through a via and Signal across a via) are shown in *Figure 12.* A through via (without any stub) is recommended wherever necessary because the stub offers a capacitive discontinuity to any high-speed signal.

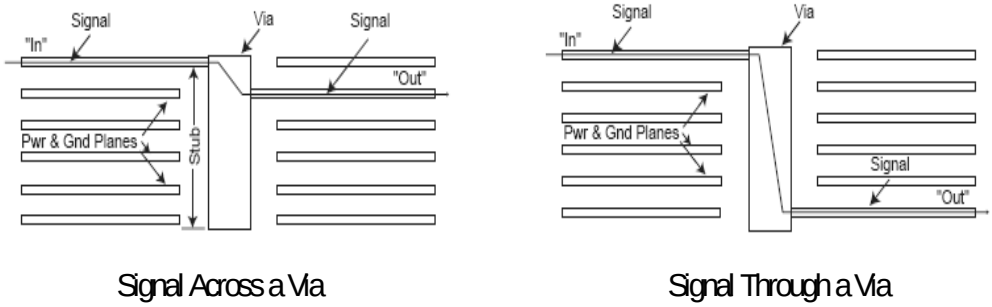


Figure 12. Signal Across a Via & Through a Via

Basic Rules for differential Vias

- *Keep vias in the signal path down to a minimum.*
- *When routing vias, try to ensure that the vias do not carry any stub especially for high-speed signals.*
- *The use of buried and blind vias is recommended because in both cases the signal travels through via without any stub.*
- *Remove all non-functional pads (NFPs).*
- *Increase vias anti-pad diameter (clearance hole).*
- *If stubs cannot be avoided, it can be removed by back-drilling or counter-boring the backside of the PCB with a slightly oversized drill bit to remove the parasitic stub. This method demands a cost premium over using standard vias because it requires an additional step in manufacturing the PCB.*
- *Add adjacent ground vias next to each signal via to provide a better AC return path.*
- *Place via adjacent to the capacitor pad. Use wide, short traces between the via and capacitor pads.*

Notes

S-RIO Receiver DC Blocking Capacitors

The Serial RapidIO high-speed serial lines are differential CML output voltage swings and these are designed to be AC-coupled. The high-speed serial connections are shown in *Figure 13.*

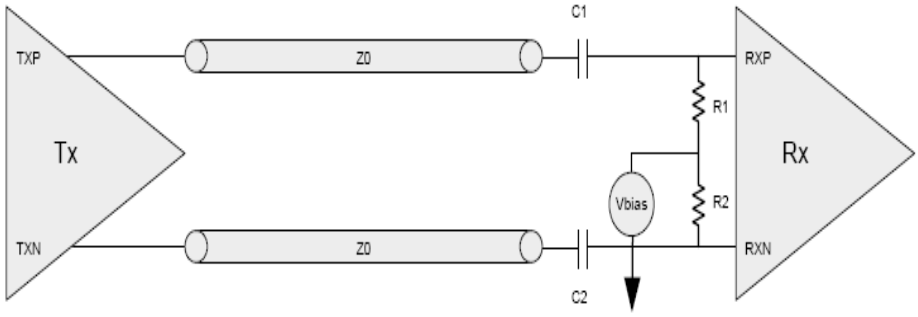


Figure 13. AC-Coupled Differential Interconnect

An inline capacitor C1 and C2 at each input of the receiver provides AC-coupling and a DC-block. Thus, any DC bias differential between the two devices on the link is negated. (Note that VBIAS is the internal bias voltage of the device's receiver. R1 and R2 are 50 Ohms each. They are embedded in IDT switch already). The IDT recommended capacitor value is 0.1uF ceramic in 0402 size (or smaller size). The AC coupling capacitors should be symmetrically placed near the receiver of the device or connector to minimize discontinuity effects. Do not place the capacitors along the signal trace at a (λ /4) increment from the driver in order to avoid possible standing wave effects Note S-RIO 2.0 specification allows the optional DC coupling for the Level II (5G and 6.25G) link, however IDT80HSPS1616 do not support this and only supports AC coupling.

Power Distribution

A system can distribute power throughout the PCB with either power planes or a power bus network. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains VDD and distributes it equally to all devices while providing very high current-sink capability, noise protection, and shielding for the logic signals on the PCB. It is recommended to use low impedance supply planes to distribute power

Good layout and bypass techniques to filter the IC's power supply have a significant impact upon signal quality. The power distribution impacts system noise. The power supply noise is of major concern as it will couple into the PLL circuits of the transceivers, thereby increasing jitter generation in the transmitter and reducing jitter tolerance in the receiver. The IDT S-RIO switch is a high speed device with both digital and analog components in its design. The correct treatment of the power rails, plane assignments, and decoupling is important to maximize IDT S-RIO switch performance. The largest indicator of poor performance on the Serial RapidIO interfaces is the presence of jitter. The die, I/O, and package designs have all been optimized to provide jitter performance exceeding the limits required by the Serial RapidIO specifications. The guidelines provided below will assist the user in achieving a board layout that will provide the best performance possible

IDT80HSPS1616 switch has the following types of power supply pins:

1)VDD3 (3.3V): digital interface power.

2)VDD (1.0V): digital core power.

3)VDDA (1.0V): analog power.

4)VDDS (1.0V): Analog power for SerDes and RX pairs.

Notes

5)VDDT (1.2V): Analog power for TX pairs.

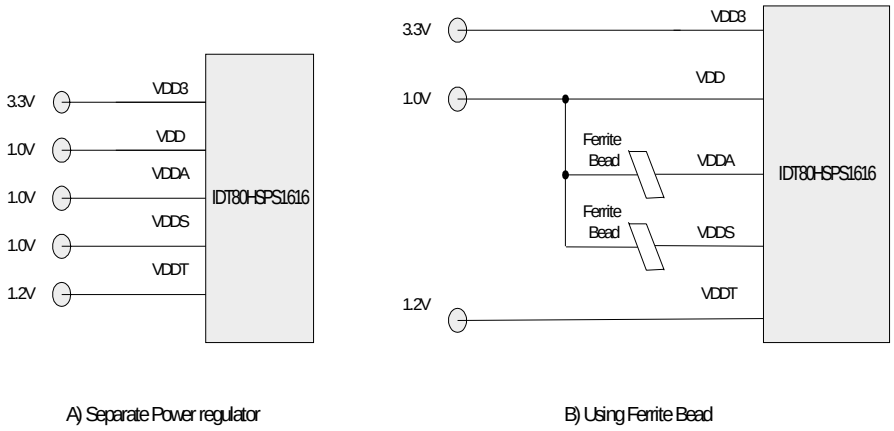


Figure 14. Board Power Supply Diagram

- *It is suggested all voltage can be derived from separate voltage regulators.*
- *VDD, VDDA, VDDS can be derived from the same voltage source with appropriate bypass capacitors and a ferrite bead. A ferrite bead can be used to attenuate the power noise and improve the analog circuit performance in a noisy environment. It is suggested to select Ferrite bead with 1Amp current, impedance of 50~120 ohm at 100MHz and low DC resistance.*
- *Note VDDS & VDDA may be tied to a common power plane.*
- *Note VDD (core, digital supply) & VDDT should have its own supply and plane.*

Decoupling Requirement

Proper decoupling is critical in high-speed board designs. Select the right decoupling capacitors, power and ground plane stack-up, and voltage regulators to minimize noise. Decoupling is one of the most important aspects of board design. It is critical to have a proper decoupling mechanism in place. With the right combination of power and GND planes, decoupling capacitors and voltage-regulator modules will provide decoupling over all frequencies.

To filter power supply noise, use a non-resonant, surface-mount ferrite bead large enough to handle the current in series with the power supply. Place a 10 to 100 uF bypass capacitor next to the ferrite bead. (If proper termination, layout, and filtering sufficiently eliminate noise, a ferrite bead may not be necessary.) The ferrite bead acts as a short for high-frequency noise coming from the VDD source. Any low frequency noise is filtered by a large 10uF capacitor after the ferrite bead. Usually, elements on the PCB add high-frequency noise to the power plane. *Figure 15.* is an example of a power noise filter

Notes

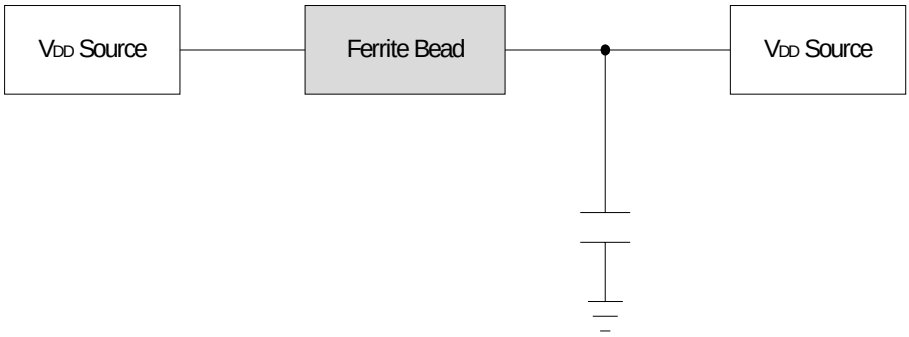


Figure 15. Power Noise Filtering Example

Voltage	Usage	Acronym	Component Requirement			
3.3V	Digital interface power	VDD3	3 x 0.1uF	3 x 0.01uF		3 x 220uF
1.0V	Digital core power	VDD	8 x 0.1uF	12 x 0.01uF	8 x 1nF	4 x 220uF
1.0V	AnalogPower	VDDA	8 x 0.1uF	8 x 0.01uF	8 x 1nF	3 x 220uF
1.0V	Analog power for SerDes and RX pairs	VDDS	8 x 0.1uF	8 x 0.01uF		3 x 220uF
1.2V	Analog power for TX pairs	VDDT	8 x 0.1uF	8 x 0.01uF		3 x 220uF

Table 1 Decoupling Capacitor Quantities and Values Recommended for IDT80HSPS1616

Table 1 shows the recommended decoupling capacitor for IDT80HSPS1616. The capacitors should be selected with the smallest surface mount body that the applied voltage permits in order to minimize the body inductance. Ceramic X7R type (0402 or smaller size) are suggested for all of the values listed. The larger value capacitors should be low ESR type and placed closely to the power supply. To optimize the effectiveness of decoupling capacitors, surface-mounted capacitors mounted on the bottom side of the PCB keeps the parasitic effects to a minimum. Placing capacitors directly underneath the BGA package will improve the high frequency response of very small value capacitors.

It is suggested to use separate vias for each capacitor and via sharing should not be used in board design for IDT S-RIO switches. Breakout vias for the decoupling capacitors should be kept as close together as possible. The trace connecting the pad to the via should also be kept as short as possible with a maximum length of 50mils. *Figure 16.* shows several recommended decoupling capacitor pad design.

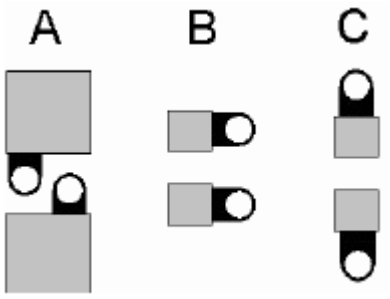


Figure 16. Recommended Decoupling Capacitor Pad Designs

Notes

It is recommended to follow some design guidelines to reduce ground bounce:

- *Use a bigger via size to connect the capacitor pad to the power and ground plane to minimize the inductance in decoupling capacitors.*
- *Place the power and ground via as close to each other as possible to increase the mutual inductive coupling between them.*
- *Traces stretching from power pins to a power plane (or island, or a decoupling capacitor) must be as wide and as short as possible.*

Clock Design and Consideration

IDT S-RIO switch reference clock is a CML based differential input. Most clock chips are LVPECL or LVDS based differential outputs. Thus clock reference must be terminated correctly. Following *Figure 17.* shows how to use the AC-coupling with LVPECL to CML receiver and *Figure 18.* shows how to use the AC-coupling with LVDS to CML receiver.

LVPECL to CML termination

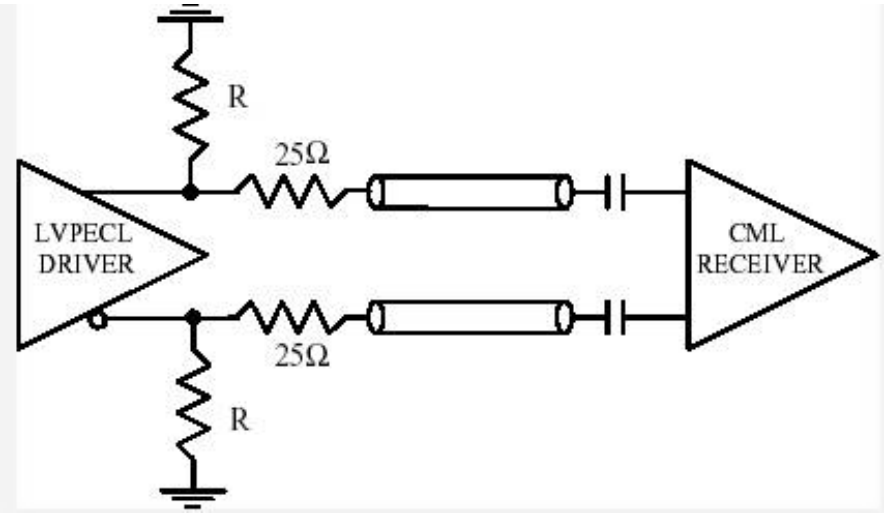


Figure 17. LVPECL to CML signal termination

- *AC-Coupling and a 0.1uF ceramic capacitor in 0402 size is suggested.*
- *Two pull-down resistors are needed to dissipate the LVPECL output emitter current. And the value can be about 142ohm ~ 200ohm.*
- *The 25 Ohm serial resistor is optional when the LVPECL Swing is beyond the CML accepted.*
- *Place resistors near the transmitter side and place decoupling caps near the receiver.*
- *If possible do not use via in clock transmission lines and shorten the signal length.*

Notes

LVDS to CML termination

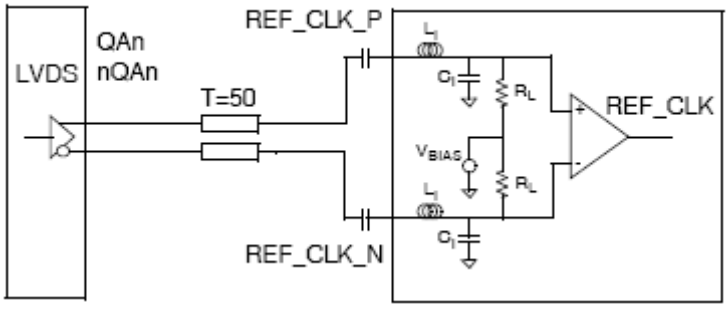


Figure 18. LVDS to CML signal termination

IDT Recommended Clock chip solution

IDT suggest ICS841N254i clock synthesizer chip to generate reference clock for IDT80HSPS1616 S-RIO switch. Please refer to "ICS841N254i datasheet".

High Speed Serial I/O and Layout Consideration

Proper PCB layout is important in order to minimize parasitic capacitance and inductance. When implementing a high speed serial communications link, the importance of layout cannot be overstressed. However, following general simple-to-use guidelines will increase the chances of success and prove easier than most designers anticipate. Before we also talk about some rules related with routing and vias. Following is an conclusion for basic rules:

- *Careful placement of components and the use of passives on both the top and bottom side will generally ensure optimal layout.*
- *A solid ground plane and power plane are quite useful in distributing clean power and providing buried capacitance with no inductance which is essential for the high speed designs.*
- *The board design should be a controlled impedance board design for the high-speed signals of SerDes. The high-speed signal traces should be designed for desired differential impedance. The design engineer should work very closely with the fabrication house to get the board material thickness, so that he can use these parameters to decide on the thickness and width of traces to get the desired impedance on the board.*
- *Keep traces as short as possible. Initial component placement must be carefully considered. Eliminate ALL stubs.*
- *For the receiver, the trace from the BGA pad to the capacitor pad must be on the top layer. On the other side of the capacitor, it is permissible to via to another layer.*
- *The trace widths and separation should be altered based on the board stackup to meet the 100 Ohm differential impedance requirement.*
- *An 0402 or smaller size, 0.1uf capacitor is recommended for AC coupling of the data lines.*
- *While routing the differential pairs, keep the trace length identical between the two traces.*
- *Reduce, if not eliminate, the number of vias to minimize impedance discontinuities. Keep vias away from traces by 3 times the trace width as minimum.*
- *Use surface mounted components for lower lead inductance and capacitance. Smaller form factor components are*
- *Keep high-speed signal traces far from other signals which might capacitively couple noise into the signals. A good rule of thumb is that "far" means tens times the width of the trace.*
- *Do not route the digital signals from other circuits across the area of the transmitter and receiver.*

Notes

IDT strongly recommends modeling the high-speed channel and simulate with available HSPICE and IBIS models of IDT device prior to committing to PCB design. The HSPICE model is provided for simulating high-speed signals where as the IBIS model is used for the slower speed signals. The Applications group is available to assist with simulation and/or review of the schematic to achieve first time success for the PCB design. Please contact IDT Applications group for additional information or support of these models

Revision History

8/6/2009: Rev-A

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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