WAN PLL

IDT82V3280

Version 7
June 22, 2015

6024 Silver Creek Valley Road, San Jose, CA 95138
Telephone: (800) 345-7015 • TWX: 910-338-2070 • FAX: (408) 284-2775
Printed in U.S.A.

DISCLAIMER

Integrated Device Technology, Inc. reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance and to supply the best possible product. IDT does not assume any responsibility for use of any circuitry described other than the circuitry embodied in an IDT product. The Company makes no representations that circuitry described herein is free from patent infringement or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent, patent rights or other rights, of Integrated Device Technology, Inc.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any components of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

© 2019 Renesas Electronics Corporation

Table of Contents

List of Tables

List of Figures

FEATURES

HIGHLIGHTS

- The first single PLL chip:
  - Features 0.5 mHz to 560 Hz bandwidth
  - Exceeds GR-253-CORE (OC-12) and ITU-T G.813 (STM-16/ Option I) jitter generation requirements
  - Provides node clocks for Cellular and WLL base-station (GSM and 3G networks)
  - Provides clocks for DSL access concentrators (DSLAM), especially for Japan TCM-ISDN network timing based ADSL equipments

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 2, 3E, 3, SMC, 4E and 4 clocks
- Employs DPLL and APLL to feature excellent jitter performance and minimize the number of the external components
- Integrates T0 DPLL and T4 DPLL; T4 DPLL locks independently or locks to T0 DPLL
- Supports Forced or Automatic operating mode switch controlled by an internal state machine; the primary operating modes are Free-Run, Locked and Holdover
- Supports programmable DPLL bandwidth (0.5 mHz to 560 Hz in 19 steps) and damping factor (1.2 to 20 in 5 steps)
- Supports $1.1X10^{-5}$ ppm absolute holdover accuracy and $4.4X10^{-8}$ ppm instantaneous holdover accuracy
- Supports PBO to minimize phase transients on T0 DPLL output to be no more than 0.61 ns
- Supports phase absorption when phase-time changes on T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds
- Supports programmable input-to-output phase offset adjustment
- Limits the phase and frequency offset of the outputs
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing
- Provides a 2 kHz, 4 kHz or 8 kHz frame sync input signal, and a 2 kHz and an 8 kHz frame sync output signals
- Provides 14 input clocks whose frequency cover from 2 kHz to 622.08 MHz
- Provides 9 output clocks whose frequency cover from 1 Hz to 622.08 MHz
- Provides output clocks for BITS, GPS, 3G, GSM, etc.
- Supports AMI, PECL/LVDS and CMOS input/output technologies
- Supports master clock calibration
- Supports Master/Slave application (two chips used together) to enable system protection against single chip failure
- Meets Telcordia GR-1244-CORE, GR-253-CORE, GR-1377-CORE, ITU-T G.812, ITU-T G.813 and ITU-T G.783 criteria

OTHER FEATURES

- Multiple microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 100-pin TQFP package, Green package options available

APPLICATIONS

- BITS / SSU
- SMC / SEC (SONET / SDH)
- DWDM cross-connect and transmission equipments
- Central Office Timing Source and Distribution
- Core and access IP switches / routers
- Gigabit and Terabit IP switches / routers
- IP and ATM core switches and access equipments
- Cellular and WLL base-station node clocks
- Broadband and multi-service access equipments
- Any other telecom equipments that need synchronous equipment system timing

DESCRIPTION

The IDT82V3280 is an integrated, single-chip solution for the Synchronous Equipment Timing Source for Stratum 2, 3E, 3, SMC, 4E and 4 clocks in SONET / SDH equipments, DWDM and Wireless base station, such as GSM, 3G, DSL concentrator, Router and Access Network applications.

The device supports three types of input clock sources: recovered clock from STM-N or OC-n, PDH network synchronization timing and external synchronization reference timing.

Based on ITU-T G.783 and Telcordia GR-253-CORE, the device consists of T0 and T4 paths. The T0 path is a high quality and highly configurable path to provide system clock for node timing synchronization within a SONET / SDH network. The T4 path is simpler and less configurable for equipment synchronization. The T4 path locks independently from the T0 path or locks to the T0 path.

An input clock is automatically or manually selected for T0 and T4 each for DPLL locking. Both the T0 and T4 paths support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

If the DPLL outputs are processed by T0/T4 APLL, the outputs of the device will be in a better jitter/wander performance.

The device provides programmable DPLL bandwidths: 0.5 mHz to 560 Hz in 19 steps and damping factors: 1.2 to 20 in 5 steps. Different settings cover all SONET / SDH clock synchronization requirements.

A high stable input is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ±741 ppm.

All the read/write registers are accessed through a microprocessor interface. The device supports five microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial.

In general, the device can be used in Master/Slave application. In this application, two devices should be used together to enable system protection against single chip failure. See Chapter 4 Typical Application for details.

FUNCTIONAL BLOCK DIAGRAM

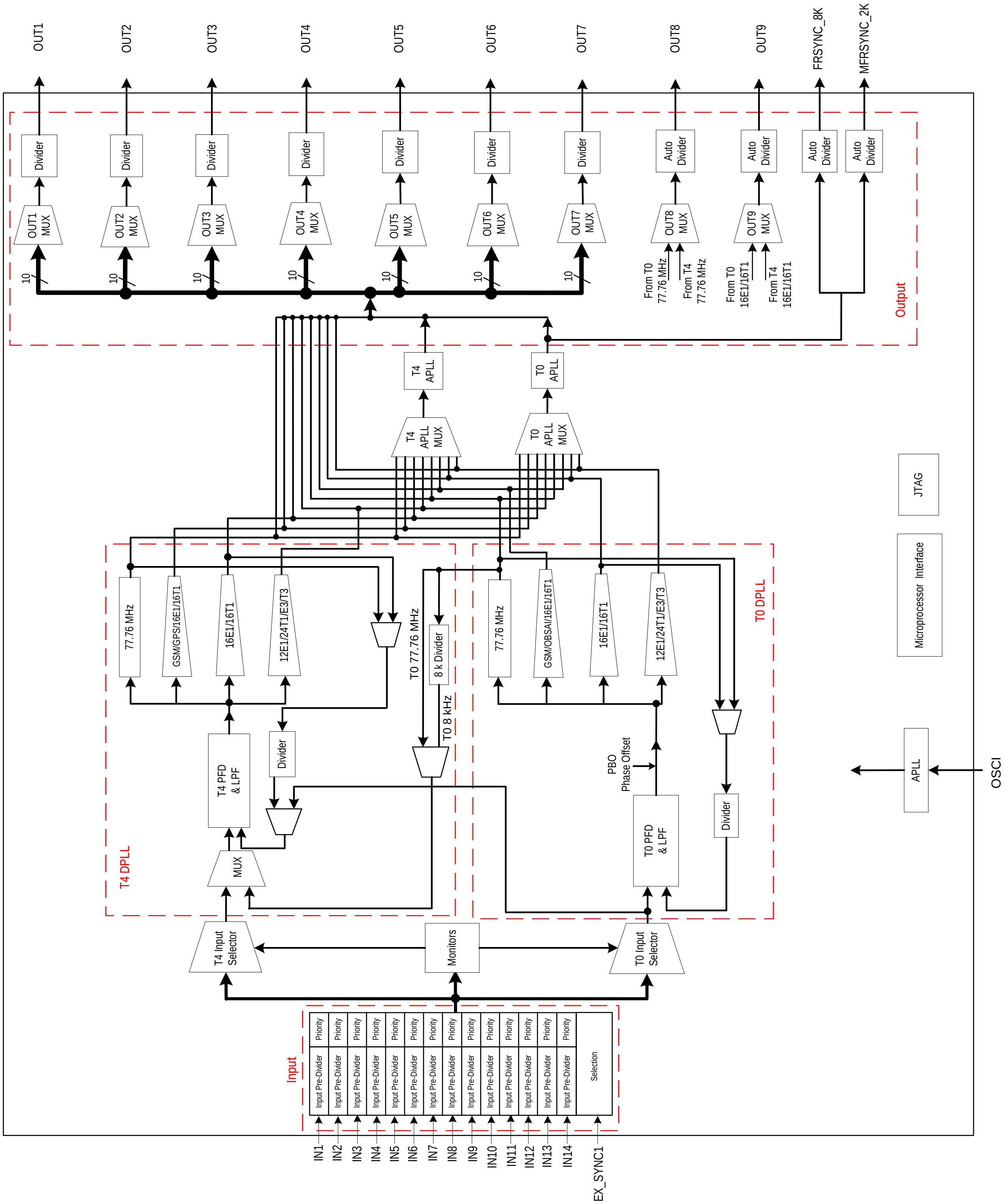


Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

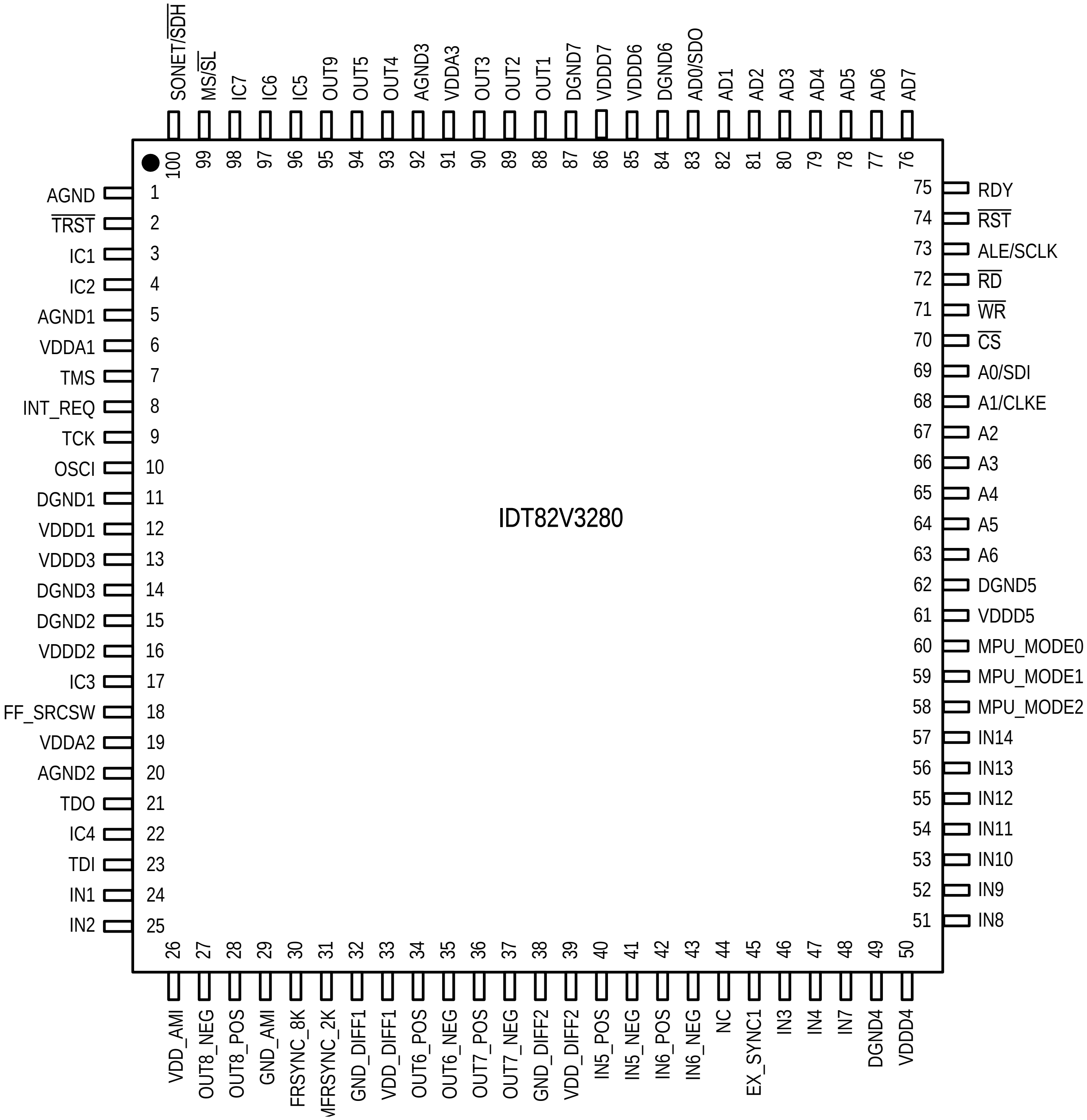


Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Name	Pin No.	I/O	Type	Description [1]
Global Control Signal				
OSCI	10	I	CMOS	OSCI: Crystal Oscillator Master Clock A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.
FF_SRCSW	18	I pull-down	CMOS	FF_SRCSW: External Fast Selection Enable During reset, this pin determines the default value of the EXT_SW bit (b4, 0BH) [2]. The EXT_SW bit determines whether the External Fast Selection is enabled. High: The default value of the EXT_SW bit (b4, 0BH) is ‘1’ (External Fast selection is enabled); Low: The default value of the EXT_SW bit (b4, 0BH) is ‘0’ (External Fast selection is disabled). After reset, this pin selects an input clock pair for the T0 DPLL if the External Fast selection is enabled: High: Pair IN3 / IN5 is selected. Low: Pair IN4 / IN6 is selected. After reset, the input on this pin takes no effect if the External Fast selection is disabled.
MS/$\overline{\text{SL}}$	99	I pull-up	CMOS	MS/$\overline{\textbf{SL}}$: Master / Slave Selection This pin, together with the MS_SL_CTRL bit (b0, 13H), controls whether the device is configured as the Master or as the Slave. Refer to Chapter 3.14 Master / Slave Configuration for details. The signal level on this pin is reflected by the MASTER_SLAVE bit (b1, 09H).
SONET/$\overline{\text{SDH}}$	100	I pull-down	CMOS	SONET/$\overline{\textbf{SDH}}$: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is ‘1’ (SONET); Low: The default value of the IN_SONET_SDH bit is ‘0’ (SDH). After reset, the value on this pin takes no effect.
$\overline{\text{RST}}$	74	I pull-up	CMOS	$\overline{\textbf{RST}}$: Reset A low pulse of at least 50 µs on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).
Frame Synchronization Input Signal				
EX_SYNC1	45	I pull-down	CMOS	EX_SYNC1: External Sync Input 1 A 2 kHz, 4 kHz or 8 kHz signal is input on this pin.
Input Clock				
IN1	24	I	AMI	IN1: Input Clock 1 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin.
IN2	25	I	AMI	IN2: Input Clock 2 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin.
IN3	46	I pull-down	CMOS	IN3: Input Clock 3 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN4	47	I pull-down	CMOS	IN4: Input Clock 4 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
IN5_POS IN5_NEG	40 41	I	PECL/LVDS	IN5_POS / IN5_NEG: Positive / Negative Input Clock 5 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 9.3.3.3 Single-Ended Input for Differential Input.
IN6_POS IN6_NEG	42 43	I	PECL/LVDS	IN6_POS / IN6_NEG: Positive / Negative Input Clock 6 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 9.3.3.3 Single-Ended Input for Differential Input.
IN7	48	I pull-down	CMOS	IN7: Input Clock 7 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN8	51	I pull-down	CMOS	IN8: Input Clock 8 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN9	52	I pull-down	CMOS	IN9: Input Clock 9 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN10	53	I pull-down	CMOS	IN10: Input Clock 10 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN11	54	I pull-down	CMOS	IN11: Input Clock 11 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin. In Slave operation, the frequency of the T0 selected input clock IN11 is recommended to be 6.48 MHz.
IN12	55	I pull-down	CMOS	IN12: Input Clock 12 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN13	56	I pull-down	CMOS	IN13: Input Clock 13 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
IN14	57	I pull-down	CMOS	IN14: Input Clock 14 A 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is input on this pin.
Output Frame Synchronization Signal				
FRSYNC_8K	30	O	CMOS	FRSYNC_8K: 8 kHz Frame Sync Output An 8 kHz signal is output on this pin.
MFRSYNC_2K	31	O	CMOS	MFRSYNC_2K: 2 kHz Multiframe Sync Output A 2 kHz signal is output on this pin.
Output Clock				
OUT1	88	O	CMOS	OUT1: Output Clock 1 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
OUT2	89	O	CMOS	OUT2: Output Clock 2 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT3	90	O	CMOS	OUT3: Output Clock 3 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT4	93	O	CMOS	OUT4: Output Clock 4 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT5	94	O	CMOS	OUT5: Output Clock 5 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz or 155.52 MHz clock is output on this pin.
OUT6_POS OUT6_NEG	34 35	O	PECL/LVDS	OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially output on this pair of pins.
OUT7_POS OUT7_NEG	36 37	O	PECL/LVDS	OUT7_POS / OUT7_NEG: Positive / Negative Output Clock 7 A 1 Hz, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz or 622.08 MHz clock is differentially output on this pair of pins.
OUT8_POS OUT8_NEG	28 27	O	AMI	OUT8_POS / OUT8_NEG: Positive / Negative Output Clock 8 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is differentially output on this pair of pins.
OUT9	95	O	CMOS	OUT9: Output Clock 9 A 1.544 MHz (SONET) / 2.048 MHz (SDH) BITS/SSU clock is output on this pin.
Microprocessor Interface				
$\overline{\text{CS}}$	70	I pull-up	CMOS	$\overline{\text{CS}}$: Chip Selection A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over.
INT_REQ	8	O	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).
MPU_MODE0 MPU_MODE1 MPU_MODE2	60 59 58	I pull-down	CMOS	MPU_MODE[2:0]: Microprocessor Interface Mode Selection The device supports five microprocessor interface modes: EPROM, Multiplexed, Intel, Motorola and Serial. During reset, these pins determine the default value of the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH) as follows: 001 (EPROM mode); 010 (Multiplexed mode); 011 (Intel mode); 100 (Motorola mode); 101 (Serial mode); 110 - 111 (Reserved). After reset, these pins are general purpose inputs. The microprocessor interface mode is selected by the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH). The value of these pins is always reflected by the MPU_PIN_STS[2:0] bits (b2~0, 02H).

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
A0 / SDI	69	I pull-down	CMOS	A[6:0]: Address Bus In ERPOM, Intel and Motorola modes, these pins are the address bus of the microprocessor interface. SDI: Serial Data Input In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. CLKE: SCLK Active Edge Selection In Serial mode, this pin selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge. In Multiplexed mode, A0/SDI, A1/CLKE and A[6:2] pins should be connected to ground. In Serial mode, A[6:2] pins should be connected to ground.
A1 / CLKE	68			
A2	67			
A3	66			
A4	65			
A5	64			
A6	63			
AD0 / SDO	83	I/O pull-down	CMOS	AD[7:0]: Address / Data Bus In EPROM, Intel and Motorola modes, these pins are the bi-directional data bus of the microprocessor interface. In Multiplexed mode, these pins are the bi-directional address/data bus of the microprocessor interface. SDO: Serial Data Output In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. In Serial mode, AD[7:1] pins should be connected to ground.
AD1	82			
AD2	81			
AD3	80			
AD4	79			
AD5	78			
AD6	77			
AD7	76			
$\overline{\text{WR}}$	71	I pull-up	CMOS	$\overline{\text{WR}}$: Write Operation In Multiplexed and Intel modes, this pin is asserted low to initiate a write operation. In Motorola mode, this pin is asserted low to initiate a write operation or s asserted high to initiate a read operation. In EPROM and Serial modes, this pin should be connected to ground.
$\overline{\text{RD}}$	72	I pull-up	CMOS	$\overline{\text{RD}}$: Read Operation In Multiplexed and Intel modes, this pin is asserted low to initiate a read operation. In EPROM, Motorola and Serial modes, this pin should be connected to ground.
ALE / SCLK	73	I pull-down	CMOS	ALE: Address Latch Enable In Multiplexed mode, the address on AD[7:0] pins is sampled into the device on the falling edge of ALE. SCLK: Shift Clock In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. In EPROM, Intel and Motorola modes, this pin should be connected to ground.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
RDY	75	O	CMOS	RDY: Ready/Data Acknowledge In Multiplexed and Intel modes, a high level on this pin indicates that a read/write cycle is completed. A low level on this pin indicates that wait state must be inserted. In Motorola mode, a low level on this pin indicates that valid information on the data bus is ready for a read operation or acknowledges the acceptance of the written data during a write operation. In EPROM and Serial modes, this pin should be connected to ground.
JTAG (per IEEE 1149.1)				
$\overline{\text{TRST}}$	2	I pull-down	CMOS	**$\overline{\text{TRST}}$**: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
TMS	7	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
TCK	9	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
TDI	23	I pull-up	CMOS	TDI: JTAG Test Data Input The test data is input on this pin. It is clocked into the device on the rising edge of TCK.
TDO	21	O	CMOS	TDO: JTAG Test Data Output The test data is output on this pin. It is clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of T0 selected input clock fail, as determined by the LOS_-FLAG_ON_TDO bit (b6, 0BH). Refer to Chapter 3.8.1 Input Clock Validity for details.
Power & Ground				
VDDD1	12	Power	-	VDDDn: 3.3 V Digital Power Supply Each VDDDn should be paralleled with ground through a 0.1 µF capacitor.
VDDD2	16			
VDDD3	13			
VDDD4	50			
VDDD5	61			
VDDD6	85			
VDDD7	86			
VDDA1	6	Power	-	VDDAn: 3.3 V Analog Power Supply Each VDDAn should be paralleled with ground through a 0.1 µF capacitor.
VDDA2	19			
VDDA3	91			
VDD_AMI	26	Power	-	VDD_AMI: 3.3 V Power Supply for AMI I/O
VDD_DIFF1	33	Power	-	VDD_DIFF1: 3.3 V Power Supply for OUT6
VDD_DIFF2	39	Power	-	VDD_DIFF2: 3.3 V Power Supply for OUT7

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1]
DGND1	11	Ground	-	DGNDn: Digital Ground
DGND2	15			
DGND3	14			
DGND4	49			
DGND5	62			
DGND6	84			
DGND7	87			
AGND1	5	Ground	-	AGNDn: Analog Ground
AGND2	20			
AGND3	92			
GND_DIFF1	32	Ground	-	GND_DIFF: Ground for OUT6
GND_DIFF2	38	Ground	-	GND_DIFF: Ground for OUT7
GND_AMI	29	Ground	-	GND_AMI: Ground for AMI I/O
AGND	1	Ground	-	AGND: Analog Ground
Others				
IC1	3	-	-	IC: Internal Connected Internal Use. These pins should be left open for normal operation.
IC2	4			
IC3	17			
IC4	22			
IC5	96			
IC6	97			
IC7	98			
NC	44	-	-	NC: Not Connected

Note:
1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.
2. The contents in the brackets indicate the position of the register bit/bits.
3. N x 8 kHz: $1 \le N \le 19440$.
4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64.
5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, 64, 96.
6. N x 13.0 MHz: N = 1, 2, 4.
7. N x 3.84 MHz: N = 1, 2, 4, 8, 16, 10, 20, 40.

3 FUNCTIONAL DESCRIPTION

3.1 RESET

The reset operation resets all registers and state machines to their default value or status.

After power on, the device must be reset for normal operation.

For a complete reset, the $\overline{\text{RST}}$ pin must be asserted low for at least 50 µs. After the $\overline{\text{RST}}$ pin is pulled high, the device will still be in reset state for 500 ms (typical). If the $\overline{\text{RST}}$ pin is held low continuously, the device remains in reset state.

3.2 MASTER CLOCK

A nominal 12.8000 MHz clock, provided by a crystal oscillator, is input on the OSCI pin. This clock is provided for the device as a master clock. The master clock is used as a reference clock for all the internal circuits. A better active edge of the master clock is selected by the OSC_EDGE bit to improve jitter and wander performance.

In fact, an offset from the nominal frequency may input on the OSCI pin. This offset can be compensated by setting the NOMINAL_FREQ_VALUE[23:0] bits. The calibration range is within ±741 ppm.

The performance of the master clock should meet GR-1244-CORE, GR-253-CORE, ITU-T G.812 and G.813 criteria.

Table 2: Related Bit / Register in Chapter 3.2

Bit	Register	Address (Hex)
NOMINAL_FREQ_VALUE[23:0]	NOMINAL_FREQ[23:16]_CNFG, NOMINAL_FREQ[15:8]_CNFG, NOMINAL_FREQ[7:0]_CNFG	06, 05, 04
OSC_EDGE	DIFFERENTIAL_IN_OUT_OSCI_CNFG	0A

3.3 INPUT CLOCKS & FRAME SYNC SIGNAL

Altogether 14 clocks and 1 frame sync signal are input to the device.

3.3.1 INPUT CLOCKS

The device provides 14 input clock ports.

According to the input port technology, the input ports support the following technologies:

- AMI
- PECL/LVDS
- CMOS

According to the input clock source, the following clock sources are supported:

- T1: Recovered clock from STM-N or OC-n
- T2: PDH network synchronization timing
- T3: External synchronization reference timing

IN1 and IN2 support the AMI input signal only and the clock source is from T3. The input clock is a 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock. The 400HZ_SEL bit should be set to match the input frequency. Any input violation that does not meet the standard composite clock structure will induce an AMI violation. The AMI violation is indicated by the AMI1_VIOL ^{1} / AMI2_VIOL ^{1} bit. If the AMI1_VIOL ^{2} / AMI2_VIOL ^{2} bit is '1', the occurrence of an AMI violation will trigger an interrupt.

IN3, IN4 and IN7 ~ IN14 support CMOS input signal only and the clock sources can be from T1, T2 or T3.

IN5 and IN6 support PECL/LVDS input signal and automatically detect whether the signal is PECL or LVDS. The clock sources can be from T1, T2 or T3.

For SDH and SONET networks, the default frequency is different. SONET / SDH frequency selection is controlled by the IN_SONET_SDH bit. During reset, the default value of the IN_SONET_SDH bit is determined by the SONET/$\overline{\text{SDH}}$ pin: high for SONET and low for SDH. After reset, the input signal on the SONET/$\overline{\text{SDH}}$ pin takes no effect.

IDT82V3280 supports single-ended input for differential input. Refer to Chapter 9.3.3.3 Single-Ended Input for Differential Input.

3.3.2 FRAME SYNC INPUT SIGNALS

A 2 kHz, 4 kHz or 8 kHz frame sync signal is input on the EX_SYNC1 pin. It is a CMOS input. The input frequency should match the setting in the SYNC_FREQ[1:0] bits.

The frame sync input signal is used for frame sync output signal synchronization. Refer to Chapter 3.13.2 Frame SYNC Output Signals for details.

Table 3: Related Bit / Register in Chapter 3.3

Bit	Register	Address (Hex)
400HZ_SEL	IN1_CNFG	14
	IN2_CNFG	15
AMI1_VIOL ^{1}	INTERRUPT3_STS	0F
AMI2_VIOL ^{1}		
AMI1_VIOL ^{2}	INTERRUPTS3_ENABLE_CNFG	12
AMI2_VIOL ^{2}		
IN_SONET_SDH	INPUT_MODE_CNFG	09
SYNC_FREQ[1:0]		

3.4 INPUT CLOCK PRE-DIVIDER

Each input clock is assigned an internal Pre-Divider. The Pre-Divider is used to divide the clock frequency down to the DPLL's required input frequency, which is no more than 38.88 MHz.

For IN1 and IN2, the DPLL required frequency is fixed to 8 kHz (i.e., the corresponding IN_FREQ[3:0] bits are '0000'). The 8 kHz clock is extracted from the composite clock and the Pre-Divider is bypassed automatically.

For IN3 ~ IN14, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

Each Pre-Divider consists of a DivN Divider and a Lock 8k Divider. IN3 and IN4 also include an HF (High Frequency) Divider. Figure 3 shows a block diagram of the pre-dividers for an input clock.

When the Lock 8k Divider is used, the input clock is divided down to 8 kHz internally; the PRE_DIVN_VALUE [14:0] bits are not required. Lock 8k Divider can be used for 1.544 MHz, 2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz or 38.88 MHz input clock frequency and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency. For 2 kHz, 4 kHz or 8 kHz input clock frequency only, the Pre-Divider is bypassed and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency. The input clock can be inverted, as determine by the IN_2K_4K_8K_INV bit.

The HF Divider, which is only available for IN5 and IN6, should be used when the input clock is higher than (>) 155.52 MHz. The input clock can be divided by 4, 5 or can bypass the HF Divider, as determined by the IN5_DIV[1:0]/IN6_DIV[1:0] bits correspondingly.

Either the DivN Divider or the Lock 8k Divider can be used or both can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit.

When the DivN Divider is used for INn ($3 \leq n \leq 14$), the division factor setting should observe the following order:

1. *Select an input clock by the PRE_DIV_CH_VALUE[3:0] bits;*
2. *Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;*
3. *Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.*

Once the division factor is set for the input clock selected by the PRE_DIV_CH_VALUE[3:0] bits, it is valid until a different division factor is set for the same input clock. The division factor is calculated as follows:

Division Factor = (the frequency of the clock input to the DivN Divider ÷ the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits) - 1

The DivN Divider can only divide the input clock whose frequency is lower than (<) 155.52 MHz.

The Pre-Divider configuration and the division factor setting depend on the input clock on one of the IN3 ~ IN14 pins and the DPLL required clock. Here is an example:

The input clock on the IN6 pin is 622.08 MHz; the DPLL required clock is 6.48 MHz by programming the IN_FREQ[3:0] bits of register IN6 to '0010'. Do the following step by step to divide the input clock:

1. *Use the HF Divider to divide the clock down to 155.52 MHz:*
   622.08 ÷ 155.52 = 4, so set the IN6_DIV[1:0] bits to '01';
2. *Use the DivN Divider to divide the clock down to 6.48 MHz:*
   Set the PRE_DIV_CH_VALUE[3:0] bits to '0110';
   Set the DIRECT_DIV bit in Register IN6_CNFG to '1' and the LOCK_8K bit in Register IN6_CNFG to '0';
   155.52 ÷ 6.48 = 24; 24 - 1 = 23, so set the PRE_DIVN_VALUE[14:0] bits to '10111'.

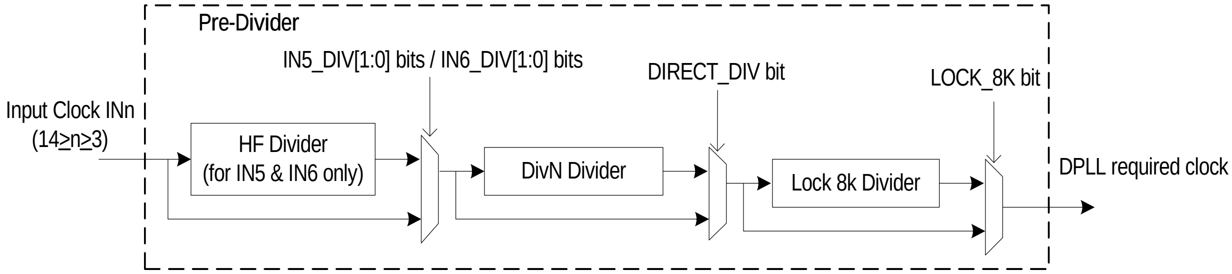


Figure 3. Pre-Divider for An Input Clock

Table 4: Related Bit / Register in Chapter 3.4

Bit	Register	Address (Hex)
IN5_DIV[1:0]	IN5_IN6_HF_DIV_CNFG	18
IN6_DIV[1:0]		
IN_FREQ[3:0]	IN1_CNFG ~ IN14_CNFG	14 ~ 17, 19 ~ 22
IN_2K_4K_8K_INV	FR_MFR_SYNC_CNFG	74
DIRECT_DIV	IN3_CNFG ~ IN14_CNFG	16, 17, 19 ~ 22
LOCK_8K		
PRE_DIV_CH_VALUE[3:0]	PRE_DIV_CH_CNFG	23
PRE_DIVN_VALUE[14:0]	PRE_DIVN[14:8]_CNFG, PRE_DIVN[7:0]_CNFG	25, 24

3.5 INPUT CLOCK QUALITY MONITORING

The qualities of all the input clocks are always monitored in the following aspects:

- LOS (loss of signal) (only for IN1 and IN2)
- Activity
- Frequency

LOS monitoring is only conducted on IN1 and IN2. Activity and frequency monitoring are conducted on all the input clocks.

The qualified clocks are available for T0/T4 DPLL selection. The T0 and T4 selected input clocks have to be monitored further. Refer to Chapter 3.7 Selected Input Clock Monitoring for details.

3.5.1 LOS MONITORING

IN1 and IN2 support the AMI input signal. LOS monitoring is conducted on IN1 and IN2. A LOS event occurs when the amplitude of the input clock falls below +0.6 Vp-p for 1 ms; the LOS event is cleared when the amplitude rises higher than +1 Vp-p.

LOS status is indicated by the AMI1_LOS [1] / AMI2_LOS [1] bit. If the AMI1_LOS [2] / AMI2_LOS [2] bit is ‘1’, the occurrence of LOS will trigger an interrupt.

The input clock in LOS status is disqualified for clock selection for T0/T4 DPLL.

3.5.2 ACTIVITY MONITORING

Activity is monitored by using an internal leaky bucket accumulator, as shown in Figure 4.

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms and the internal leaky bucket accumulator increases by 1 when an event is detected; it decreases by 1 if no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the master clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the corresponding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; ‘n’ is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_NO_ACTIVITY_ALARM bit (14 ≥ n ≥ 1).

The input clock with a no-activity alarm is disqualified for clock selection for T0/T4 DPLL.

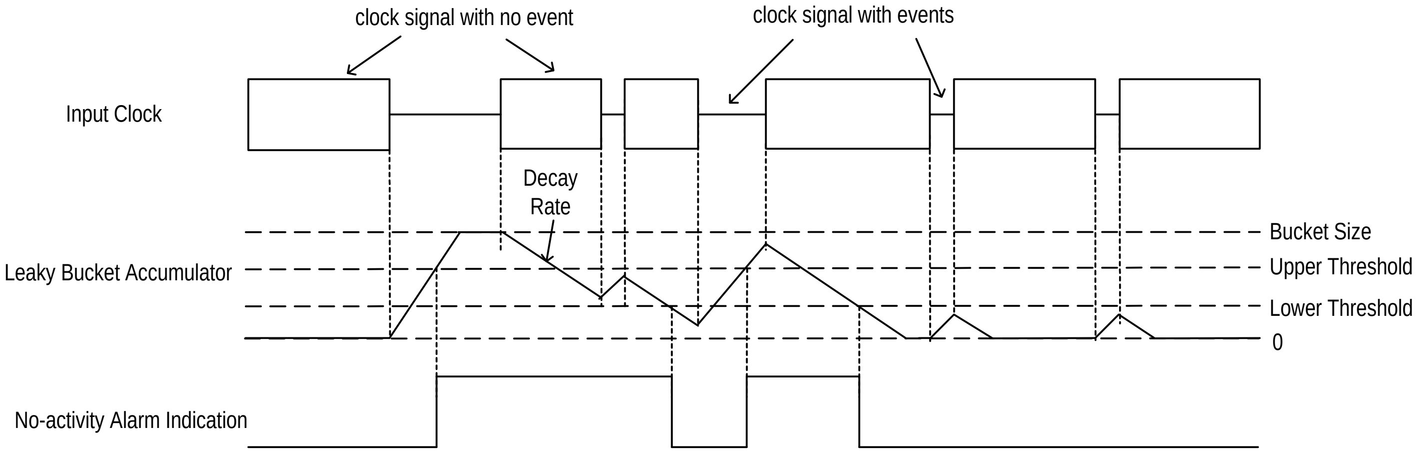


Figure 4. Input Clock Activity Monitoring

3.5.3 FREQUENCY MONITORING

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the master clock or the output of T0 DPLL, as determined by the FREQ_MON_CLK bit.

A frequency hard alarm threshold is set for frequency monitoring. If the FREQ_MON_HARD_EN bit is '1', a frequency hard alarm is raised when the frequency of the input clock with respect to the reference clock is above the threshold; the alarm is cleared when the frequency is below the threshold.

The frequency hard alarm threshold can be calculated as follows:

Frequency Hard Alarm Threshold (ppm) = (ALL_FREQ_HARD_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0]

If the FREQ_MON_HARD_EN bit is '1', the frequency hard alarm status of the input clock is indicated by the INn_FREQ_HARD_ALARM bit (14 ≥ n ≥ 1). When the FREQ_MON_HARD_EN bit is '0', no frequency hard alarm is raised even if the input clock is above the frequency hard alarm threshold.

The input clock with a frequency hard alarm is disqualified for clock selection for T0/T4 DPLL.

In addition, if the input clock is 2 kHz, 4 kHz or 8 kHz, its clock edges with respect to the reference clock are monitored. If any edge drifts outside ±5%, the input clock is disqualified for clock selection for T0/T4 DPLL. The input clock is qualified if any edge drifts inside ±5%. This function is supported only when the IN_NOISE_WINDOW bit is '1'.

The frequency of each input clock with respect to the reference clock can be read by doing the following step by step:

1. *Select an input clock by setting the IN_FREQ_READ_CH[3:0] bits;*
2. *Read the value in the IN_FREQ_VALUE[7:0] bits and calculate as follows:*

   Input Clock Frequency (ppm) = IN_FREQ_VALUE[7:0] X FREQ_MON_FACTOR[3:0]

Note that the value set by the FREQ_MON_FACTOR[3:0] bits depends on the application.

Table 5: Related Bit / Register in Chapter 3.5

Bit	Register	Address (Hex)
AMI1_LOS [1]	INTERRUPTS3_STS	0F
AMI2_LOS [1]		
AMI1_LOS [2]	INTERRUPTS3_ENABLE_CNFG	12
AMI2_LOS [2]		
BUCKET_SIZE_n_DATA[7:0] (3 ≥ n ≥ 0)	BUCKET_SIZE_0_CNFG ~ BUCKET_SIZE_3_CNFG	33, 37, 3B, 3F
UPPER_THRESHOLD_n_DATA[7:0] (3 ≥ n ≥ 0)	UPPER_THRESHOLD_0_CNFG ~ UPPER_THRESHOLD_3_CNFG	31, 35, 39, 3D
LOWER_THRESHOLD_n_DATA[7:0] (3 ≥ n ≥ 0)	LOWER_THRESHOLD_0_CNFG ~ LOWER_THRESHOLD_3_CNFG	32, 36, 3A, 3E
DECAY_RATE_n_DATA[1:0] (3 ≥ n ≥ 0)	DECAY_RATE_0_CNFG ~ DECAY_RATE_3_CNFG	34, 38, 3C, 40
BUCKET_SEL[1:0]	IN1_CNFG ~ IN14_CNFG	14 ~ 17, 19 ~ 22
INn_NO_ACTIVITY_ALARM (14 ≥ n ≥ 1)	IN1_IN2_STS ~ IN13_IN14_STS	43 ~ 49
INn_FREQ_HARD_ALARM (14 ≥ n ≥ 1)		
FREQ_MON_CLK	MON_SW_PBO_CNFG	0B
FREQ_MON_HARD_EN		
ALL_FREQ_HARD_THRESHOLD[3:0]	ALL_FREQ_MON_THRESHOLD_CNFG	2F
FREQ_MON_FACTOR[3:0]	FREQ_MON_FACTOR_CNFG	2E
IN_NOISE_WINDOW	PHASE_MON_PBO_CNFG	78
IN_FREQ_READ_CH[3:0]	IN_FREQ_READ_CH_CNFG	41
IN_FREQ_VALUE[7:0]	IN_FREQ_READ_STS	42

3.6 T0 / T4 DPLL INPUT CLOCK SELECTION

An input clock is selected for T0 DPLL and for T4 DPLL respectively.

For T0 path, the EXT_SW bit and the T0_INPUT_SEL[3:0] bits determine the input clock selection, as shown in Table 6:

Table 6: Input Clock Selection for T0 Path

Control Bits		Input Clock Selection
EXT_SW	T0_INPUT_SEL[3:0]	
1	don't-care	External Fast selection
0	other than 0000	Forced selection
	0000	Automatic selection

For T4 path, the T4 DPLL may lock to a T0 DPLL output or lock independently from T0 path, as determined by the T4_LOCK_T0 bit. When the T4 DPLL locks to the T0 DPLL output, the T4 selected input clock is a 77.76 MHz or 8 kHz signal from the T0 DPLL 77.76 MHz path (refer to Chapter 3.11.5.1 T0 Path), as determined by the T0_FOR_T4 bit. When the T4 path locks independently from the T0 path, the T4 DPLL input clock selection is determined by the T4_INPUT_SEL[3:0] bits. Refer to Table 7:

Table 7: Input Clock Selection for T4 Path

Control Bits - T4_INPUT_SEL[3:0]	Input Clock Selection
other than 0000	Forced selection
0000	Automatic selection

External Fast selection is done between IN3/IN5 and IN4/IN6 pairs.

Forced selection is done by setting the related registers.

Automatic selection is done based on the results of input clocks quality monitoring and the related registers configuration.

The selected input clock is attempted to be locked in T0/T4 DPLL.

3.6.1 EXTERNAL FAST SELECTION (T0 ONLY)

The External Fast selection is supported by T0 path only. In External Fast selection, only IN3/IN5 and IN4/IN6 pairs are available for selection. Refer to Figure 5. The results of input clocks quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring) do not affect input clock selection.

The T0 input clock selection is determined by the FF_SRCSW pin after reset (this pin determines the default value of the EXT_SW bit during reset, refer to Chapter 2 Pin Description), the IN3_SEL_PRIORITY[3:0] bits and the IN4_SEL_PRIORITY[3:0] bits, as shown in Figure 5 and Table 8:

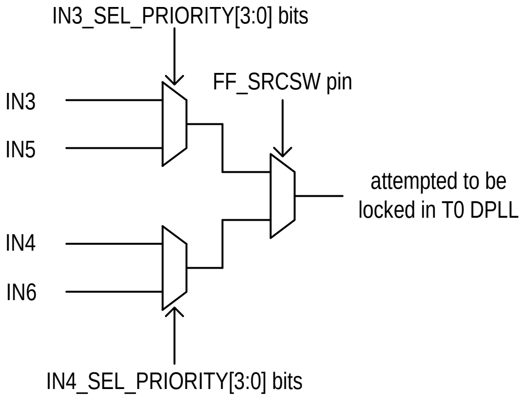


Figure 5. External Fast Selection

Table 8: External Fast Selection

Control Pin & Bits			the Selected Input Clock
FF_SRCSW (after reset)	IN3_SEL_PRIORITY[3:0]	IN4_SEL_PRIORITY[3:0]	
high	0000	don't-care	IN5
	other than 0000		IN3
low	don't-care	0000	IN6
		other than 0000	IN4

3.6.2 FORCED SELECTION

In Forced selection, the selected input clock is set by the T0_INPUT_SEL[3:0] / T4_INPUT_SEL[3:0] bits. The results of input clocks quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring) do not affect the input clock selection.

3.6.3 AUTOMATIC SELECTION

In Automatic selection, the input clock selection is determined by its validity, priority and locking allowance configuration. The validity depends on the results of input clock quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring). Locking allowance is configured by the corresponding INn_VALID bit(14 ≥ n ≥ 1). Refer to Figure 6. In all the qualified input clocks, the one with the highest priority is selected. The priority is set by the corresponding INn_SEL_PRIORITY[3:0] bits (14 ≥ n ≥ 1). If more than one qualified input clock INn is available and has the same priority, the input clock with the smallest 'n' is selected.

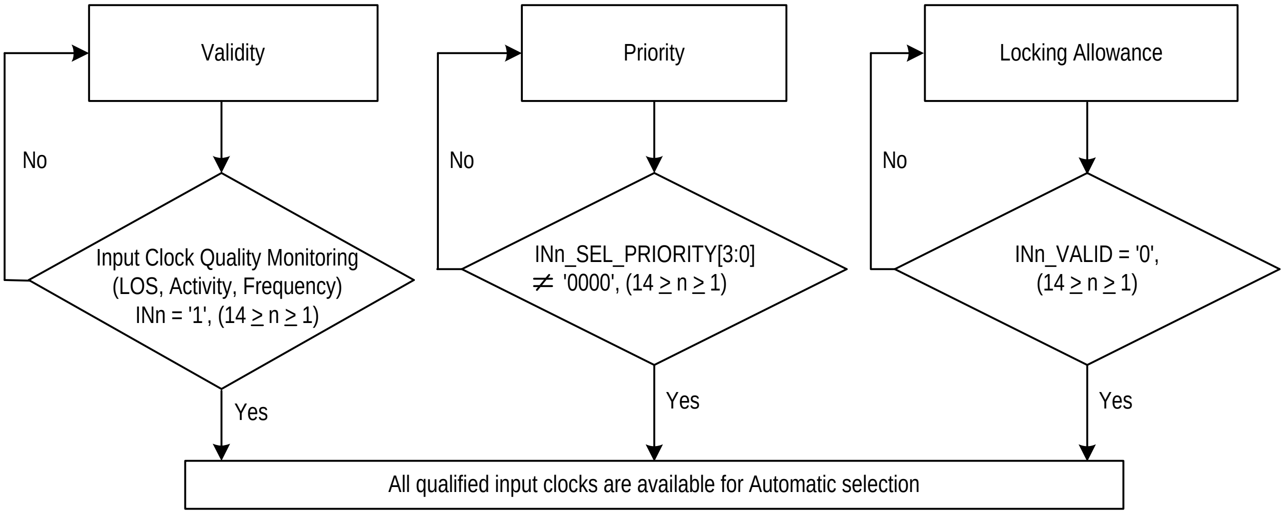


Figure 6. Qualified Input Clocks for Automatic Selection

Table 9: Related Bit / Register in Chapter 3.6

Bit	Register	Address (Hex)
EXT_SW	MON_SW_PBO_CNFG	0B
T0_INPUT_SEL[3:0]	T0_INPUT_SEL_CNFG	50
T4_LOCK_T0	T4_INPUT_SEL_CNFG	51
T0_FOR_T4		
T4_INPUT_SEL[3:0]		
INn_SEL_PRIORITY[3:0] (14 ≥ n ≥ 1)	IN1_IN2_SEL_PRIORITY_CNFG ~ IN13_IN14_SEL_PRIORITY_CNFG	26 ~ 2C *
INn_VALID (14 ≥ n ≥ 1)	REMOTE_INPUT_VALID1_CNFG, REMOTE_INPUT_VALID2_CNFG	4C, 4D
INn (14 ≥ n ≥ 1)	INPUT_VALID1_STS, INPUT_VALID2_STS	4A, 4B
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 26 ~ 2C registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.7 SELECTED INPUT CLOCK MONITORING

The quality of the selected input clock is always monitored (refer to Chapter 3.5 Input Clock Quality Monitoring) and the DPLL locking status is always monitored.

3.7.1 T0 / T4 DPLL LOCKING DETECTION

The following events is always monitored:

- Fast Loss;
- Coarse Phase Loss;
- Fine Phase Loss;
- Hard Limit Exceeding.

3.7.1.1 Fast Loss

A fast loss is triggered when the selected input clock misses 2 consecutive clock cycles. It is cleared once an active clock edge is detected.

For T0 path, the occurrence of the fast loss will result in T0 DPLL unlocked if the FAST_LOS_SW bit is '1'. For T4 path, the occurrence of the fast loss will result in T4 DPLL unlocked regardless of the FAST_LOS_SW bit.

3.7.1.2 Coarse Phase Loss

The T0/T4 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the coarse phase limit, a coarse phase loss is triggered. It is cleared once the phase-compared result is within the coarse phase limit.

When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to Table 10. When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to Table 11.

Table 10: Coarse Phase Limit Programming (the selected input clock of 2 kHz, 4 kHz or 8 kHz)

MULTI_PH_8K_4K_2K_EN	WIDE_EN	Coarse Phase Limit
0	don't-care	±1 UI
1	0	±1 UI
	1	set by the PH_LOS_COARSE_LIMT[3:0] bits

Table 11: Coarse Phase Limit Programming (the selected input clock of other than 2 kHz, 4 kHz and 8 kHz)

WIDE_EN	Coarse Phase Limit
0	±1 UI
1	set by the PH_LOS_COARSE_LIMT[3:0] bits

The occurrence of the coarse phase loss will result in T0/T4 DPLL unlocked if the COARSE_PH_LOS_LIMT_EN bit is '1'.

3.7.1.3 Fine Phase Loss

The T0/T4 DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the fine phase limit programmed by the PH_LOS_FINE_LIMT[2:0] bits, a fine phase loss is triggered. It is cleared once the phase-compared result is within the fine phase limit.

The occurrence of the fine phase loss will result in T0/T4 DPLL unlocked if the FINE_PH_LOS_LIMT_EN bit is '1'.

3.7.1.4 Hard Limit Exceeding

Two limits are available for this monitoring. They are DPLL soft limit and DPLL hard limit. When the frequency of the DPLL output with respect to the master clock exceeds the DPLL soft / hard limit, a DPLL soft / hard alarm will be raised; the alarm is cleared once the frequency is within the corresponding limit. The occurrence of the DPLL soft alarm does not affect the T0/T4 DPLL locking status. The DPLL soft alarm is indicated by the corresponding T0_DPLL_SOFT_FREQ_ALARM / T4_DPLL_SOFT_FREQ_ALARM bit. The occurrence of the DPLL hard alarm will result in T0/T4 DPLL unlocked if the FREQ_LIMT_PH_LOS bit is '1'.

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMT[6:0] bits and can be calculated as follows:

DPLL Soft Limit (ppm) = DPLL_FREQ_SOFT_LIMT[6:0] X 0.724

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMT[15:0] bits and can be calculated as follows:

DPLL Hard Limit (ppm) = DPLL_FREQ_HARD_LIMT[15:0] X 0.0014

3.7.2 LOCKING STATUS

The DPLL locking status depends on the locking monitoring results. The DPLL is in locked state if none of the following events is triggered during 2 seconds; otherwise, the DPLL is unlocked.

- Fast Loss (the FAST_LOS_SW bit is '1');
- Coarse Phase Loss (the COARSE_PH_LOS_LIMT_EN bit is '1');
- Fine Phase Loss (the FINE_PH_LOS_LIMT_EN bit is '1');
- DPLL Hard Alarm (the FREQ_LIMT_PH_LOS bit is '1').

If the FAST_LOS_SW bit, the COARSE_PH_LOS_LIMT_EN bit, the FINE_PH_LOS_LIMT_EN bit or the FREQ_LIMT_PH_LOS bit is '0', the DPLL locking status will not be affected even if the corresponding event is triggered. If all these bits are '0', the DPLL will be in locked state in 2 seconds.

The DPLL locking status is indicated by the T0_DPLL_LOCK / T4_DPLL_LOCK bit.

The T4_STS [1] bit will be set when the locking status of the T4 DPLL changes (from 'lock' to 'unlock' or from 'unlock' to 'lock'). If the T4_STS [2] bit is '1', an interrupt will be generated.

3.7.3 PHASE LOCK ALARM (T0 ONLY)

A phase lock alarm will be raised when the selected input clock can not be locked in T0 DPLL within a certain period. This period can be calculated as follows:

Period (sec.) = TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0]

The phase lock alarm is indicated by the corresponding INn_PH_LOCK_ALARM bit (14 ≥ n ≥ 1).

The phase lock alarm can be cleared by the following two ways, as selected by the PH_ALARM_TIMEOUT bit:

- Be cleared when a ‘1’ is written to the corresponding INn_PH_LOCK_ALARM bit;
- Be cleared after the period (= *TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0] in second*) which starts from when the alarm is raised.

The selected input clock with a phase lock alarm is disqualified for T0 DPLL locking.

Note that no phase lock alarm is raised if the T4 selected input clock can not be locked.

Table 12: Related Bit / Register in Chapter 3.7

Bit	Register	Address (Hex)
FAST_LOS_SW	PHASE_LOSS_FINE_LIMIT_CNFG	5B *
PH_LOS_FINE_LIMT[2:0]		
FINE_PH_LOS_LIMT_EN		
MULTI_PH_8K_4K_2K_EN	PHASE_LOSS_COARSE_LIMIT_CNFG	5A *
WIDE_EN		
PH_LOS_COARSE_LIMT[3:0]		
COARSE_PH_LOS_LIMT_EN		
T0_DPLL_SOFT_FREQ_ALARM	OPERATING_STS	52
T4_DPLL_SOFT_FREQ_ALARM		
T0_DPLL_LOCK		
T4_DPLL_LOCK		
DPLL_FREQ_SOFT_LIMT[6:0]	DPLL_FREQ_SOFT_LIMIT_CNFG	65
FREQ_LIMT_PH_LOS		
DPLL_FREQ_HARD_LIMT[15:0]	DPLL_FREQ_HARD_LIMIT[15:8]_CNFG, DPLL_FREQ_HARD_LIMIT[7:0]_CNFG	67, 66
T4_STS [1]	INTERRUPTS3_STS	0F
T4_STS [2]	INTERRUPTS3_ENABLE_CNFG	12
TIME_OUT_VALUE[5:0]	PHASE_ALARM_TIME_OUT_CNFG	08
MULTI_FACTOR[1:0]		
INn_PH_LOCK_ALARM (14 ≥ n ≥ 1)	IN1_IN2_STS ~ IN13_IN14_STS	43 ~ 49
PH_ALARM_TIMEOUT	INPUT_MODE_CNFG	09
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 5A and 5B registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.8 SELECTED INPUT CLOCK SWITCH

If the input clock is selected by External Fast selection or by Forced selection, it can be switched by setting the related registers (refer to Chapter 3.6.1 External Fast Selection (T0 only) & Chapter 3.6.2 Forced Selection) any time. In this case, whether the input clock is qualified for DPLL locking does not affect the clock switch. If the T4 selected input clock is a T0 DPLL output, it can only be switched by setting the T0_FOR_T4 bit.

When the input clock is selected by Automatic selection, the input clock switch depends on its validity, priority and locking allowance configuration. If the current selected input clock is disqualified, a new qualified input clock may be switched to.

3.8.1 INPUT CLOCK VALIDITY

For all the input clocks, the validity depends on the results of input clock quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring). When all of the following conditions are satisfied, the input clock is valid; otherwise, it is invalid.

- No LOS (the AMI1_LOS / AMI2_LOS bit is '0');
- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is '0');
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is '0');
- If the IN_NOISE_WINDOW bit is '1', all the edges of the input clock of 2 kHz, 4 kHz or 8 kHz drift inside ±5%; if the IN_NOISE_WINDOW bit is '0', this condition is ignored.

The validity qualification of the T0 selected input clock is different from that of the T4 selected input clock. The validity qualification of the T4 selected input clock is the same as the above. The T0 selected input clock is valid when all of the above and the following conditions are satisfied; otherwise, it is invalid.

- No phase lock alarm, i.e., the INn_PH_LOCK_ALARM bit is '0';
- If the ULTR_FAST_SW bit is '1', the T0 selected input clock misses less than (<) 2 consecutive clock cycles; if the ULTR_FAST_SW bit is '0', this condition is ignored.

The validities of all the input clocks are indicated by the INn [1] bit (14 ≥ n ≥ 1). When the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), the INn [2] bit will be set. If the INn [3] bit is '1', an interrupt will be generated.

When the T0 selected input clock has failed, i.e., the validity of the T0 selected input clock changes from 'valid' to 'invalid', the T0_MAIN_REF_FAILED [1] bit will be set. If the T0_MAIN_REF_FAILED [2] bit is '1', an interrupt will be generated. This interrupt can also be indicated by hardware - the TDO pin, as determined by the LOS_FLAG_TO_TDO bit. When the TDO pin is used to indicate this interrupt, it will be set high when this interrupt is generated and will remain high until this interrupt is cleared.

3.8.2 SELECTED INPUT CLOCK SWITCH

When the device is configured as Automatic input clock selection, T0 input clock switch is different from T4 input clock switch.

For T0 path, Revertive and Non-Revertive switches are supported, as selected by the REVERTIVE_MODE bit.

For T4 path, only Revertive switch is supported.

The difference between Revertive and Non-Revertive switches is that whether the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available for selection. In Non-Revertive switch, input clock switch is minimized.

Conditions of the qualified input clocks available for T0 selection are different from that for T4 selection, as shown in Table 13:

Table 13: Conditions of Qualified Input Clocks Available for T0 & T4 Selection

	Conditions of Qualified Input Clocks Available for T0 & T4 Selection
T0	• Valid, i.e., the INn [1] bit is '1'; • Priority enabled, i.e., the corresponding INn_SEL_PRIORITY[3:0] bits are not '0000'; • Locking to the input clock is allowed, i.e., the corresponding INn_VALID bit is '0'.
T4	• Valid (all the validity conditions listed in Chapter 3.8.1 Input Clock Validity are satisfied); • Priority enabled, i.e., the corresponding INn_SEL_PRIORITY[3:0] bits are not '0000'; • Locking to the input clock is allowed, i.e., the corresponding INn_VALID bit is '0'.

The input clock is disqualified if any of the above conditions is not satisfied.

In summary, the selected input clock can be switched by:

- External Fast selection (supported by T0 path only);
- Forced selection;
- Revertive switch;
- Non-Revertive switch (supported by T0 path only);
- T4 DPLL locked to T0 DPLL output (supported by T4 path only).

3.8.2.1 Revertive Switch

In Revertive switch, the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available.

The selected input clock is switched if any of the following is satisfied:

- the selected input clock is disqualified;
- another qualified input clock with a higher priority than the selected input clock is available.

A qualified input clock with the highest priority is selected by revertive switch. If more than one qualified input clock INn is available and has the same priority, the input clock with the smallest 'n' is selected.

3.8.2.2 Non-Revertive Switch (T0 only)

In Non-Revertive switch, the T0 selected input clock is not switched when another qualified input clock with a higher priority than the current selected input clock is available. In this case, the selected input clock is switched and a qualified input clock with the highest priority is selected only when the T0 selected input clock is disqualified. If more than one qualified input clock is available and has the same priority, the input clock with the smallest ‘n’ is selected.

3.8.3 SELECTED / QUALIFIED INPUT CLOCKS INDICATION

The selected input clock is indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits. Note if the T4 selected input clock is a T0 DPLL output, it can not be indicated by these bits.

The qualified input clocks with the three highest priorities are indicated by HIGHEST_PRIORITY_VALIDATED[3:0] bits, the SECOND_PRIORITY_VALIDATED[3:0] bits and the THIRD_PRIORITY _VALIDATED[3:0] bits respectively. If more than one input clock INn has the same priority, the input clock with the smallest ‘n’ is indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits.

When the device is configured in Automatic selection and Revertive switch is enabled, the input clock indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits is the same as the one indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits; otherwise, they are not the same.

When all the input clocks for T4 path changes to be unqualified, the INPUT_TO_T4 ^{1} bit will be set. If the INPUT_TO_T4 ^{2} bit is ‘1’, an interrupt will be generated.

Table 14: Related Bit / Register in Chapter 3.8

Bit	Register	Address (Hex)
T0_FOR_T4	T4_INPUT_SEL_CNFG	51
INn ^{1} (14 ≥ n ≥ 1)	INPUT_VALID1_STS, INPUT_VALID2_STS	4A, 4B
INn ^{2} (14 ≥ n ≥ 1)	INTERRUPTS1_STS, INTERRUPTS2_STS	0D, 0E
INn ^{3} (14 ≥ n ≥ 1)	INTERRUPTS1_ENABLE_CNFG, INTERRUPTS2_ENABLE_CNFG	10, 11
AMI1_LOS	INTERRUPTS3_STS	0F
AMI2_LOS		
INn_NO_ACTIVITY_ALARM (14 ≥ n ≥ 1)	IN1_IN2_STS ~ IN13_IN14_STS	43 ~ 49
INn_FREQ_HARD_ALARM (14 ≥ n ≥ 1)		
INn_PH_LOCK_ALARM (14 ≥ n ≥ 1)		
IN_NOISE_WINDOW	PHASE_MON_PBO_CNFG	78
ULTR_FAST_SW	MON_SW_PBO_CNFG	0B
LOS_FLAG_TO_TDO		
T0_MAIN_REF_FAILED ^{1}	INTERRUPTS2_STS	0E
T0_MAIN_REF_FAILED ^{2}	INTERRUPTS2_ENABLE_CNFG	11
INPUT_TO_T4 ^{1}	INTERRUPTS3_STS	0F
INPUT_TO_T4 ^{2}	INTERRUPTS3_ENABLE_CNFG	12
REVERTIVE_MODE	INPUT_MODE_CNFG	09
INn_SEL_PRIORITY[3:0] (14 ≥ n ≥ 1)	IN1_IN2_SEL_PRIORITY_CNFG ~ IN13_IN14_SEL_PRIORITY_CNFG	26 ~ 2C *
INn_VALID (14 ≥ n ≥ 1)	REMOTE_INPUT_VALID1_CNFG, REMOTE_INPUT_VALID2_CNFG	4C, 4D
CURRENTLY_SELECTED_INPUT[3:0]	PRIORITY_TABLE1_STS	4E *
HIGHEST_PRIORITY_VALIDATED[3:0]		
SECOND_PRIORITY_VALIDATED[3:0]	PRIORITY_TABLE2_STS	4F *
THIRD_PRIORITY_VALIDATED[3:0]		
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 26 ~ 2C, 4E and 4F registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.9 SELECTED INPUT CLOCK STATUS VS. DPLL OPERATING MODE

The operating modes supported by T0 DPLL are more complex than the ones supported by T4 DPLL for T0 path is the main one. T0 DPLL supports three primary operating modes: Free-Run, Locked and Holdover, and three secondary, temporary operating modes: Pre-Locked, Pre-Locked2 and Lost-Phase. T4 DPLL supports three operating modes: Free-Run, Locked and Holdover. The operating modes of T0 DPLL and T4 DPLL can be switched automatically or by force, as controlled by the T0_OPERATING_MODE[2:0] / T4_OPERATING_MODE[2:0] bits respectively.

When the operating mode is switched by force, the operating mode switch is under external control and the status of the selected input clock takes no effect to the operating mode selection. The forced operating mode switch is applicable for special cases, such as testing.

When the operating mode is switched automatically, the internal state machines for T0 and for T4 automatically determine the operating mode respectively.

3.9.1 T0 SELECTED INPUT CLOCK VS. DPLL OPERATING MODE

The T0 DPLL operating mode is controlled by the T0_OPERATING_-MODE[2:0] bits, as shown in Table 15:

Table 15: T0 DPLL Operating Mode Control

T0_OPERATING_MODE[2:0]	T0 DPLL Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked
101	Forced - Pre-Locked2
110	Forced - Pre-Locked
111	Forced - Lost-Phase

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 7.

Whether the operating mode is under external control or is switched automatically, the current operating mode is always indicated by the T0_DPLL_OPERATING_MODE[2:0] bits. When the operating mode switches, the T0_OPERATING_MODE [1] bit will be set. If the T0_OPERATING_MODE [2] bit is ‘1’, an interrupt will be generated.

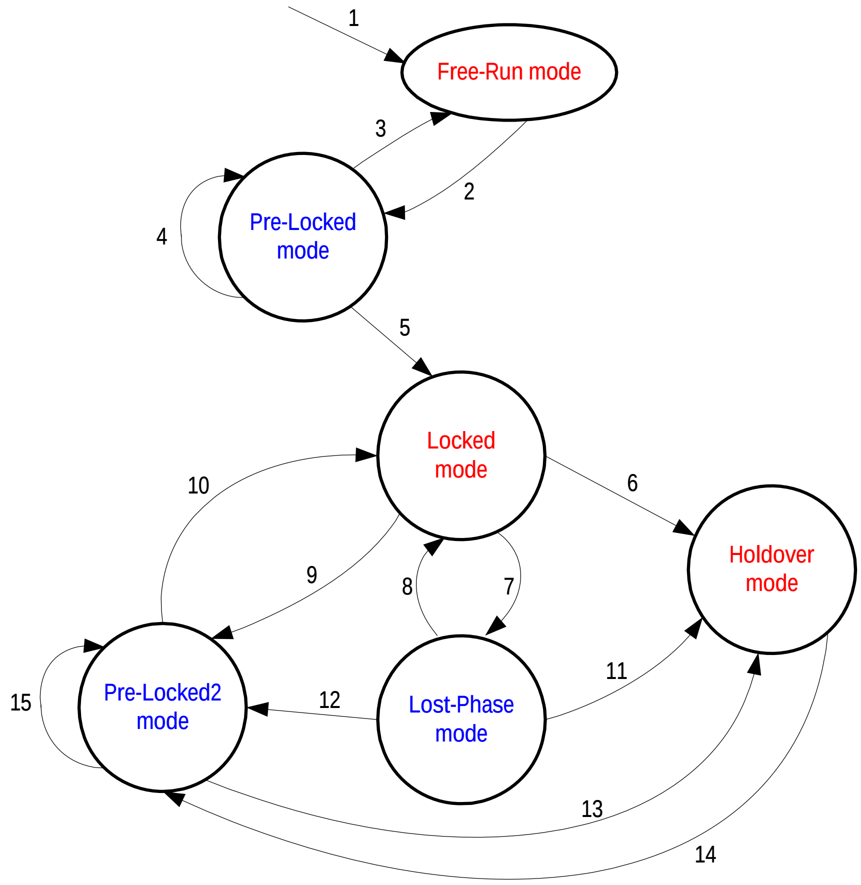


Figure 7. T0 Selected Input Clock vs. DPLL Automatic Operating Mode

Notes to Figure 7:

1. *Reset.*
2. *An input clock is selected.*
3. *The T0 selected input clock is disqualified AND No qualified input clock is available.*
4. *The T0 selected input clock is switched to another one.*
5. *The T0 selected input clock is locked (the T0_DPLL_LOCK bit is ‘1’).*
6. *The T0 selected input clock is disqualified AND No qualified input clock is available.*
7. *The T0 selected input clock is unlocked (the T0_DPLL_LOCK bit is ‘0’).*
8. *The T0 selected input clock is locked again (the T0_DPLL_LOCK bit is ‘1’).*
9. *The T0 selected input clock is switched to another one.*
10. *The T0 selected input clock is locked (the T0_DPLL_LOCK bit is ‘1’).*
11. *The T0 selected input clock is disqualified AND No qualified input clock is available.*
12. *The T0 selected input clock is switched to another one.*
13. *The T0 selected input clock is disqualified AND No qualified input clock is available.*
14. *An input clock is selected.*
15. *The T0 selected input clock is switched to another one.*

The causes of Item 4, 9, 12, 15 - 'the T0 selected input clock is switched to another one' - are: (The T0 selected input clock is disqualified AND Another input clock is switched to) OR (In Revertive switch, a qualified input clock with a higher priority is switched to) OR (The T0 selected input clock is switched to another one by External Fast selection or Forced selection).

Refer to Table 13 for details about the input clock qualification for T0 path.

3.9.2 T4 SELECTED INPUT CLOCK VS. DPLL OPERATING MODE

The T4 DPLL operating mode is controlled by the T4_OPERATING_MODE[2:0] bits, as shown in Table 16:

Table 16: T4 DPLL Operating Mode Control

T4_OPERATING_MODE[2:0]	T4 DPLL Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 8:

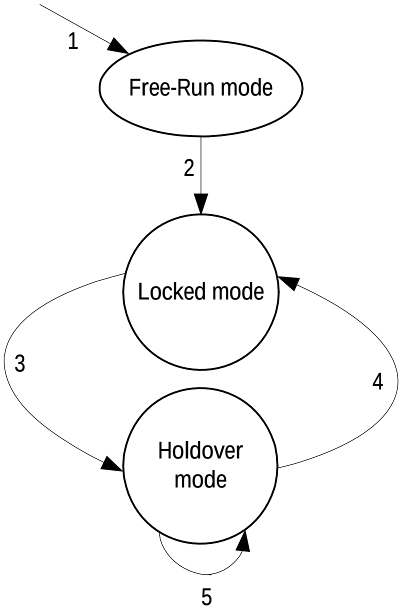


Figure 8. T4 Selected Input Clock vs. DPLL Automatic Operating Mode

Notes to Figure 8:

1. *Reset.*
2. *An input clock is selected.*
3. *(The T4 selected input clock is disqualified) OR (A qualified input clock with a higher priority is switched to) OR (The T4 selected input clock is switched to another one by Forced selection) OR (When T4 DPLL locks to the T0 DPLL output, the T4 selected input clock is switched by setting the T0_FOR_T4 bit).*
4. *An input clock is selected.*
5. *No input clock is selected.*

Refer to Table 13 for details about the input clock qualification for T4 path.

Table 17: Related Bit / Register in Chapter 3.9

Bit	Register	Address (Hex)
T0_OPERATING_MODE[2:0]	T0_OPERATING_MODE_CNFG	53
T4_OPERATING_MODE[2:0]	T4_OPERATING_MODE_CNFG	54
T0_DPLL_OPERATING_MODE[2:0]	OPERATING_STS	52
T0_DPLL_LOCK		
T0_OPERATING_MODE [1]	INTERRUPTS2_STS	0E
T0_OPERATING_MODE [2]	INTERRUPTS2_ENABLE_CNFG	11
T0_FOR_T4	T4_INPUT_SEL_CNFG	51

3.10 T0 / T4 DPLL OPERATING MODE

The T0/T4 DPLL gives a stable performance in different applications without being affected by operating conditions or silicon process variations. It integrates a PFD (Phase & Frequency Detector), a LPF (Low Pass Filter) and a DCO (Digital Controlled Oscillator), which forms a closed loop. If no input clock is selected, the loop is not closed, and the PFD and LPF do not function.

The PFD detects the phase error, including the fast loss, coarse phase loss and fine phase loss (refer to Chapter 3.7.1.1 Fast Loss to Chapter 3.7.1.3 Fine Phase Loss). The averaged phase error of the T0/T4 DPLL feedback with respect to the selected input clock is indicated by the CURRENT_PH_DATA[15:0] bits. It can be calculated as follows:

Averaged Phase Error (ns) = CURRENT_PH_DATA[15:0] X 0.61

The LPF filters jitters. Its 3 dB bandwidth and damping factor are programmable. A range of bandwidths and damping factors can be set to meet different application requirements. Generally, the lower the damping factor is, the longer the locking time is and the more the gain is.

The DCO controls the DPLL output. The frequency of the DPLL output is always multiplied on the basis of the master clock. The phase and frequency offset of the DPLL output may be locked to those of the selected input clock. The current frequency offset with respect to the master clock is indicated by the CURRENT_DPLL_FREQ[23:0] bits, and can be calculated as follows:

Current Frequency Offset (ppm) = CURRENT_DPLL_FREQ[23:0] X 0.000011

3.10.1 T0 DPLL OPERATING MODE

The T0 DPLL loop is closed except in Free-Run mode and Holdover mode.

For a closed loop, different bandwidths and damping factors can be used depending on DPLL locking stages: starting, acquisition and locked.

In the first two seconds when the T0 DPLL attempts to lock to the selected input clock, the starting bandwidth and damping factor are used. They are set by the T0_DPLL_START_BW[4:0] bits and the T0_DPLL_START_DAMPING[2:0] bits respectively.

During the acquisition, the acquisition bandwidth and damping factor are used. They are set by the T0_DPLL_ACQ_BW[4:0] bits and the T0_DPLL_ACQ_DAMPING[2:0] bits respectively.

When the T0 selected input clock is locked, the locked bandwidth and damping factor are used. They are set by the T0_DPLL_LOCKED_BW[4:0] bits and the T0_DPLL_LOCKED_DAMPING[2:0] bits respectively.

The corresponding bandwidth and damping factor are used when the T0 DPLL operates in different DPLL locking stages: starting, acquisition and locked, as controlled by the device automatically.

Only the locked bandwidth and damping factor can be used regardless of the T0 DPLL locking stage, as controlled by the AUTO_BW_SEL bit.

3.10.1.1 Free-Run Mode

In Free-Run mode, the T0 DPLL output refers to the master clock and is not affected by any input clock. The accuracy of the T0 DPLL output is equal to that of the master clock.

3.10.1.2 Pre-Locked Mode

In Pre-Locked mode, the T0 DPLL output attempts to track the selected input clock.

The Pre-Locked mode is a secondary, temporary mode.

3.10.1.3 Locked Mode

In Locked mode, the T0 selected input clock is locked. The phase and frequency offset of the T0 DPLL output track those of the T0 selected input clock.

In this mode, if the T0 selected input clock is in fast loss status and the FAST_LOS_SW bit is '1', the T0 DPLL is unlocked (refer to Chapter 3.7.1.1 Fast Loss) and will enter Lost-Phase mode when the operating mode is switched automatically; if the T0 selected input clock is in fast loss status and the FAST_LOS_SW bit is '0', the T0 DPLL locking status is not affected and the T0 DPLL will enter Temp-Holdover mode automatically.

3.10.1.3.1 Temp-Holdover Mode

The T0 DPLL will automatically enter Temp-Holdover mode with a selected input clock switch or no qualified input clock available when the operating mode switch is under external control.

In Temp-Holdover mode, the T0 DPLL has temporarily lost the selected input clock. The T0 DPLL operation in Temp-Holdover mode and that in Holdover mode are alike (refer to Chapter 3.10.1.5 Holdover Mode) except the frequency offset acquiring methods. See Chapter 3.10.1.5 Holdover Mode for details about the methods. The method is selected by the TEMP_HOLDOVER_MODE[1:0] bits, as shown in Table 18:

Table 18: Frequency Offset Control in Temp-Holdover Mode

TEMP_HOLDOVER_MODE[1:0]	Frequency Offset Acquiring Method
00	the same as that used in Holdover mode
01	Automatic Instantaneous
10	Automatic Fast Averaged
11	Automatic Slow Averaged

The device automatically controls the T0 DPLL to exit from Temp-Holdover mode.

3.10.1.4 Lost-Phase Mode

In Lost-Phase mode, the T0 DPLL output attempts to track the selected input clock.

The Lost-Phase mode is a secondary, temporary mode.

3.10.1.5 Holdover Mode

In Holdover mode, the T0 DPLL resorts to the stored frequency data acquired in Locked mode to control its output. The T0 DPLL output is not phase locked to any input clock. The frequency offset acquiring method is selected by the MAN_HOLDOVER bit, the AUTO_AVG bit and the FAST_AVG bit, as shown in Table 19:

Table 19: Frequency Offset Control in Holdover Mode

MAN_HOLDOVER	AUTO_AVG	FAST_AVG	Frequency Offset Acquiring Method
0	0	don't-care	Automatic Instantaneous
	1	0	Automatic Slow Averaged
		1	Automatic Fast Averaged
1	don't-care		Manual

3.10.1.5.1 Automatic Instantaneous

By this method, the T0 DPLL freezes at the operating frequency when it enters Holdover mode. The accuracy is $4.4X10^{-8}$ ppm.

3.10.1.5.2 Automatic Slow Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 110 minutes. The accuracy is $1.1X10^{-5}$ ppm.

3.10.1.5.3 Automatic Fast Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 8 minutes. The accuracy is $1.1X10^{-5}$ ppm.

3.10.1.5.4 Manual

By this method, the frequency offset is set by the T0_HOLDOVER_FREQ[23:0] bits. The accuracy is $1.1X10^{-5}$ ppm.

The frequency offset of the T0 DPLL output is indicated by the CURRENT_DPLL_FREQ[23:0] bits.

The device provides a reference for the value to be written to the T0_HOLDOVER_FREQ[23:0] bits. The value to be written can refer to the value read from the CURRENT_DPLL_FREQ[23:0] bits or the T0_HOLDOVER_FREQ[23:0] bits (refer to Chapter 3.10.1.5.5 Holdover Frequency Offset Read); or then be processed by external software filtering.

3.10.1.5.5 Holdover Frequency Offset Read

The offset value, which is acquired by Automatic Slow Averaged, Automatic Fast Averaged and is set by related register bits, can be read from the T0_HOLDOVER_FREQ[23:0] bits by setting the READ_AVG bit and the FAST_AVG bit, as shown in Table 20.

Table 20: Holdover Frequency Offset Read

READ_AVG	FAST_AVG	Offset Value Read from T0_HOLDOVER_FREQ[23:0]
0	don't-care	The value is equal to the one written to.
1	0	The value is acquired by Automatic Slow Averaged method, not equal to the one written to.
	1	The value is acquired by Automatic Fast Averaged method, not equal to the one written to.

The frequency offset in ppm is calculated as follows:

Holdover Frequency Offset (ppm) = T0_HOLDOVER_FREQ[23:0] X 0.000011

3.10.1.6 Pre-Locked2 Mode

In Pre-Locked2 mode, the T0 DPLL output attempts to track the selected input clock.

The Pre-Locked2 mode is a secondary, temporary mode.

3.10.2 T4 DPLL OPERATING MODE

The T4 path is simpler compared with the T0 path.

3.10.2.1 Free-Run Mode

In Free-Run mode, the T4 DPLL output refers to the master clock and is affected by any input clock. The accuracy of the T4 DPLL output is equal to that of the master clock.

3.10.2.2 Locked Mode

In Locked mode, the T4 selected input clock may be locked in the T4 DPLL.

When the T4 selected input clock is locked, the phase and frequency offset of the T4 DPLL output track those of the T4 selected input clock; when unlocked, the phase and frequency offset of the T4 DPLL output attempt to track those of the selected input clock.

The T4 DPLL loop is closed in Locked mode. Its bandwidth and damping factor are set by the T4_DPLL_LOCKED_BW[1:0] bits and the T4_DPLL_LOCKED_DAMPING[2:0] bits respectively.

3.10.2.3 Holdover Mode

In Holdover mode, the T4 DPLL resorts to the stored frequency data acquired in Locked mode to control its output. The T4 DPLL output is not phase locked to any input clock. The T4 DPLL freezes at the operating frequency when it enters Holdover mode. The accuracy is $4.4X10^{-8}$ ppm.

Table 21: Related Bit / Register in Chapter 3.10

Bit	Register	Address (Hex)
CURRENT_PH_DATA[15:0]	CURRENT_DPLL_PHASE[15:8]_STS, CURRENT_DPLL_PHASE[7:0]_STS	69 *, 68 *
CURRENT_DPLL_FREQ[23:0]	CURRENT_DPLL_FREQ[23:16]_STS, CURRENT_DPLL_FREQ[15:8]_STS, CURRENT_DPLL_-FREQ[7:0]_STS	64 *, 63 *, 62 *
T0_DPLL_START_BW[4:0]	T0_DPLL_START_BW_DAMPING_CNFG	56
T0_DPLL_START_DAMPING[2:0]		
T0_DPLL_ACQ_BW[4:0]	T0_DPLL_ACQ_BW_DAMPING_CNFG	57
T0_DPLL_ACQ_DAMPING[2:0]		
T0_DPLL_LOCKED_BW[4:0]	T0_DPLL_LOCKED_BW_DAMPING_CNFG	58
T0_DPLL_LOCKED_DAMPING[2:0]		
AUTO_BW_SEL	T0_BW_OVERSHOOT_CNFG	59
FAST_LOS_SW	PHASE_LOSS_FINE_LIMIT_CNFG	5B *
TEMP_HOLDOVER_MODE[1:0]	T0_HOLDOVER_MODE_CNFG	5C
MAN_HOLDOVER		
AUTO_AVG		
FAST_AVG		
READ_AVG		
T0_HOLDOVER_FREQ[23:0]	T0_HOLDOVER_FREQ[23:16]_CNFG, T0_HOLDOVER_FREQ[15:8]_CNFG, T0_HOLDOVER_-FREQ[7:0]_CNFG	5F, 5E, 5D
T4_DPLL_LOCKED_BW[1:0]	T4_DPLL_LOCKED_BW_DAMPING_CNFG	61
T4_DPLL_LOCKED_DAMPING[2:0]		
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 5B, 62 ~ 64, 68 and 69 registers is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.11 T0 / T4 DPLL OUTPUT

The DPLL output is locked to the selected input clock. According to the phase-compared result of the feedback and the selected input clock, and the DPLL output frequency offset, the PFD output is limited and the DPLL output is frequency offset limited.

3.11.1 PFD OUTPUT LIMIT

The PFD output is limited to be within ±1 UI or within the coarse phase limit (refer to Chapter 3.7.1.2 Coarse Phase Loss), as determined by the MULTI_PH_APP bit.

3.11.2 FREQUENCY OFFSET LIMIT

The DPLL output is limited to be within the DPLL hard limit (refer to Chapter 3.7.1.4 Hard Limit Exceeding).

For T0 DPLL, the integral path value can be frozen when the DPLL hard limit is reached. This function, enabled by the T0_LIMT bit, will minimize the subsequent overshoot when T0 DPLL is pulling in.

3.11.3 PBO (T0 ONLY)

The PBO function is only supported by the T0 path.

When a PBO event is triggered, the phase offset of the selected input clock with respect to the T0 DPLL output is measured. The device then automatically accounts for the measured phase offset and compensates an appropriate phase offset into the DPLL output so that the phase transients on the T0 DPLL output are minimized.

A PBO event is triggered if any one of the following conditions occurs:

- T0 selected input clock switches (the PBO_EN bit is ‘1’);
- T0 DPLL exits from Holdover mode or Free-Run mode (the PBO_EN bit is ‘1’);
- Phase-time changes on the T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds (the PH_MON_PBO_EN bit is ‘1’).

For the first two conditions, the phase transients on the T0 DPLL output are minimized to be no more than 0.61 ns with PBO. The PBO can also be frozen at the current phase offset by setting the PBO_FREZ bit. When the PBO is frozen, the device will ignore any further PBO events triggered by the above two conditions, and maintain the current phase offset. When the PBO is disabled, there may be a phase shift on the T0 DPLL output and the T0 DPLL output tracks back to 0 degree phase offset with respect to the T0 selected input clock.

The last condition is specially for stratum 2 and 3E clocks. The PBO requirement specified in the Telcordia GR-1244-CORE is: ‘Input phase-time changes of 3.5 µs or greater over an interval of less than 0.1 seconds or less shall be built-out by stratum 2 and 3E clocks to reduce the resulting clock phase-time change to less than 50 ns. Phase-time changes of 1.0 µs or less over an interval of 0.1 seconds shall not be built-out.’ Based on this requirement, phase-time changes of more than 1.0 µs but less than 3.5 µs that occur over an interval of less than 0.1 seconds may or may not be built-out.

An integrated Phase Transient Monitor can be enabled by the PH_MON_EN bit to monitor the phase-time changes on the T0 selected input clock. When the phase-time changes are greater than a limit over an interval of less than 0.1 seconds, a PBO event is triggered and the phase transients on the DPLL output are absorbed. The limit is programmed by the PH_TR_MON_LIMT[3:0] bits, and can be calculated as follows:

Limit (ns) = (PH_TR_MON_LIMT[3:0] + 7) X 156

The phase offset induced by PBO will never result in a coarse or fine phase loss.

3.11.4 PHASE OFFSET SELECTION (T0 ONLY)

The phase offset of the T0 selected input clock with respect to the T0 DPLL output can be adjusted. If the device is configured as the Master, the PH_OFFSET_EN bit determines whether the input-to-output phase offset is enabled; if the device is configured as the Slave, the input-to-output phase offset is always enabled. If enabled, the input-to-output phase offset can be adjusted by setting the PH_OFFSET[9:0] bits.

The input-to-output phase offset can be calculated as follows:

Phase Offset (ns) = PH_OFFSET[9:0] X 0.61

3.11.5 FOUR PATHS OF T0 / T4 DPLL OUTPUTS

The T0 DPLL output and the T4 DPLL output are phase aligned with the T0 selected input clock and the T4 selected input clock respectively every 125 µs period. Each DPLL has four output paths.

3.11.5.1 T0 Path

The four paths for T0 DPLL output are as follows:

- 77.76 MHz path - outputs a 77.76 MHz clock;
- 16E1/16T1 path - outputs a 16E1 or 16T1 clock, as selected by the IN_SONET_SDH bit;
- GSM/OBSAI/16E1/16T1 path - outputs a GSM, OBSAI, 16E1 or 16T1 clock, as selected by the T0_GSM_OBSAI_16E1_16T1_SEL[1:0] bits;
- 12E1/24T1/E3/T3 path - outputs a 12E1, 24T1, E3 or T3 clock, as selected by the T0_12E1_24T1_E3_T3_SEL[1:0] bits.

T0 selected input clock is compared with a T0 DPLL output for DPLL locking. The output can only be derived from the 77.76 MHz path or the 16E1/16T1 path. The output path is automatically selected and the output is automatically divided to get the same frequency as the T0 selected input clock.

The T0 DPLL 77.76 MHz output or an 8 kHz signal derived from it can be provided for the T4 DPLL input clock selection (refer to Chapter 3.6 T0 / T4 DPLL Input Clock Selection).

T0 DPLL outputs are provided for T0/T4 APLL or device output process.

3.11.5.2 T4 Path

The four paths for T4 DPLL output are as follows:

- 77.76 MHz path - outputs a 77.76 MHz clock;
- 16E1/16T1 path - outputs a 16E1 or 16T1 clock, as selected by the IN_SONET_SDH bit;
- GSM/GPS/16E1/16T1 path - outputs a GSM, GPS, 16E1 or 16T1 clock, as selected by the T4_GSM_GPS_16E1_16T1_SEL[1:0] bits;
- 12E1/24T1/E3/T3 path - outputs a 12E1, 24T1, E3 or T3 clock, as selected by the T4_12E1_24T1_E3_T3_SEL[1:0] bits.

T4 selected input clock is compared with a T4 DPLL output for DPLL locking. The output can be derived from the 77.76 MHz path or the 16E1/16T1 path. In this case, the output path is automatically selected and the output is automatically divided to get the same frequency as the T4 selected input clock.

In addition, T4 selected input clock is compared with the T0 selected input clock to get the phase difference between T0 and T4 selected input clocks, as determined by the T4_TEST_T0_PH bit.

T4 DPLL outputs are provided for T0/T4 APLL or device output process.

Table 22: Related Bit / Register in Chapter 3.11

Bit	Register	Address (Hex)
MULTI_PH_APP	PHASE_LOSS_COARSE_LIMIT_CNFG	5A *
T0_LIMT	T0_BW_OVERSHOOT_CNFG	59
PBO_EN	MON_SW_PBO_CNFG	0B
PBO_FREZ		
PH_MON_PBO_EN	PHASE_MON_PBO_CNFG	78
PH_MON_EN		
PH_TR_MON_LIMT[3:0]		
PH_OFFSET_EN	PHASE_OFFSET[9:8]_CNFG	7B
PH_OFFSET[9:0]	PHASE_OFFSET[9:8]_CNFG, PHASE_OFFSET[7:0]_CNFG	7B, 7A
IN_SONET_SDH	INPUT_MODE_CNFG	09
T0_GSM_OBSAI_16E1_16T1_SEL[1:0]	T0_DPLL_APLL_PATH_CNFG	55
T0_12E1_24T1_E3_T3_SEL[1:0]		
T4_GSM_GPS_16E1_16T1_SEL[1:0]	T4_DPLL_APLL_PATH_CNFG	60
T4_12E1_24T1_E3_T3_SEL[1:0]		
T4_TEST_T0_PH	T4_INPUT_SEL_CNFG	51
T4_T0_SEL	T4_T0_REG_SEL_CNFG	07

Note: * The setting in the 5A register is either for T0 path or for T4 path, as determined by the T4_T0_SEL bit.

3.12 T0 / T4 APLL

A T0 APLL and a T4 APLL are provided for a better jitter and wander performance of the device output clocks.

The bandwidths of the T0/T4 APLL are set by the T0_APLL_BW[1:0] / T4_APLL_BW[1:0] bits respectively. The lower the bandwidth is, the better the jitter and wander performance of the T0/T4 APLL output are.

The input of the T0/T4 APLL can be derived from one of the T0 and T4 DPLL outputs, as selected by the T0_APLL_PATH[3:0] / T4_APLL_PATH[3:0] bits respectively.

Both the APLL and DPLL outputs are provided for selection for the device output.

Table 23: Related Bit / Register in Chapter 3.12

Bit	Register	Address (Hex)
T0_APLL_BW[1:0]	T0_T4_APLL_BW_CNFG	6A
T4_APLL_BW[1:0]		
T0_APLL_PATH[3:0]	T0_DPLL_APLL_PATH_CNFG	55
T4_APLL_PATH[3:0]	T4_DPLL_APLL_PATH_CNFG	60

3.13 OUTPUT CLOCKS & FRAME SYNC SIGNALS

The device supports 9 output clocks and 2 frame sync output signals altogether.

3.13.1 OUTPUT CLOCKS

The device provides 9 output clocks.

According to the output port technology, the output ports support the following technologies:

- AMI;
- PECL/LVDS;
- CMOS.

OUT1 ~ OUT5 and OUT9 output a CMOS signal.

OUT6 and OUT7 output a PECL or LVDS signal, as selected by the OUT6_PECL_LVDS bit and the OUT7_PECL_LVDS bit respectively.

OUT8 outputs an AMI signal.

The outputs on OUT1 ~ OUT7 are variable, depending on the signals derived from the T0/T4 DPLL and T0/T4 APLL outputs, and the corresponding OUTn_PATH_SEL[3:0] bits ($1 \leq n \leq 7$). The derived signal can be from the T0/T4 DPLL and T0/T4 APLL outputs, as selected by the corresponding OUTn_PATH_SEL[3:0] bits ($1 \leq n \leq 7$). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 24 for the output frequency. If the signal is derived from the T0/T4 APLL output, please refer to Table 25 for the output frequency.

The output on OUT8 is derived from T0 or T4 DPLL 77.76 MHz path, as selected by the OUT8_PATH_SEL bit. After being divided automatically, the output is of 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz, as selected by the 400HZ_SEL bit. Its duty cycle is 50:50 or 5:8, as determined by the AMI_OUT_DUTY bit.

The output on OUT9 is derived from T0 or T4 DPLL 16E1/16T1 path, as selected by the OUT9_PATH_SEL bit. After being divided automatically, the output is of 2.048 MHz or 1.544 MHz, as selected by the IN_SONET_SDH bit.

The outputs on OUT8 and OUT9 can be enabled or disabled, or may be affected by the status of the T4 input clock. It is determined by the OUT8_EN / OUT9_EN and T4_INPUT_FAIL [1] / T4_INPUT_FAIL [2] bits. Refer to Table 26.

The outputs on OUT1 to OUT7 and OUT9 can be inverted, as determined by the corresponding OUTn_INV bit ($1 \leq n \leq 7$ or $n = 9$).

All the output clocks derived from T0/T4 selected input clock are aligned with the T0/T4 selected input clock respectively every 125 µs period.

Table 24: Outputs on OUT1 ~ OUT7 if Derived from T0/T4 DPLL Outputs

OUTn_DIVIDER[3:0] (Output Divider) [1]	outputs on OUT1 ~ OUT7 if derived from T0/T4 DPLL outputs [2]									
	77.76 MHz	12E1	16E1	24T1	16T1	E3	T3	GSM (26 MHz)	OBSAI (30.72 MHz)	GPS (40 MHz)
0000	Output is disabled (output low).									
0001										
0010	77.76 MHz	12E1	16E1	24T1	16T1	E3	T3			
0011		6E1	8E1	12T1	8T1			13 MHz	15.36 MHz	20
0100		3E1	4E1	6T1	4T1					10
0101		2E1		4T1						
0110			2E1	3T1	2T1					5
0111		E1		2T1						
1000			E1		T1					
1001				T1						
1010	64 kHz									
1011	8 kHz									
1100	2 kHz									
1101	400 Hz									
1110	1Hz									
1111	Output is disabled (output high).									

Note:

1. $1 \leq n \leq 7$. Each output is assigned a frequency divider.
2. E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.

Table 25: Outputs on OUT1 ~ OUT7 if Derived from T0/T4 APLL

OUTn_DIVIDER[3:0] (Output Divider) [1]	outputs on OUT1 ~ OUT7 if derived from T0/T4 APLL output [2]									
	77.76 MHz X 4	12E1 X 4	16E1 X 4	24T1 X 4	16T1 X 4	E3	T3	GSM (26 MHz X 2)	OBSAI (30.72 MHz X 10)	GPS (40 MHz)
0000	Output is disabled (output low).									
0001	622.08 MHz [3]									
0010	311.04 MHz [3]	48E1	64E1	96T1	64T1	E3	T3	52 MHz		
0011	155.52 MHz	24E1	32E1	48T1	32T1			26 MHz	153.6 MHz	20 MHz
0100	77.76 MHz	12E1	16E1	24T1	16T1			13 MHz	76.8 MHz	10 MHz
0101	51.84 MHz	8E1		16T1						
0110	38.88 MHz	6E1	8E1	12T1	8T1				38.4 MHz	5 MHz
0111	25.92 MHz	4E1		8T1						
1000	19.44 MHz	3E1	4E1	6T1	4T1					
1001		2E1		4T1					61.44 MHz [4]	
1010			2E1	3T1	2T1				30.72 MHz [4]	
1011	6.48 MHz	E1		2T1					15.36 MHz [4]	
1100			E1		T1				7.68 MHz [4]	
1101				T1					3.84 MHz [4]	
1110										
1111	Output is disabled (output high).									

Note:

1. 1 ≤ n ≤ 7. Each output is assigned a frequency divider.
2. In the APLL, the selected T0/T4 DPLL output may be multiplied. E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.
3. The 622.08 MHz and 311.04 MHz differential signals are only output on OUT6 and OUT7.
4. The 61.44 MHz, 30.72 MHz, 15.36 MHz, 7.68 MHz and 3.84 MHz outputs are only derived from T0 APLL.

Table 26: Outputs on OUT8 & OUT9

OUT8_EN / OUT9_EN	T4_INPUT_FAIL [1] / T4_INPUT_FAIL [2]	Outputs on OUT8 & OUT9
0	don’t-care	Output is disabled (output low).
1	0	Output is enabled.
	1	Output is enabled when the T4 selected input clock does not fail. Output is disabled (output low) when the T4 selected input clock fails.

3.13.2 FRAME SYNC OUTPUT SIGNALS

An 8 kHz and a 2 kHz frame sync signals are output on the FRSYNC_8K and MFRSYNC_2K pins if enabled by the 8K_EN and 2K_EN bits respectively. They are CMOS outputs.

The two frame sync signals are derived from the T0 APLL output and are aligned with the output clock. They can be synchronized to the frame sync input signal.

If the frame sync input signal with respect to the T0 selected input clock is above a limit set by the SYNC_MON_LIMT[2:0] bits, an external sync alarm will be raised and EX_SYNC1 is disabled to synchronize the frame sync output signals. The external sync alarm is cleared once EX_SYNC1 with respect to the T0 selected input clock is within the limit. If it is within the limit, whether EX_SYNC1 is enabled to synchronize the frame sync output signal is determined by the AUTO_EXT_SYNC_EN bit and the EXT_SYNC_EN bit. Refer to Table 27 for details.

When the frame sync input signal is enabled to synchronize the frame sync output signal, it should be adjusted to align itself with the T0 selected input clock. Nominally, the falling edge of EX_SYNC1 is aligned with the rising edge of the T0 selected input clock. EX_SYNC1 may be 0.5 UI early/late or 1 UI late due to the circuit and board wiring delays. Setting the sampling of EX_SYNC1 by the SYNC_PH1[1:0] bits will compensate this early/late. Refer to Figure 9 to Figure 12.

The EX_SYNC_ALARM_MON bit indicates whether EX_SYNC1 is in external sync alarm status. The external sync alarm is indicated by the EX_SYNC_ALARM [1] bit. If the EX_SYNC_ALARM [2] bit is '1', the occurrence of the external sync alarm will trigger an interrupt.

The 8 kHz and the 2 kHz frame sync output signals can be inverted by setting the 8K_INV and 2K_INV bits respectively. The frame sync outputs can be 50:50 duty cycle or pulsed, as determined by the 8K_PUL and 2K_PUL bits respectively. When they are pulsed, the pulse width is defined by the period of OUT3; and they are pulsed on the position of the falling or rising edge of the standard 50:50 duty cycle, as selected by the 2K_8K_PUL_POSITION bit.

Table 27: Synchronization Control

AUTO_EXT_SYNC_EN	EXT_SYNC_EN	Synchronization
don't-care	0	Disabled
0	1	Enabled
1	1	Enabled if the T0 selected input clock is IN11; otherwise, disabled.

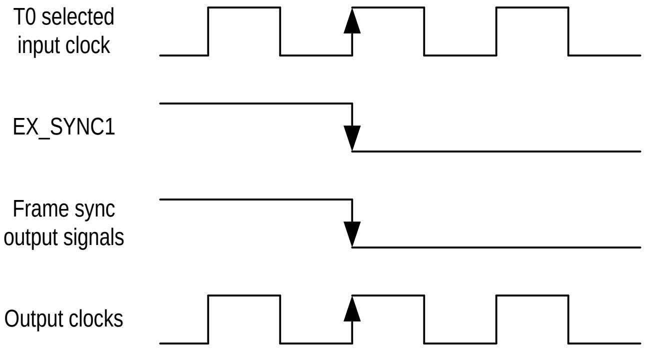


Figure 9. On Target Frame Sync Input Signal Timing

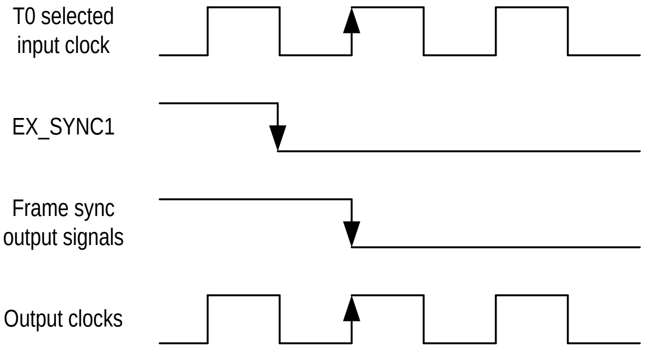


Figure 10. 0.5 UI Early Frame Sync Input Signal Timing

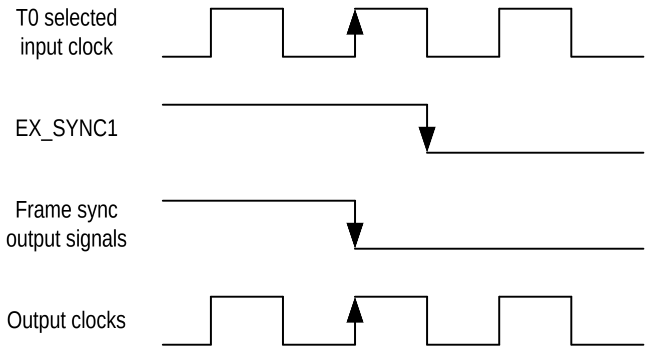


Figure 11. 0.5 UI Late Frame Sync Input Signal Timing

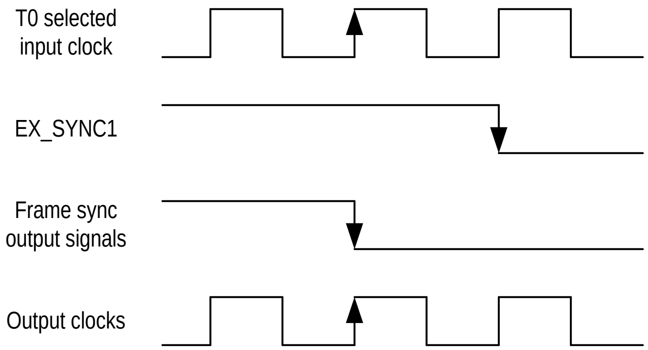


Figure 12. 1 UI Late Frame Sync Input Signal Timing

Table 28: Related Bit / Register in Chapter 3.13

Bit	Register	Address (Hex)
OUT6_PECL_LVDS	DIFFERENTIAL_IN_OUT_OSCI_CNFG	0A
OUT7_PECL_LVDS		
OUTn_PATH_SEL[3:0] (1 ≤ n ≤ 7)	OUT1_FREQ_CNFG ~ OUT7_FREQ_CNFG	6B ~ 71
OUTn_DIVIDER[3:0] (1 ≤ n ≤ 7)		
OUT8_PATH_SEL	OUT8_FREQ_CNFG	72
400HZ_SEL		
AMI_OUT_DUTY		
T4_INPUT_FAIL [1]		
OUT8_EN		
OUT9_PATH_SEL	OUT9_FREQ_CNFG	73
OUT9_EN		
T4_INPUT_FAIL [2]		
IN_SONET_SDH	INPUT_MODE_CNFG	09
AUTO_EXT_SYNC_EN		
EXT_SYNC_EN		
OUTn_INV (1 ≤ n ≤ 7 or n = 9)	OUT9_FREQ_CNFG, OUT8_FREQ_CNFG	73, 72
8K_EN	FR_MFR_SYNC_CNFG	74
2K_EN		
8K_INV		
2K_INV		
8K_PUL		
2K_PUL		
2K_8K_PUL_POSITION		
SYNC_MON_LIMT[2:0]	SYNC_MONITOR_CNFG	7C
SYNC_PH1[1:0]	SYNC_PHASE_CNFG	7D
EX_SYNC_ALARM_MON	OPERATING_STS	52
EX_SYNC_ALARM [1]	INTERRUPTS3_STS	0F
EX_SYNC_ALARM [2]	INTERRUPTS3_ENABLE_CNFG	12

3.14 MASTER / SLAVE CONFIGURATION

Master / Slave configuration is only supported by the T0 path of the device.

Two devices should be used together in order to:

- Enable system protection against single chip failure;
- Guarantee no service interrupt during system maintenance, such as software or hardware upgrade.

Of the two devices, one is configured as the Master and the other is configured as the Slave. The configuration is made by the MS/$\overline{\text{SL}}$ pin and the MS_SL_CTRL bit (b0, 13H), as shown in Table 29:

Table 29: Device Master / Slave Control

Master / Slave Control		Result
MS/$\overline{\text{SL}}$ pin	MS_SL_CTRL Bit	
High	0	Master
	1	Slave
Low	0	Slave
	1	Master

In this application, all the output clocks derived from the T0 selected input clock and the frame sync output signals from the two devices are at the same frequency offset and phase. Refer to Chapter 3.13.2 Frame SYNC Output Signals for details.

The difference between the Master and the Slave is: in the Master, the IN11 should not be selected by the T0 DPLL; in the Slave, the following functions are automatically forced:

- The T0 selected input clock is IN11;
- T0 PBO is disabled;
- T0 DPLL operates at the acquisition bandwidth and damping factor;
- EX_SYNC1 is used for synchronization;
- T0 DPLL operates in Locked mode.

In the Slave, the corresponding registers of the above forced functions can still be configured, but their configuration does not take any effect. The frequency of the T0 selected input clock IN11 is recommended to be 6.48 MHz.

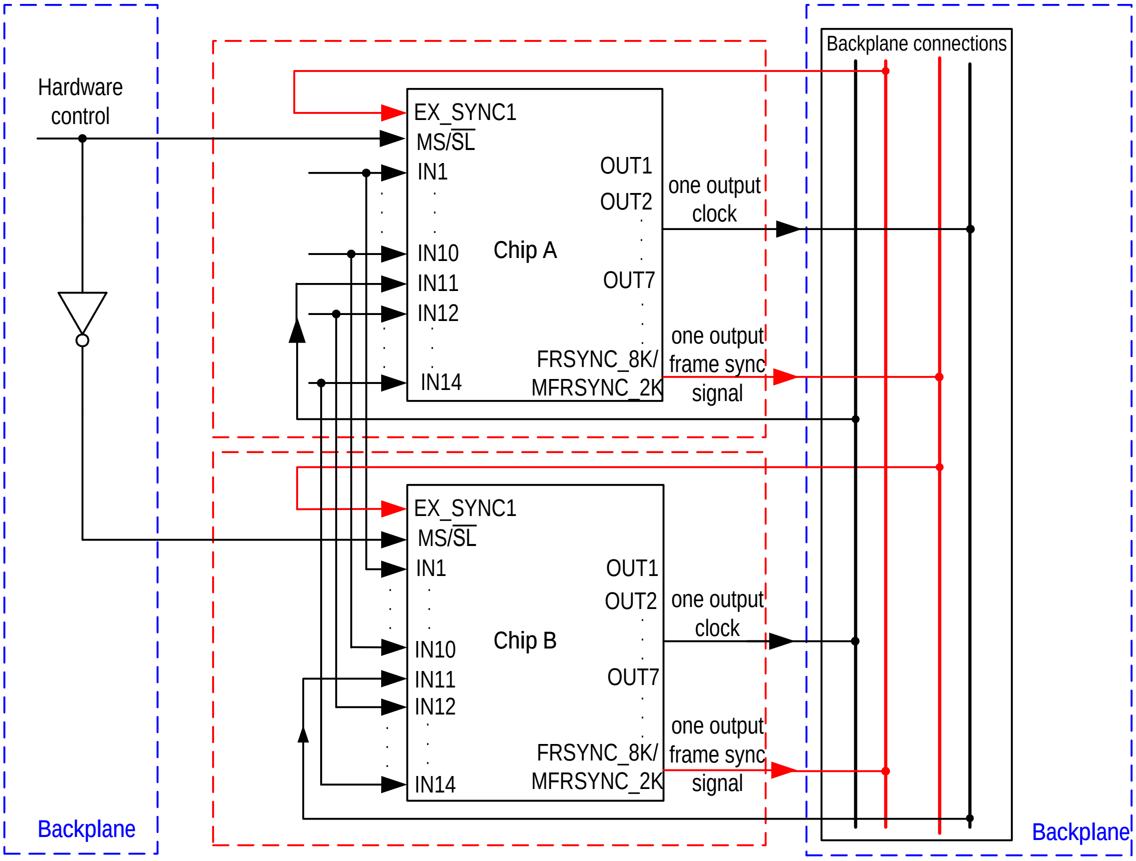


Figure 13. Physical Connection Between Two Devices

3.15 INTERRUPT SUMMARY

The interrupt sources of the device are as follows:

- AMI violation
- LOS
- T4 DPLL locking status change
- Input clocks for T0 path validity change
- T0 selected input clock fail
- Input clocks for T4 path change to be no qualified input clock available
- T0 DPLL operating mode switch
- External sync alarm

All of the above interrupt events are indicated by the corresponding interrupt status bit. If the corresponding interrupt enable bit is set, any of the interrupts can be reported by the INT_REQ pin. The output characteristics on the INT_REQ pin are determined by the HZ_EN bit and the INT_POL bit.

Interrupt events are cleared by writing a '1' to the corresponding interrupt status bit. The INT_REQ pin will be inactive only when all the pending enabled interrupts are cleared.

In addition, the interrupt of T0 selected input clock fail can be reported by the TDO pin, as determined by the LOS_FLAG_TO_TDO bit.

Table 30: Related Bit / Register in Chapter 3.15

Bit	Register	Address (Hex)
HZ_EN	INTERRUPT_CNFG	0C
INT_POL		
LOS_FLAG_TO_TDO	MON_SW_PBO_CNFG	0B

3.16 T0 AND T4 SUMMARY

The main features supported by the T0 path are as follows:

- Phase lock alarm;
- Forced or Automatic input clock selection/switch;
- 3 primary and 3 secondary, temporary DPLL operating modes, switched automatically or under external control;
- Automatic switch between starting, acquisition and locked bandwidths/damping factors;
- Programmable DPLL bandwidths from 0.5 mHz to 560 Hz in 19 steps;
- Programmable damping factors: 1.2, 2.5, 5, 10 and 20;
- Fast loss, coarse phase loss, fine phase loss and hard limit exceeding monitoring;
- Output phase and frequency offset limited;
- Automatic Instantaneous, Automatic Slow Averaged, Automatic Fast Averaged or Manual holdover frequency offset acquiring;
- PBO to minimize output phase transients;
- Programmable output phase offset;
- Low jitter multiple clock outputs with programmable polarity;
- Low jitter 2 kHz and 8 kHz frame sync signal outputs with programmable pulse width and polarity;
- Master / Slave application to enable system protection against single device failure.

The main features supported by the T4 path are as follows:

- Forced or Automatic input clock selection/switch;
- Locking to T0 DPLL output;
- 3 DPLL operating modes, switched automatically or under external control;
- Programmable DPLL bandwidth: 18 Hz, 35 Hz, 70 Hz and 560 Hz;
- Programmable damping factor: 1.2, 2.5, 5, 10 and 20;
- Fast loss, coarse phase loss, fine phase loss and hard limit exceeding monitoring;
- Output phase and frequency offset limited;
- Automatic Instantaneous holdover frequency offset;
- Low jitter multiple clock outputs with programmable polarity.

3.17 POWER SUPPLY FILTERING TECHNIQUES

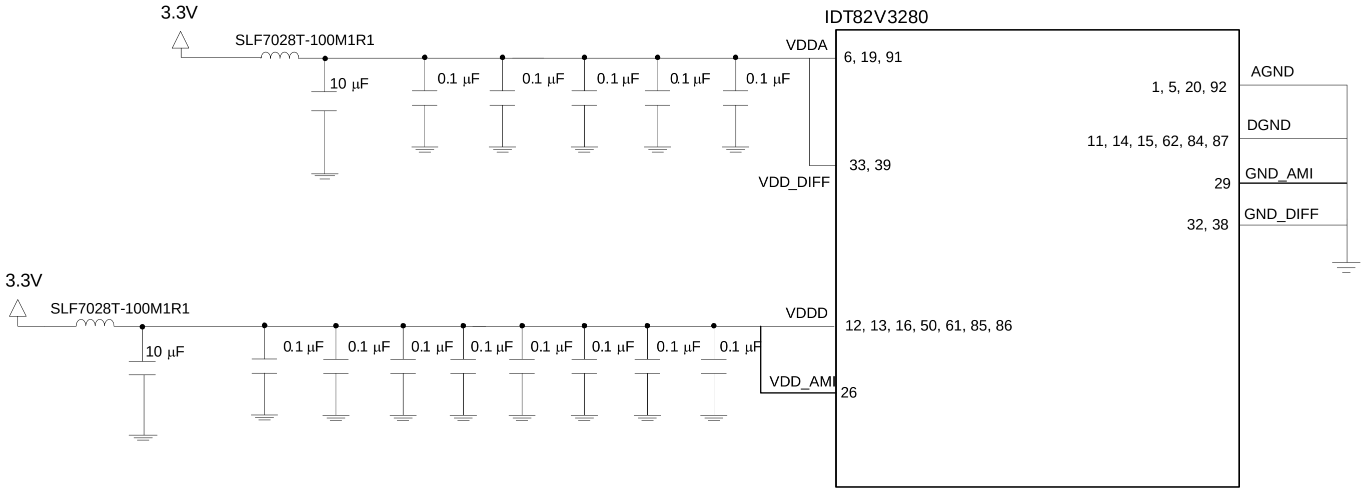


Figure 14. IDT82V3280 Power Decoupling Scheme

To achieve optimum jitter performance, power supply filtering is required to minimize supply noise modulation of the output clocks. The common sources of power supply noise are switch power supplies and the high switching noise from the outputs to the internal PLL. The IDT82V3280 provides separate VDDA power pins for the internal analog PLL, VDD_DIFF for the differential output driver circuit and VDDD pins for the core logic as well as I/O driver circuits.

To minimize switching power supply noise generated by the switching regulator, the power supply output should be filtering with sufficient bulk capacity to minimize ripple and 0.1 uF (0402 case size, ceramic) caps to filter out the switching transients.

For the IDT82V3280, the decoupling for VDDA, VDD_DIFF, VDD_AMI and VDDD are handled individually. VDDD, VDD_AMI, VDD_DIFF and VDDA should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. Figure 14 illustrated how bypass capacitor and ferrite bead should be connected to power pins.

The analog power supply VDDA and VDD_DIFF should have low impedance. This can be achieved by using one 10 uF (1210 case size, ceramic) and at least four 0.1 uF (0402 case size, ceramic) capacitors in parallel. The 0.1 uF (0402 case size, ceramic) capacitors must be placed right next to the VDDA and VDD_DIFF pins as close as possible. Note that the 10 uF capacitor must be of 1210 case size, and it must be ceramic for lowest ESR (Effective Series Resistance) possible. The 0.1 uF should be of case size 0402, this offers the lowest ESL (Effective Series Inductance) to achieve low impedance towards the high speed range.

For VDDD and VDD_AMI, at least ten 0.1 uF (0402 case size, ceramic) and one 10 uF (1210 case size, ceramic) capacitors are recommended. The 0.1 uF capacitors should be placed as close to the VDDD pins as possible.

Please refer to evaluation board schematic for details.

4 TYPICAL APPLICATION

The device supports Master / Slave application, as shown in Figure 15:

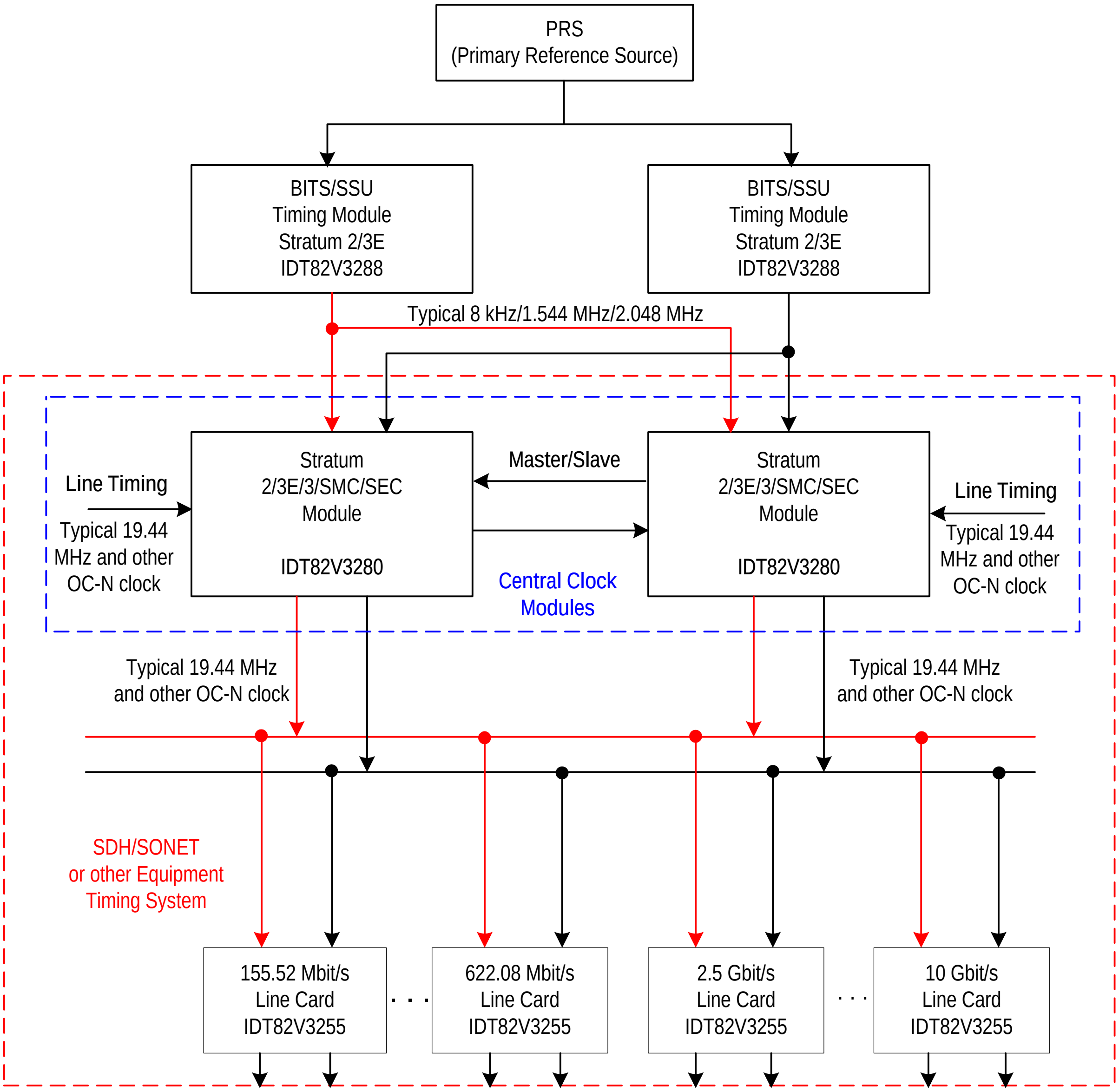


Figure 15. Typical Application

4.1 MASTER / SLAVE APPLICATION

Master / Slave application is only supported by the T0 path of the device.

In Master / Slave application, two devices should be used together. Of the two devices, one is configured as the Master and the other is configured as the Slave. Refer to Chapter 3.14 Master / Slave Configuration for details.

5 MICROPROCESSOR INTERFACE

The microprocessor interface provides access to read and write the registers in the device. The microprocessor interface supports the following five modes:

- EPROM mode;
- Multiplexed mode;
- Intel mode;
- Motorola mode;
- Serial mode.

The microprocessor interface mode is selected by the MPU_SEL_CNFG[2:0] bits (b2~0, 7FH). The interface pins in different interface modes are listed in Table 31:

Table 31: Microprocessor Interface

MPU_SEL_CNFG[2:0] bits	Microprocessor Interface Mode	Interface Pins
001	ERPOM	$\overline{\text{CS}}$, A[6:0], AD[7:0]
010	Multiplexed	$\overline{\text{CS}}$, ALE, $\overline{\text{WR}}$, $\overline{\text{RD}}$, AD[7:0], RDY
011	Intel	$\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{RD}}$, A[6:0], AD[7:0], RDY
100	Motorola	$\overline{\text{CS}}$, $\overline{\text{WR}}$, A[6:0], AD[7:0], RDY
101	Serial	$\overline{\text{CS}}$, SCLK, SDI, SDO, CLKE

5.1 EPROM MODE

In this mode, the device is used with an EPROM. The configuration data will be automatically read from the EPROM after the device is powered on.

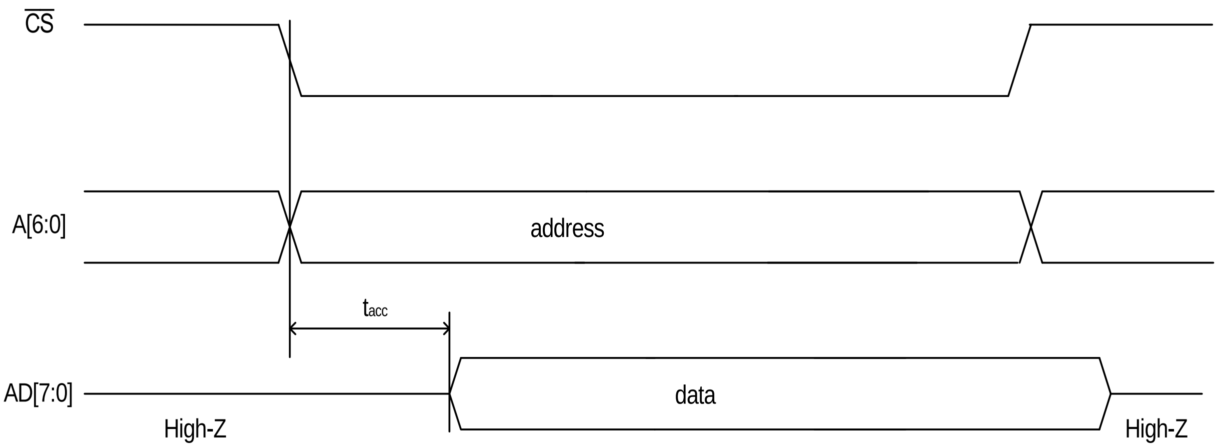


Figure 16. EPROM Access Timing Diagram

Table 32: Access Timing Characteristics in EPROM Mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{acc}	$\overline{CS}$ to valid data delay time			920	ns

5.2 MULTIPLEXED MODE

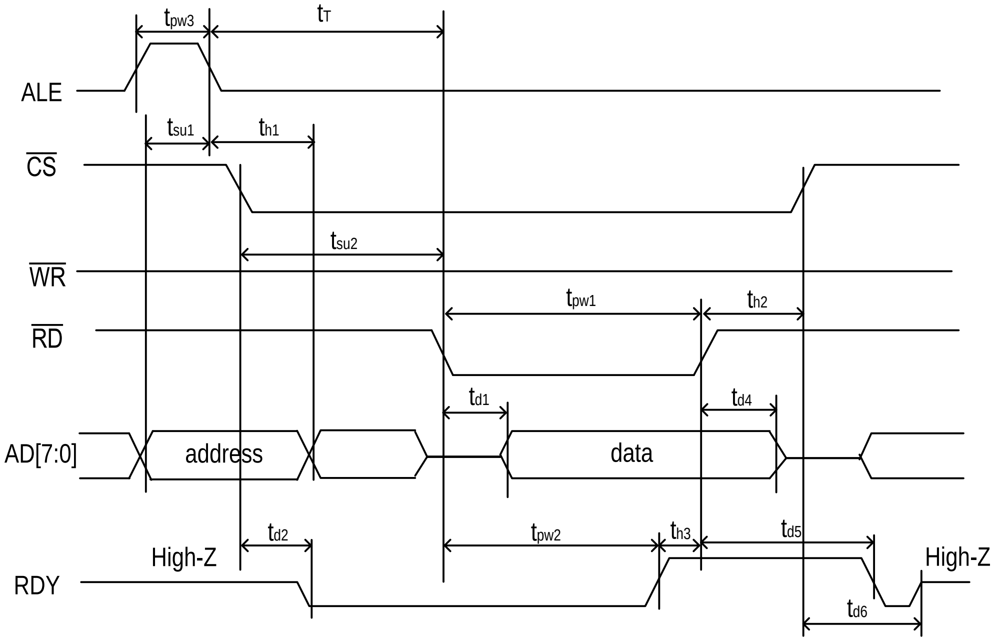


Figure 17. Multiplexed Read Timing Diagram

Table 33: Read Timing Characteristics in Multiplexed Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to ALE falling edge setup time	2			ns
t_{su2}	Valid $\overline{CS}$ to Valid $\overline{RD}$ setup time	0			ns
t_{d1}	Valid $\overline{RD}$ to valid data delay time			3.5T + 10	ns
t_{d2}	Valid $\overline{CS}$ to valid RDY delay time		13		ns
t_{d4}	$\overline{RD}$ rising edge to AD[7:0] high impedance delay time		10		ns
t_{d5}	$\overline{RD}$ rising edge to RDY low delay time		13		ns
t_{d6}	$\overline{CS}$ rising edge to RDY release delay time		13		ns
t_{pw1}	Valid $\overline{RD}$ pulse width low	4.5T + 10 *			ns
t_{pw2}	Valid RDY pulse width low	4.5T + 10			ns
t_{pw3}	Valid ALE pulse width high	2			ns
t_{h1}	Valid address after ALE falling edge hold time	3			ns
t_{h2}	Valid $\overline{CS}$ after $\overline{RD}$ rising edge hold time	0			ns
t_{h3}	Valid $\overline{RD}$ after RDY rising edge hold time	0			ns
t_T	Time between ALE falling edge and $\overline{RD}$ falling edge	0			ns
t_{TI}	Time between consecutive Read-Read or Read-Write accesses ($\overline{RD}$ rising edge to ALE rising edge)	>T			ns

Note:
* Timing with RDY. If RDY is not used, t_{pw1} is 3.5T + 10.

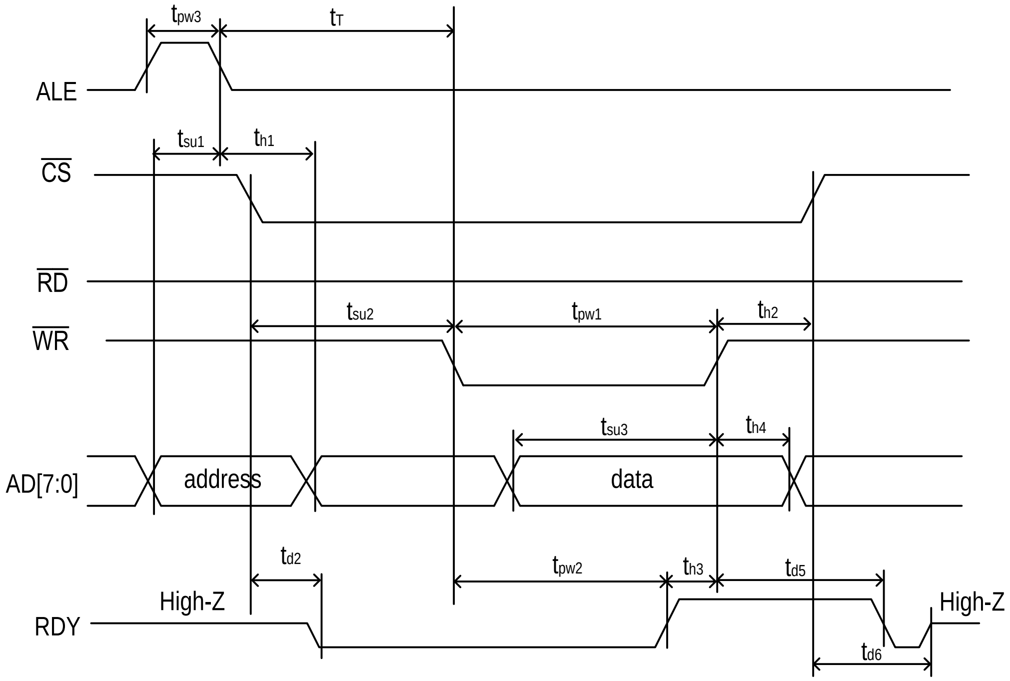


Figure 18. Multiplexed Write Timing Diagram

Table 34: Write Timing Characteristics in Multiplexed Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to ALE falling edge setup time	2			ns
t_{su2}	Valid $\overline{CS}$ to valid $\overline{WR}$ setup time	0			ns
t_{su3}	Valid data to $\overline{WR}$ rising edge setup time	3			ns
t_{d2}	Valid $\overline{CS}$ to valid RDY delay time		13		ns
t_{d5}	$\overline{WR}$ rising edge to RDY low delay time		13		ns
t_{d6}	$\overline{CS}$ rising edge to RDY release delay time		13		ns
t_{pw1}	Valid $\overline{WR}$ pulse width low	1.5T + 10			ns
t_{pw2}	Valid RDY pulse width low	1.5T + 10			ns
t_{pw3}	Valid ALE pulse width high	2			ns
t_{h1}	Valid address after ALE falling edge hold time	3			ns
t_{h2}	Valid $\overline{CS}$ after $\overline{WR}$ rising edge hold time	0			ns
t_{h3}	Valid $\overline{WR}$ after RDY rising edge hold time	0			ns
t_{h4}	Valid data after $\overline{WR}$ rising edge hold time	9			ns
t_T	Time between ALE falling edge and $\overline{WR}$ falling edge	0			ns
t_{TI}	Time between consecutive Write-Read or Write-Write accesses ($\overline{WR}$ rising edge to ALE rising edge)	>7T			ns

5.3 INTEL MODE

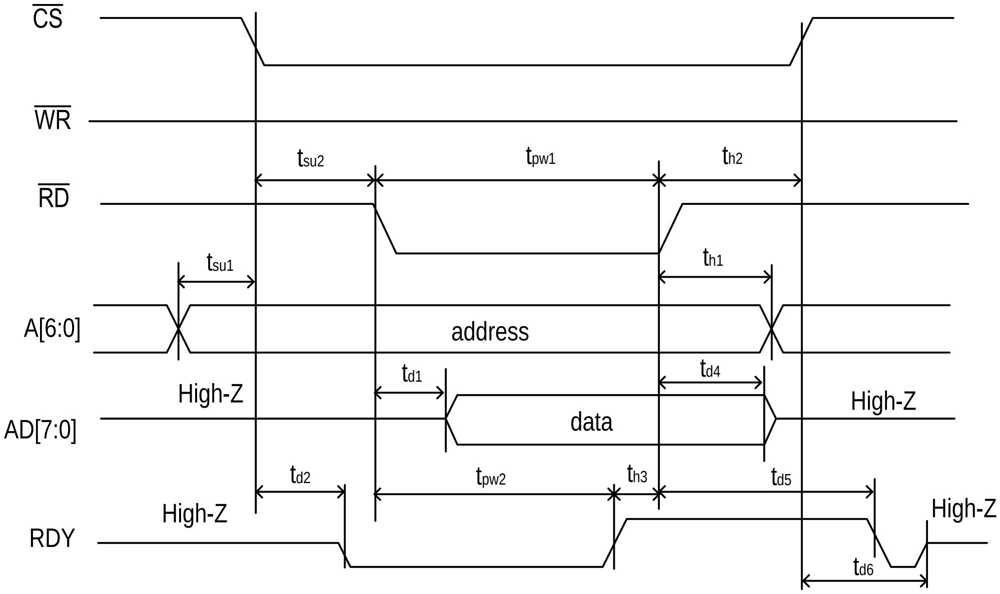


Figure 19. Intel Read Timing Diagram

Table 35: Read Timing Characteristics in Intel Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to valid $\overline{CS}$ setup time	0			ns
t_{su2}	Valid $\overline{CS}$ to valid $\overline{RD}$ setup time	0			ns
t_{d1}	Valid $\overline{RD}$ to valid data delay time			3.5T + 10	ns
t_{d2}	Valid $\overline{CS}$ to valid RDY delay time		13		ns
t_{d4}	$\overline{RD}$ rising edge to AD[7:0] high impedance delay time		10		ns
t_{d5}	$\overline{RD}$ rising edge to RDY low delay time		13		ns
t_{d6}	$\overline{CS}$ rising edge to RDY release delay time		13		ns
t_{pw1}	Valid $\overline{RD}$ pulse width low	4.5T + 10 *			ns
t_{pw2}	Valid RDY pulse width low	4.5T + 10			ns
t_{h1}	Valid address after $\overline{RD}$ rising edge hold time	0			ns
t_{h2}	Valid $\overline{CS}$ after $\overline{RD}$ rising edge hold time	0			ns
t_{h3}	Valid $\overline{RD}$ after RDY rising edge hold time	0			ns
t_{TI}	Time between consecutive Read-Read or Read-Write accesses ($\overline{RD}$ rising edge to $\overline{RD}$ falling edge, or $\overline{RD}$ rising edge to $\overline{WR}$ falling edge)	>T			ns

Note:
* Timing with RDY. If RDY is not used, t_{pw1} is 3.5T + 10.

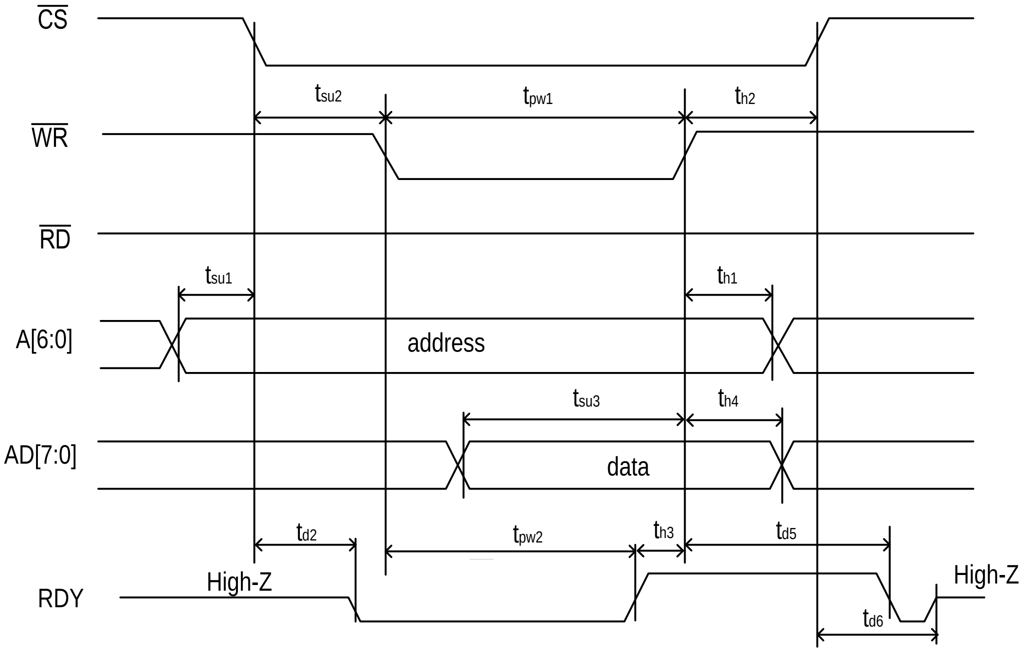


Figure 20. Intel Write Timing Diagram

Table 36: Write Timing Characteristics in Intel Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to valid $\overline{CS}$ setup time	0			ns
t_{su2}	Valid $\overline{CS}$ to valid $\overline{WR}$ setup time	0			ns
t_{su3}	Valid data before $\overline{WR}$ rising edge setup time	3			ns
t_{d2}	Valid $\overline{CS}$ to valid RDY delay time		13		ns
t_{d5}	$\overline{WR}$ rising edge to RDY low delay time		13		ns
t_{d6}	$\overline{CS}$ rising edge to RDY release delay time		13		ns
t_{pw1}	Valid $\overline{WR}$ pulse width low	1.5T + 10			ns
t_{pw2}	Valid RDY pulse width low	1.5T + 10			ns
t_{h1}	Valid address after $\overline{WR}$ rising edge hold time	0			ns
t_{h2}	Valid $\overline{CS}$ after $\overline{WR}$ rising edge hold time	0			ns
t_{h3}	Valid $\overline{WR}$ after RDY rising edge hold time	0			ns
t_{h4}	Valid data after $\overline{WR}$ rising edge hold time	9			ns
t_{TI}	Time between consecutive Write-Read or Write-Write accesses ($\overline{WR}$ rising edge to $\overline{WR}$ falling edge, or $\overline{WR}$ rising edge to $\overline{RD}$ falling edge)	>7T			ns

5.4 MOTOROLA MODE

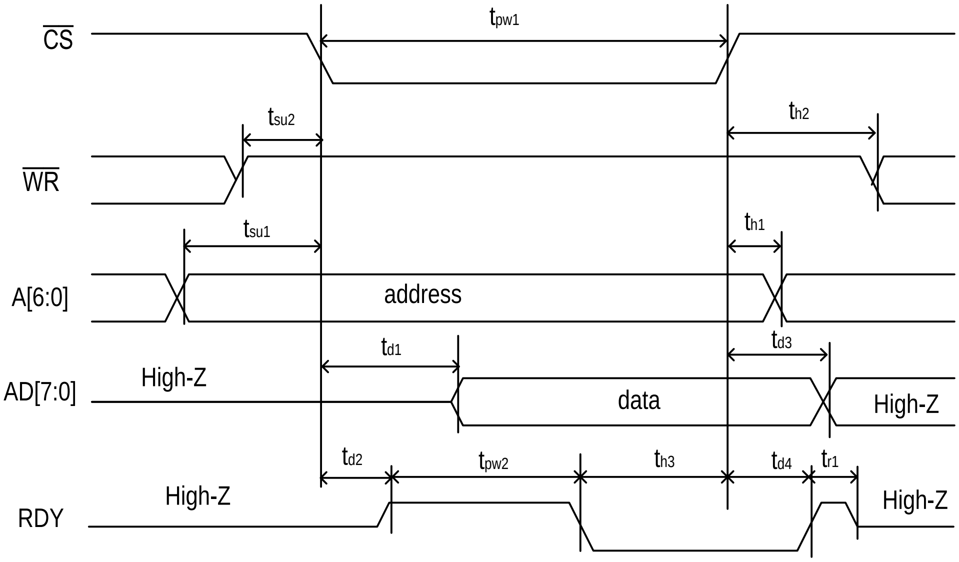


Figure 21. Motorola Read Timing Diagram

Table 37: Read Timing Characteristics in Motorola Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to valid $\overline{CS}$ setup time	0			ns
t_{su2}	Valid $\overline{WR}$ to valid $\overline{CS}$ setup time	0			ns
t_{d1}	Valid $\overline{CS}$ to valid data delay time			3.5T + 10	ns
t_{d2}	Valid $\overline{CS}$ to valid RDY delay time		13		ns
t_{d3}	$\overline{CS}$ rising edge to AD[7:0] high impedance delay time		10		ns
t_{d4}	$\overline{CS}$ rising edge to RDY release delay time		13		ns
t_{pw1}	Valid $\overline{CS}$ pulse width low	4.5T + 10 *			ns
t_{pw2}	Valid RDY pulse width high	4.5T + 10			ns
t_{h1}	Valid address after $\overline{CS}$ rising edge hold time	0			ns
t_{h2}	Valid $\overline{WR}$ after $\overline{CS}$ rising edge hold time	0			ns
t_{h3}	Valid $\overline{CS}$ after RDY falling edge hold time	0			ns
t_{r1}	RDY release time		3		ns
t_{TI}	Time between consecutive Read-Read or Read-Write accesses ($\overline{CS}$ rising edge to $\overline{CS}$ falling edge)	> T			ns

Note:
* Timing with RDY. If RDY is not used, t_{pw1} is 3.5T +10.

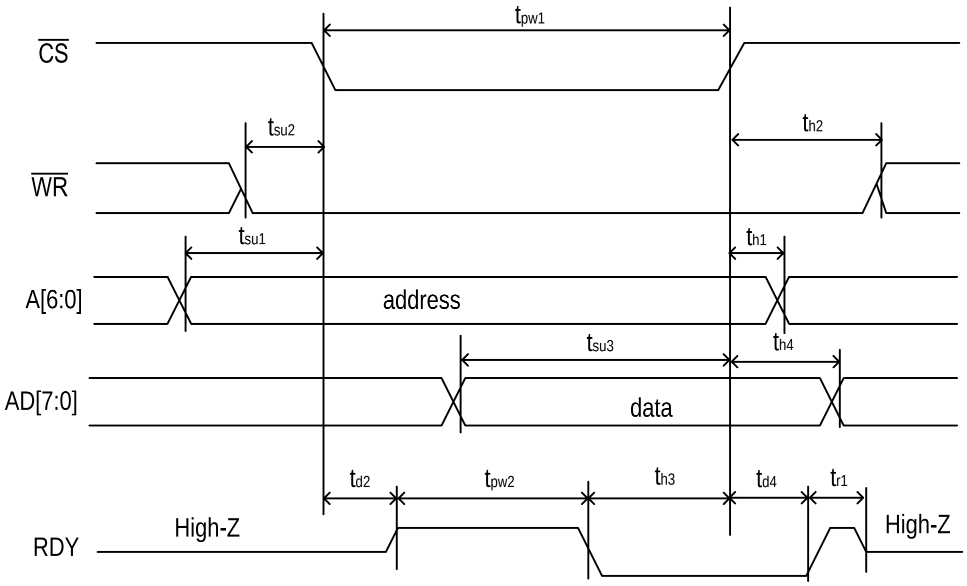


Figure 22. Motorola Write Timing Diagram

Table 38: Write Timing Characteristics in Motorola Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid address to valid $\overline{CS}$ setup time	0			ns
t_{su2}	Valid $\overline{WR}$ to valid $\overline{CS}$ setup time	0			ns
t_{su3}	Valid data before $\overline{CS}$ rising edge setup time	3			ns
t_{d2}	Valid $\overline{CS}$ to valid RDY delay time		13		ns
t_{d4}	$\overline{CS}$ rising edge to RDY release delay time		13		ns
t_{pw1}	Valid $\overline{CS}$ pulse width low	1.5T + 10			ns
t_{pw2}	Valid RDY pulse width high	1.5T + 10			ns
t_{h1}	Valid address after valid $\overline{CS}$ rising edge hold time	0			ns
t_{h2}	Valid $\overline{WR}$ after valid $\overline{CS}$ rising edge hold time	0			ns
t_{h3}	Valid $\overline{CS}$ after RDY falling edge hold time	0			ns
t_{h4}	Valid data after valid $\overline{CS}$ rising edge hold time	9			ns
t_{r1}	RDY release time		3		ns
t_{TI}	Time between consecutive Write-Write or Write-Read accesses ($\overline{CS}$ rising edge to $\overline{CS}$ falling edge)	> 7T			ns

5.5 SERIAL MODE

In a read operation, the active edge of SCLK is selected by CLKE. When CLKE is asserted low, data on SDO will be clocked out on the rising edge of SCLK. When CLKE is asserted high, data on SDO will be clocked out on the falling edge of SCLK.

In a write operation, data on SDI will be clocked in on the rising edge of SCLK.

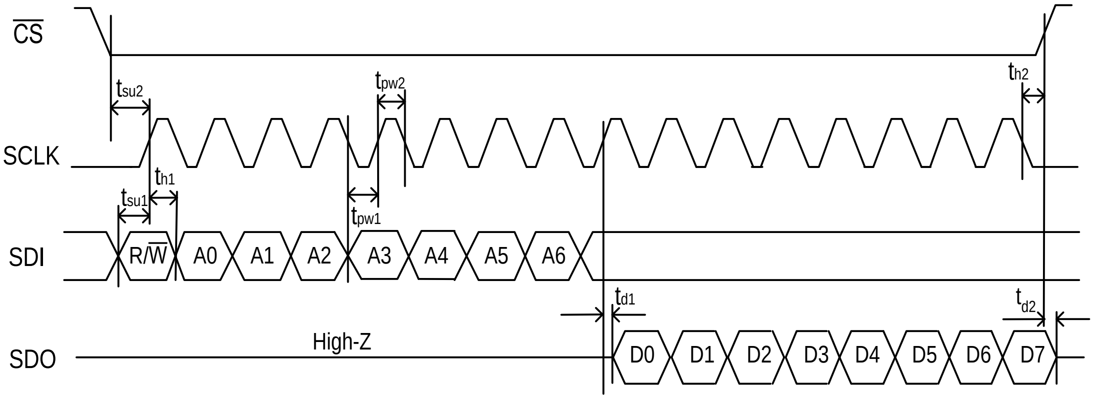


Figure 23. Serial Read Timing Diagram (CLKE Asserted Low)

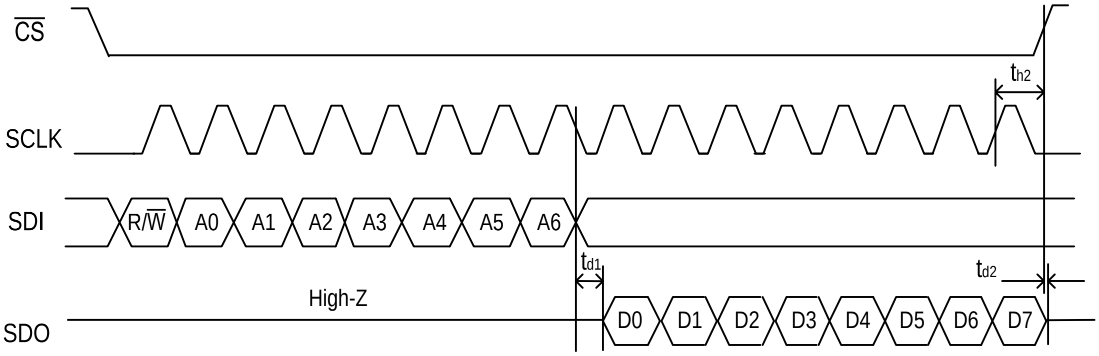


Figure 24. Serial Read Timing Diagram (CLKE Asserted High)

Table 39: Read Timing Characteristics in Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid SDI to valid SCLK setup time	4			ns
t_{su2}	Valid $\overline{CS}$ to valid SCLK setup time	14			ns
t_{d1}	Valid SCLK to valid data delay time		10		ns
t_{d2}	$\overline{CS}$ rising edge to SDO high impedance delay time		10		ns
t_{pw1}	SCLK pulse width low	3.5T + 5			ns
t_{pw2}	SCLK pulse width high	3.5T + 5			ns
t_{h1}	Valid SDI after valid SCLK hold time	6			ns
t_{h2}	Valid $\overline{CS}$ after valid SCLK hold time (CLKE = 0/1)	5			ns
t_{TI}	Time between consecutive Read-Read or Read-Write accesses ($\overline{CS}$ rising edge to $\overline{CS}$ falling edge)	10			ns

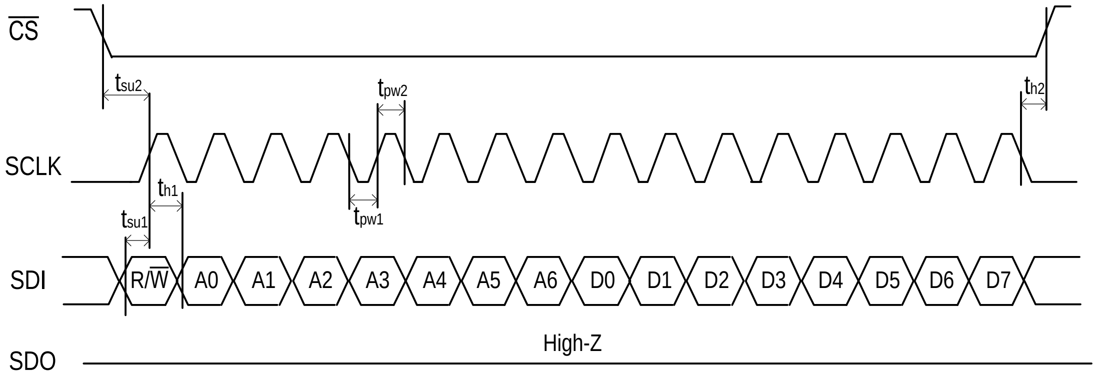


Figure 25. Serial Write Timing Diagram

Table 40: Write Timing Characteristics in Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid SDI to valid SCLK setup time	4			ns
t_{su2}	Valid $\overline{CS}$ to valid SCLK setup time	14			ns
t_{pw1}	SCLK pulse width low	3.5T			ns
t_{pw2}	SCLK pulse width high	3.5T			ns
t_{h1}	Valid SDI after valid SCLK hold time	6			ns
t_{h2}	Valid $\overline{CS}$ after valid SCLK hold time	5			ns
t_{TI}	Time between consecutive Write-Write or Write-Read accesses ($\overline{CS}$ rising edge to $\overline{CS}$ falling edge)	10			ns

6 JTAG

This device is compliant with the IEEE 1149.1 Boundary Scan standard except the following:

- The output boundary scan cells do not capture data from the core and the device does not support EXTEST instruction;
- The $\overline{\text{TRST}}$ pin is set low by default and JTAG is disabled in order to be consistent with other manufacturers.

The JTAG interface timing diagram is shown in Figure 26.

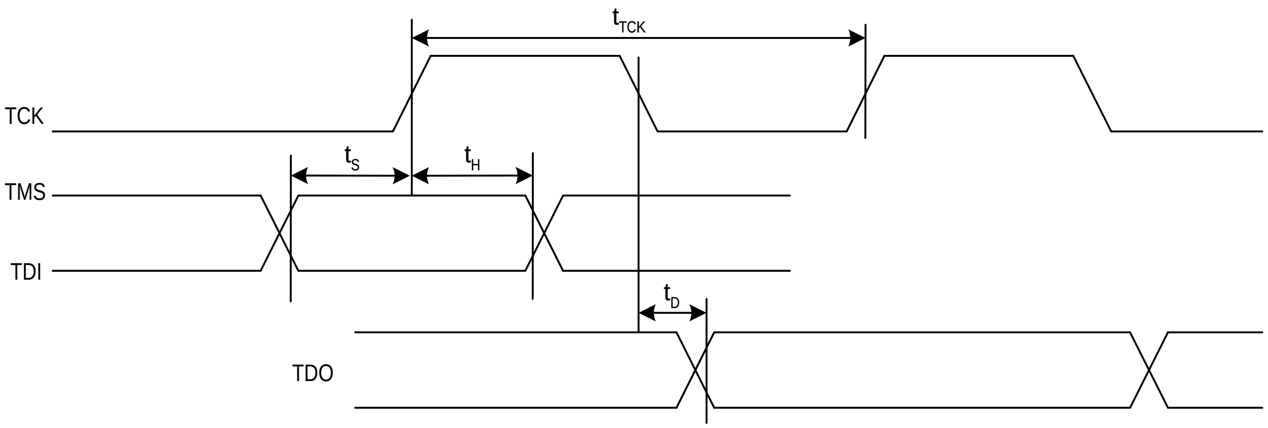


Figure 26. JTAG Interface Timing Diagram

Table 41: JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{TCK}	TCK period	100			ns
t_S	TMS / TDI to TCK setup time	25			ns
t_H	TCK to TMS / TDI Hold Time	25			ns
t_D	TCK to TDO delay time			50	ns

7 PROGRAMMING INFORMATION

After reset, all the registers are set to their default values. The registers are read or written via the microprocessor interface.

Before any write operation, the value in register PROTECTION_CNFG is recommended to be confirmed to make sure whether the write operation is enabled. The device provides 3 register protection modes:

- Protected mode: no other registers can be written except register PROTECTION_CNFG itself;
- Fully Unprotected mode: all the writable registers can be written;
- Single Unprotected mode: one more register can be written besides register PROTECTION_CNFG. After write operation (not including writing a '1' to clear a bit to '0'), the device automatically switches to Protected mode.

Writing '0' to the registers will take no effect if the registers are cleared by writing '1'.

T0 and T4 paths share some registers, whose addresses are 26H ~ 2CH, 4EH, 4FH, 5AH, 5BH, 62H ~ 64H, 68H and 69H. The names of shared registers are marked with a *. Before register read/write operation, register T4_T0_REG_SEL_CNFG is recommended to be confirmed to make sure whether the register operation is available for T0 or T4 path.

The access of the Multi-word Registers is different from that of the Single-word Registers. Take the registers (04H, 05H and 06H) for an example, the write operation for the Multi-word Registers follows a fixed sequence. The register (04H) is configured first and the register (06H) is configured last. The three registers are configured continuously and should not be interrupted by any operation. The crystal calibration configuration will take effect after all the three registers are configured. During read operation, the register (04H) is read first and the register (06H) is read last. The crystal calibration reading should be continuous and not be interrupted by any operation.

Certain bit locations within the device register map are designated as Reserved. To ensure proper and predictable operation, bits designated as Reserved should not be written by the users. In addition, their value should be masked out from any testing or error detection methods that are implemented.

7.1 REGISTER MAP

Table 42 is the map of all the registers, sorted in an ascending order of their addresses.

Table 42: Register List and Map

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
Global Control Registers										
00	ID[7:0] - Device ID 1	ID[7:0]								P 66
01	ID[15:8] - Device ID 2	ID[15:8]								P 66
02	MPU_PIN_STS - MPU_MODE[2:0] Pins Status	-	-	-	-	-	MPU_PIN_STS[2:0]			P 66
04	NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1	NOMINAL_FREQ_VALUE[7:0]								P 67
05	NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2	NOMINAL_FREQ_VALUE[15:8]								P 67
06	NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3	NOMINAL_FREQ_VALUE[23:16]								P 67
07	T4_T0_REG_SEL_CNFG - T0 / T4 Registers Selection Configuration	-	-	-	T4_T0_SEL	-	-	-	-	P 68
08	PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration	MULTI_FACTOR[1:0]		TIME_OUT_VALUE[5:0]						P 68
09	INPUT_MODE_CNFG - Input Mode Configuration	AUTO_EXT_SYNC_EN	EXT_SYNC_EN	PH_ALARM_TIMEOUT	SYNC_FREQ[1:0]		IN_SONET_SDH	MASTER_SLAVE	REVERTIVE_MODE	P 69

Table 42: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
0A	DIFFERENTIAL_IN_OUT_OSCI_CNFG - Differential Input / Output Port & Master Clock Configuration	-	-	-	-	-	OSC_EDGE	OUT7_PECL_LVDS	OUT6_PECL_LVDS	P 70
0B	MON_SW_PBO_CNFG - Frequency Monitor, Input Clock Selection & PBO Control	FREQ_MON_CLK	LOS_FLAG_TO_TDO	ULTR_FAST_SW	EXT_SW	PBO_FREZ	PBO_EN	-	FREQ_MON_HARD_EN	P 71
13	MS_SL_CTRL_CNFG - Master Slave Control	-	-	-	-	-	-	-	MS_SL_CTRL	P 72
7E	PROTECTION_CNFG - Register Protection Mode Configuration	PROTECTION_DATA[7:0]								P 72
7F	MPU_SEL_CNFG - Microprocessor Interface Mode Configuration	-	-	-	-	-	MPU_SEL_CNFG[2:0]			P 73
Interrupt Registers										
0C	INTERRUPT_CNFG - Interrupt Configuration	-	-	-	-	-	-	HZ_EN	INT_POL	P 74
0D	INTERRUPTS1_STS - Interrupt Status 1	IN[8:1]								P 74
0E	INTERRUPTS2_STS - Interrupt Status 2	T0_OPERATING_MODE	T0_MAIN_REF_FAILED	IN[14:9]						P 75
0F	INTERRUPTS3_STS - Interrupt Status 3	EX_SYNC_ALARM	T4_STS	-	INPUT_TO_T4	AMI2_VIOL	AMI2_LOS	AMI1_VIOL	AMI1_LOS	P 76
10	INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1	IN[8:1]								P 77
11	INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2	T0_OPERATING_MODE	T0_MAIN_REF_FAILED	IN[14:9]						P 77
12	INTERRUPTS3_ENABLE_CNFG - Interrupt Control 3	EX_SYNC_ALARM	T4_STS	-	INPUT_TO_T4	AMI2_VIOL	AMI2_LOS	AMI1_VIOL	AMI1_LOS	P 78
Input Clock Frequency & Priority Configuration Registers										
14	IN1_CNFG - Input Clock 1 Configuration	-	400HZ_SEL	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 79
15	IN2_CNFG - Input Clock 2 Configuration	-	400HZ_SEL	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 79
16	IN3_CNFG - Input Clock 3 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 80
17	IN4_CNFG - Input Clock 4 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 81
18	IN5_IN6_HF_DIV_CNFG - Input Clock 5 & 6 High Frequency Divider Configuration	IN6_DIV[1:0]		-	-	-	-	IN5_DIV[1:0]		P 82
19	IN5_CNFG - Input Clock 5 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 83
1A	IN6_CNFG - Input Clock 6 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 84
1B	IN7_CNFG - Input Clock 7 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 85
1C	IN8_CNFG - Input Clock 8 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 86

Table 42: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
1D	IN9_CNFG - Input Clock 9 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 87
1E	IN10_CNFG - Input Clock 10 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 88
1F	IN11_CNFG - Input Clock 11 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 89
20	IN12_CNFG - Input Clock 12 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 90
21	IN13_CNFG - Input Clock 13 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 91
22	IN14_CNFG - Input Clock 14 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 92
23	PRE_DIV_CH_CNFG - DivN Divider Channel Selection	-	-	-	-	PRE_DIV_CH_VALUE[3:0]				P 93
24	PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1	PRE_DIVN_VALUE[7:0]								P 93
25	PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2	-	PRE_DIVN_VALUE[14:8]							P 94
26	IN1_IN2_SEL_PRIORITY_CNFG - Input Clock 1 & 2 Priority Configuration *	IN2_SEL_PRIORITY[3:0]				IN1_SEL_PRIORITY[3:0]				P 95
27	IN3_IN4_SEL_PRIORITY_CNFG - Input Clock 3 & 4 Priority Configuration *	IN4_SEL_PRIORITY[3:0]				IN3_SEL_PRIORITY[3:0]				P 96
28	IN5_IN6_SEL_PRIORITY_CNFG - Input Clock 5 & 6 Priority Configuration *	IN6_SEL_PRIORITY[3:0]				IN5_SEL_PRIORITY[3:0]				P 97
29	IN7_IN8_SEL_PRIORITY_CNFG - Input Clock 7 & 8 Priority Configuration *	IN8_SEL_PRIORITY[3:0]				IN7_SEL_PRIORITY[3:0]				P 98
2A	IN9_IN10_SEL_PRIORITY_CNFG - Input Clock 9 & 10 Priority Configuration *	IN10_SEL_PRIORITY[3:0]				IN9_SEL_PRIORITY[3:0]				P 99
2B	IN11_IN12_SEL_PRIORITY_CNFG - Input Clock 11 & 12 Priority Configuration *	IN12_SEL_PRIORITY[3:0]				IN11_SEL_PRIORITY[3:0]				P 100
2C	IN13_IN14_SEL_PRIORITY_CNFG - Input Clock 13 & 14 Priority Configuration *	IN14_SEL_PRIORITY[3:0]				IN13_SEL_PRIORITY[3:0]				P 101
Input Clock Quality Monitoring Configuration & Status Registers										
2E	FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration	-	-	-	-	FREQ_MON_FACTOR[3:0]				P 102
2F	ALL_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for All Input Clocks Configuration	-	-	-	-	ALL_FREQ_HARD_THRESHOLD[3:0]				P 102
31	UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0	UPPER_THRESHOLD_0_DATA[7:0]								P 103

Table 42: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
32	LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0	LOWER_THRESHOLD_0_DATA[7:0]								P 103
33	BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0	BUCKET_SIZE_0_DATA[7:0]								P 103
34	DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0	-	-	-	-	-	-	DECAY_RATE_0_DATA[1:0]		P 104
35	UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1	UPPER_THRESHOLD_1_DATA[7:0]								P 104
36	LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1	LOWER_THRESHOLD_1_DATA[7:0]								P 104
37	BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1	BUCKET_SIZE_1_DATA[7:0]								P 105
38	DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1	-	-	-	-	-	-	DECAY_RATE_1_DATA[1:0]		P 105
39	UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2	UPPER_THRESHOLD_2_DATA[7:0]								P 105
3A	LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2	LOWER_THRESHOLD_2_DATA[7:0]								P 106
3B	BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2	BUCKET_SIZE_2_DATA[7:0]								P 106
3C	DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2	-	-	-	-	-	-	DECAY_RATE_2_DATA[1:0]		P 106
3D	UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3	UPPER_THRESHOLD_3_DATA[7:0]								P 107
3E	LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3	LOWER_THRESHOLD_3_DATA[7:0]								P 107
3F	BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3	BUCKET_SIZE_3_DATA[7:0]								P 107
40	DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3	-	-	-	-	-	-	DECAY_RATE_3_DATA[1:0]		P 108
41	IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection	-	-	-	-	IN_FREQ_READ_CH[3:0]				P 108
42	IN_FREQ_READ_STS - Input Clock Frequency Read Value	IN_FREQ_VALUE[7:0]								P 109
43	IN1_IN2_STS - Input Clock 1 & 2 Status	-	IN2_FREQ_HARD_ALARM	IN2_NO_ACTIVITY_ALARM	IN2_PH_LOCK_ALARM	-	IN1_FREQ_HARD_ALARM	IN1_NO_ACTIVITY_ALARM	IN1_PH_LOCK_ALARM	P 109
44	IN3_IN4_STS - Input Clock 3 & 4 Status	-	IN4_FREQ_HARD_ALARM	IN4_NO_ACTIVITY_ALARM	IN4_PH_LOCK_ALARM	-	IN3_FREQ_HARD_ALARM	IN3_NO_ACTIVITY_ALARM	IN3_PH_LOCK_ALARM	P 110

Table 42: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
45	IN5_IN6_STS - Input Clock 5 & 6 Status	-	IN6_FREQ_HARD_ALARM	IN6_NO_ACTIVITY_ALARM	IN6_PH_LOCK_ALARM	-	IN5_FREQ_HARD_ALARM	IN5_NO_ACTIVITY_ALARM	IN5_PH_LOCK_ALARM	P 111
46	IN7_IN8_STS - Input Clock 7 & 8 Status	-	IN8_FREQ_HARD_ALARM	IN8_NO_ACTIVITY_ALARM	IN8_PH_LOCK_ALARM	-	IN7_FREQ_HARD_ALARM	IN7_NO_ACTIVITY_ALARM	IN7_PH_LOCK_ALARM	P 112
47	IN9_IN10_STS - Input Clock 9 & 10 Status	-	IN10_FREQ_HARD_ALARM	IN10_NO_ACTIVITY_ALARM	IN10_PH_LOCK_ALARM	-	IN9_FREQ_HARD_ALARM	IN9_NO_ACTIVITY_ALARM	IN9_PH_LOCK_ALARM	P 113
48	IN11_IN12_STS - Input Clock 11 & 12 Status	-	IN12_FREQ_HARD_ALARM	IN12_NO_ACTIVITY_ALARM	IN12_PH_LOCK_ALARM	-	IN11_FREQ_HARD_ALARM	IN11_NO_ACTIVITY_ALARM	IN11_PH_LOCK_ALARM	P 114
49	IN13_IN14_STS - Input Clock 13 & 14 Status	-	IN14_FREQ_HARD_ALARM	IN14_NO_ACTIVITY_ALARM	IN14_PHASE_LOCK_ALARM	-	IN13_FREQ_HARD_ALARM	IN13_NO_ACTIVITY_ALARM	IN13_PHASE_LOCK_ALARM	P 115
T0 / T4 DPLL Input Clock Selection Registers										
4A	INPUT_VALID1_STS - Input Clocks Validity 1	IN[8:1]								P 116
4B	INPUT_VALID2_STS - Input Clocks Validity 2	-	-	IN[14:9]						P 116
4C	REMOTE_INPUT_VALID1_CNFG - Input Clocks Validity Configuration 1	IN8_VALID	IN7_VALID	IN6_VALID	IN5_VALID	IN4_VALID	IN3_VALID	IN2_VALID	IN1_VALID	P 116
4D	REMOTE_INPUT_VALID2_CNFG - Input Clocks Validity Configuration 2	-	-	IN14_VALID	IN13_VALID	IN12_VALID	IN11_VALID	IN10_VALID	IN9_VALID	P 117
4E	PRIORITY_TABLE1_STS - Priority Status 1 *	HIGHEST_PRIORITY_VALIDATED[3:0]				CURRENTLY_SELECTED_INPUT[3:0]				P 117
4F	PRIORITY_TABLE2_STS - Priority Status 2 *	THIRD_HIGHEST_PRIORITY_VALIDATED[3:0]				SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]				P 118
50	T0_INPUT_SEL_CNFG - T0 Selected Input Clock Configuration	-	-	-	-	T0_INPUT_SEL[3:0]				P 118
51	T4_INPUT_SEL_CNFG - T4 Selected Input Clock Configuration	-	T4_LOCK_T0	T0_FOR_T4	T4_TEST_T0_PH	T4_INPUT_SEL[3:0]				P 119
T0 / T4 DPLL State Machine Control Registers										
52	OPERATING_STS - DPLL Operating Status	EX_SYNC_ALARM_MON	T4_DPLL_LOCK	T0_DPLL_SOFT_FREQ_ALARM	T4_DPLL_SOFT_FREQ_ALARM	T0_DPLL_LOCK	T0_DPLL_OPERATING_MODE[2:0]			P 120
53	T0_OPERATING_MODE_CNFG - T0 DPLL Operating Mode Configuration	-	-	-	-	-	T0_OPERATING_MODE[2:0]			P 121
54	T4_OPERATING_MODE_CNFG - T4 DPLL Operating Mode Configuration	-	-	-	-	-	T4_OPERATING_MODE[2:0]			P 121
T0 / T4 DPLL & APLL Configuration Registers										
55	T0_DPLL_APLL_PATH_CNFG - T0 DPLL & APLL Path Configuration	T0_APLL_PATH[3:0]				T0_GSM_OBSAI_16E1_16T1_SEL[1:0]		T0_12E1_24T1_E3_T3_SEL[1:0]		P 122

Table 42: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
56	T0_DPLL_START_BW_DAMPING_CNFG - T0 DPLL Start Bandwidth & Damping Factor Configuration	T0_DPLL_START_DAMPING[2:0]			T0_DPLL_START_BW[4:0]					P 123
57	T0_DPLL_ACQ_BW_DAMPING_CNFG - T0 DPLL Acquisition Bandwidth & Damping Factor Configuration	T0_DPLL_ACQ_DAMPING[2:0]			T0_DPLL_ACQ_BW[4:0]					P 124
58	T0_DPLL_LOCKED_BW_DAMPING_CNFG - T0 DPLL Locked Bandwidth & Damping Factor Configuration	T0_DPLL_LOCKED_DAMPING[2:0]			T0_DPLL_LOCKED_BW[4:0]					P 125
59	T0_BW_OVERSHOOT_CNFG - T0 DPLL Bandwidth Overshoot Configuration	AUTO_BW_SEL	-	-	-	T0_LIMT	-	-	-	P 126
5A	PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration *	COARSE_PH_LOS_LIMT_EN	WIDE_EN	MULTI_PH_APP	MULTI_PH_8K_4K_2K_EN	PH_LOS_COARSE_LIMT[3:0]				P 127
5B	PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration *	FINE_PH_LOS_LIMT_EN	FAST_LOS_SW	-	-	-	PH_LOS_FINE_LIMT[2:0]			P 128
5C	T0_HOLDOVER_MODE_CNFG - T0 DPLL Holdover Mode Configuration	MAN_HOLDOVER	AUTO_AVG	FAST_AVG	READ_AVG	TEMP_HOLDOVER_MODE[1:0]		-	-	P 129
5D	T0_HOLDOVER_FREQ[7:0]_CNFG - T0 DPLL Holdover Frequency Configuration 1	T0_HOLDOVER_FREQ[7:0]								P 129
5E	T0_HOLDOVER_FREQ[15:8]_CNFG - T0 DPLL Holdover Frequency Configuration 2	T0_HOLDOVER_FREQ[15:8]								P 130
5F	T0_HOLDOVER_FREQ[23:16]_CNFG - T0 DPLL Holdover Frequency Configuration 3	T0_HOLDOVER_FREQ[23:16]								P 130
60	T4_DPLL_APLL_PATH_CNFG - T4 DPLL & APLL Path Configuration	T4_APLL_PATH[3:0]				T4_GSM_GPS_16E1_16T1_SEL[1:0]		T4_12E1_24T1_E3_T3_SEL[1:0]		P 131
61	T4_DPLL_LOCKED_BW_DAMPING_CNFG - T4 DPLL Locked Bandwidth & Damping Factor Configuration	T4_DPLL_LOCKED_DAMPING[2:0]			-	-	-	T4_DPLL_LOCKED_BW[1:0]		P 132
62	CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1 *	CURRENT_DPLL_FREQ[7:0]								P 132
63	CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2 *	CURRENT_DPLL_FREQ[15:8]								P 132
64	CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3 *	CURRENT_DPLL_FREQ[23:16]								P 133
65	DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration	FREQ_LIMT_PH_LOS	DPLL_FREQ_SOFT_LIMT[6:0]							P 133
66	DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1	DPLL_FREQ_HARD_LIMT[7:0]								P 133

Table 42: Register List and Map (Continued)

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
67	DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2	DPLL_FREQ_HARD_LIMT[15:8]								P 134
68	CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1 *	CURRENT_PH_DATA[7:0]								P 134
69	CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2 *	CURRENT_PH_DATA[15:8]								P 134
6A	T0_T4_APLL_BW_CNFG - T0 / T4 APLL Bandwidth Configuration	-	-	T0_APLL_BW[1:0]		-	-	T4_APLL_BW[1:0]		P 135
Output Configuration Registers										
6B	OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration	OUT1_PATH_SEL[3:0]				OUT1_DIVIDER[3:0]				P 136
6C	OUT2_FREQ_CNFG - Output Clock 2 Frequency Configuration	OUT2_PATH_SEL[3:0]				OUT2_DIVIDER[3:0]				P 137
6D	OUT3_FREQ_CNFG - Output Clock 3 Frequency Configuration	OUT3_PATH_SEL[3:0]				OUT3_DIVIDER[3:0]				P 138
6E	OUT4_FREQ_CNFG - Output Clock 4 Frequency Configuration	OUT4_PATH_SEL[3:0]				OUT4_DIVIDER[3:0]				P 139
6F	OUT5_FREQ_CNFG - Output Clock 5 Frequency Configuration	OUT5_PATH_SEL[3:0]				OUT5_DIVIDER[3:0]				P 140
70	OUT6_FREQ_CNFG - Output Clock 6 Frequency Configuration	OUT6_PATH_SEL[3:0]				OUT6_DIVIDER[3:0]				P 141
71	OUT7_FREQ_CNFG - Output Clock 7 Frequency Configuration	OUT7_PATH_SEL[3:0]				OUT7_DIVIDER[3:0]				P 142
72	OUT8_FREQ_CNFG - Output Clock 8 Frequency Configuration & Output Clock 6, 7 & 9 Invert Configuration	OUT8_PATH_SEL	OUT8_EN	T4_INPUT_FAIL	AMI_OUT_DUTY	400HZ_SEL	OUT9_INV	OUT7_INV	OUT6_INV	P 143
73	OUT9_FREQ_CNFG - Output Clock 9 Frequency Configuration & Output Clock 1 ~ 5 Invert Configuration	OUT9_PATH_SEL	OUT9_EN	T4_INPUT_FAIL	OUT5_INV	OUT4_INV	OUT3_INV	OUT2_INV	OUT1_INV	P 144
74	FR_MFR_SYNC_CNFG - Frame Sync & Multiframe Sync Output Configuration	IN_2K_4K_8K_INV	8K_EN	2K_EN	2K_8K_PUL_POSITION	8K_INV	8K_PUL	2K_INV	2K_PUL	P 145
PBO & Phase Offset Control Registers										
78	PHASE_MON_PBO_CNFG - Phase Transient Monitor & PBO Configuration	IN_NOISE_WINDOW	-	PH_MON_EN	PH_MON_PBO_EN	PH_TR_MON_LIMT[3:0]				P 146
7A	PHASE_OFFSET[7:0]_CNFG - Phase Offset Configuration 1	PH_OFFSET[7:0]								P 146
7B	PHASE_OFFSET[9:8]_CNFG - Phase Offset Configuration 2	PH_OFFSET_EN	-	-	-	-	-	PH_OFFSET[9:8]		P 147
Synchronization Configuration Registers										
7C	SYNC_MONITOR_CNFG - Sync Monitor Configuration	-	SYNC_MON_LIMT[2:0]			-	-	-	-	P 148
7D	SYNC_PHASE_CNFG - Sync Phase Configuration	-	-	-	-	-	-	SYNC_PH1[1:0]		P 148

7.2 REGISTER DESCRIPTION

7.2.1 GLOBAL CONTROL REGISTERS

ID[7:0] - Device ID 1

Address: 00H
Type: Read
Default Value: 10001000

7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bit	Name	Description
7 - 0	ID[7:0]	Refer to the description of the ID[15:8] bits (b7~0, 01H).

ID[15:8] - Device ID 2

Address: 01H
Type: Read
Default Value: 00010001

7	6	5	4	3	2	1	0
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

Bit	Name	Description
7 - 0	ID[15:8]	The value in the ID[15:0] bits are pre-set, representing the identification number for the IDT82V3280.

MPU_PIN_STS - MPU_MODE[2:0] Pins Status

Address: 02H
Type: Read
Default Value: XXXXXXXX

7	6	5	4	3	2	1	0
-	-	-	-	-	MPU_PIN_STS2	MPU_PIN_STS1	MPU_PIN_STS0

Bit	Name	Description
7 - 3	-	Reserved.
2 - 0	MPU_PIN_STS[2:0]	These bits indicate the value of the MPU_MODE[2:0] pins. The default value of these bits is determined by the MPU_MODE[2:0] pins during reset.

NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1

Address: 04H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
NOMINAL_FREQ_VALUE7	NOMINAL_FREQ_VALUE6	NOMINAL_FREQ_VALUE5	NOMINAL_FREQ_VALUE4	NOMINAL_FREQ_VALUE3	NOMINAL_FREQ_VALUE2	NOMINAL_FREQ_VALUE1	NOMINAL_FREQ_VALUE0

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[7:0]	Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H).

NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2

Address: 05H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
NOMINAL_FREQ_VALUE15	NOMINAL_FREQ_VALUE14	NOMINAL_FREQ_VALUE13	NOMINAL_FREQ_VALUE12	NOMINAL_FREQ_VALUE11	NOMINAL_FREQ_VALUE10	NOMINAL_FREQ_VALUE9	NOMINAL_FREQ_VALUE8

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[15:8]	Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H).

NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3

Address: 06H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
NOMINAL_FREQ_VALUE23	NOMINAL_FREQ_VALUE22	NOMINAL_FREQ_VALUE21	NOMINAL_FREQ_VALUE20	NOMINAL_FREQ_VALUE19	NOMINAL_FREQ_VALUE18	NOMINAL_FREQ_VALUE17	NOMINAL_FREQ_VALUE16

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[23:16]	The NOMINAL_FREQ_VALUE[23:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.0000884, the calibration value for the master clock in ppm will be gotten. For example, the frequency offset on OSCI is +3 ppm. Though -3 ppm should be compensated, the calibration value is calculated as +3 ppm: 3 ÷ 0.0000884 = 33937 (Dec.) = 8490 (Hex); So '008490' should be written into these bits. The calibration range is within ±741 ppm.

T4_T0_REG_SEL_CNFG - T0 / T4 Registers Selection Configuration

Address: 07H
Type: Read / Write
Default Value: XXX0XXXX

7	6	5	4	3	2	1	0
-	-	-	T4_T0_SEL	-	-	-	-

Bit	Name	Description
7 - 5	-	Reserved.
4	T4_T0_SEL	A part of the registers are shared by T0 and T4 paths. These registers are addressed 26H ~ 2CH, 4EH, 4FH, 5AH, 5BH, 62H ~ 64H, 68H and 69H. This bit determines whether the register configuration is available for T0 or T4 path. 0: T0 path (default). 1: T4 path.
3 - 0	-	Reserved.

PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration

Address: 08H
Type: Read / Write
Default Value: 00110010

7	6	5	4	3	2	1	0
MULTI_FACTOR1	MULTI_FACTOR0	TIME_OUT_VALUE5	TIME_OUT_VALUE4	TIME_OUT_VALUE3	TIME_OUT_VALUE2	TIME_OUT_VALUE1	TIME_OUT_VALUE0

Bit	Name	Description
7 - 6	MULTI_FACTOR[1:0]	These bits determine a factor which has a relationship with a period in seconds. A phase lock alarm will be raised if the T0 selected input clock is not locked in T0 DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, the phase lock alarm will be cleared after this period (starting from when the alarm is raised). Refer to the description of the TIME_OUT_VALUE[5:0] bits (b5~0, 08H). 00: 2 (default) 01: 4 10: 8 11: 16
5 - 0	TIME_OUT_VALUE[5:0]	These bits represent an unsigned integer. If the value in these bits is multiplied by the value in the MULTI_FACTOR[1:0] bits (b7~6, 08H), a period in seconds will be gotten. A phase lock alarm will be raised if the T0 selected input clock is not locked in T0 DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, the phase lock alarm will be cleared after this period (starting from when the alarm is raised).

INPUT_MODE_CNFG - Input Mode Configuration

Address: 09H
Type: Read / Write
Default Value: 10100XX0

7	6	5	4	3	2	1	0
AUTO_EXT_SYNC_EN	EXT_SYNC_EN	PH_ALARM_TIMEOUT	SYNC_FREQ1	SYNC_FREQ0	IN_SONET_SDH	MASTER_SLAVE	REVERTIVE_MODE

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>AUTO_EXT_SYNC_EN</td><td>Refer to the description of the EXT_SYNC_EN bit (b6, 09H).</td></tr>
<tr><td>6</td><td>EXT_SYNC_EN</td><td>This bit, together with the AUTO_EXT_SYNC_EN bit (b7, 09H), determines whether EX_SYNC1 is enabled to synchronize the frame sync output signals.
<table>
<tr><th>AUTO_EXT_SYNC_EN</th><th>EXT_SYNC_EN</th><th>Synchronization</th></tr>
<tr><td>don't-care</td><td>0</td><td>Disabled (default)</td></tr>
<tr><td>0</td><td>1</td><td>Enabled</td></tr>
<tr><td>1</td><td>1</td><td>Enabled if the T0 selected input clock is IN11; otherwise, disabled.</td></tr>
</table></td></tr>
<tr><td>5</td><td>PH_ALARM_TIMEOUT</td><td>This bit determines how to clear the phase lock alarm.
0: The phase lock alarm will be cleared when a '1' is written to the corresponding INn_PH_LOCK_ALARM bit (b4/0, 43H~49H).
1: The phase lock alarm will be cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised. (default)</td></tr>
<tr><td>4 - 3</td><td>SYNC_FREQ[1:0]</td><td>These bits set the frequency of the frame sync signal input on the EX_SYNC1 pin.
00: 8 kHz (default)
01: 8 kHz.
10: 4 kHz.
11: 2 kHz.</td></tr>
<tr><td>2</td><td>IN_SONET_SDH</td><td>This bit selects the SDH or SONET network type.
0: SDH. The DPLL required clock is 2.048 MHz when the IN_FREQ[3:0] bits (b3~0, 14H~17H & 19H~22H) are '0001'; the T0/T4 DPLL output from the 16E1/16T1 path is 16E1; and OUT9 outputs a 2.048 MHz signal if enabled.
1: SONET. The DPLL required clock is 1.544 MHz when the IN_FREQ[3:0] bits (b3~0, 14H~17H & 19H~22H) are '0001'; the T0/T4 DPLL output from the 16E1/16T1 path is 16T1; and OUT9 outputs a 1.544 MHz signal if enabled.
The default value of this bit is determined by the SONET/$\overline{\text{SDH}}$ pin during reset.</td></tr>
<tr><td>1</td><td>MASTER_SLAVE</td><td>This bit is read only. It indicates the value of the MS/$\overline{\text{SL}}$ pin.
Its default value is determined by the MS/$\overline{\text{SL}}$ pin during reset.</td></tr>
<tr><td>0</td><td>REVERTIVE_MODE</td><td>This bit selects Revertive or Non-Revertive switch for T0 path.
0: Non-Revertive switch. (default)
1: Revertive switch.</td></tr>
</table>

DIFFERENTIAL_IN_OUT_OSCI_CNFG - Differential Input / Output Port & Master Clock Configuration

Address: 0AH
Type: Read / Write
Default Value: XXXXX001

7	6	5	4	3	2	1	0
-	-	-	-	-	OSC_EDGE	OUT7_PECL_LVDS	OUT6_PECL_LVDS

Bit	Name	Description
7 - 3	-	Reserved.
2	OSC_EDGE	This bit selects a better active edge of the master clock. 0: The rising edge. (default) 1: The falling edge.
1	OUT7_PECL_LVDS	This bit selects a port technology for OUT7. 0: LVDS. (default) 1: PECL.
0	OUT6_PECL_LVDS	This bit selects a port technology for OUT6. 0: LVDS. 1: PECL. (default)

MON_SW_PBO_CNFG - Frequency Monitor, Input Clock Selection & PBO Control

Address: 0BH
Type: Read / Write
Default Value: 100X01X1

7	6	5	4	3	2	1	0
FREQ_MON_CLK	LOS_FLAG_TO_TDO	ULTR_FAST_SW	EXT_SW	PBO_FREZ	PBO_EN	-	FREQ_MON_HARD_EN

Bit	Name	Description
7	FREQ_MON_CLK	The bit selects a reference clock for input clock frequency monitoring. 0: The output of T0 DPLL. 1: The master clock. (default)
6	LOS_FLAG_TO_TDO	The bit determines whether the interrupt of T0 selected input clock fail - is reported by the TDO pin. 0: Not reported. TDO pin is used as JTAG test data output which complies with IEEE 1149.1. (default) 1: Reported. TDO pin mimics the state of the T0_MAIN_REF_FAILED bit (b6, 0EH) and does not strictly comply with IEEE 1149.1.
5	ULTR_FAST_SW	This bit determines whether the T0 selected input clock is valid when missing 2 consecutive clock cycles or more. 0: Valid. (default) 1: Invalid.
4	EXT_SW	This bit determines the T0 input clock selection. 0: Forced selection or Automatic selection, as controlled by the T0_INPUT_SEL[3:0] bits (b3~0, 50H). 1: External Fast selection. The default value of this bit is determined by the FF_SRCSW pin during reset.
3	PBO_FREZ	This bit is valid only when the PBO is enabled by the PBO_EN bit (b2, 0BH). It determines whether PBO is frozen at the current phase offset when a PBO event is triggered. 0: Not frozen. (default) 1: Frozen. Further PBO events are ignored and the current phase offset is maintained.
2	PBO_EN	This bit determines whether PBO is enabled when the T0 selected input clock switch or the T0 DPLL exiting from Holdover mode or Free-Run mode occurs. 0: Disabled. 1: Enabled. (default)
1	-	Reserved.
0	FREQ_MON_HARD_EN	This bit determines whether the frequency hard alarm is enabled when the frequency of the input clock with respect to the reference clock is above the frequency hard alarm threshold. The reference clock can be the output of T0 DPLL or the master clock, as determined by the FREQ_MON_CLK bit (b7, 0BH). 0: Disabled. 1: Enabled. (default)

MS_SL_CTRL_CNFG - Master Slave Control

Address: 13H
Type: Read / Write
Default Value: XXXXXXX0

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	MS_SL_CTRL

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7-1</td><td>-</td><td>Reserved.</td></tr>
<tr><td>0</td><td>MS_SL_CTRL</td><td>These bits, together with the MS/$\overline{\text{SL}}$ pin, control whether the device is configured as the Master or as the Slave.
<table>
<tr><th colspan="2">Master/Slave Control</th><th rowspan="2">Result</th></tr>
<tr><th>MS/$\overline{\text{SL}}$ pin</th><th>MS_SL_CTRL Bit</th></tr>
<tr><td rowspan="2">High</td><td>0</td><td>Master</td></tr>
<tr><td>1</td><td>Slave</td></tr>
<tr><td rowspan="2">Low</td><td>0</td><td>Slave</td></tr>
<tr><td>1</td><td>Master</td></tr>
</table>
The default value of this bit is ‘0’.</td></tr>
</table>

PROTECTION_CNFG - Register Protection Mode Configuration

Address: 7EH
Type: Read / Write
Default Value: 10000101

7	6	5	4	3	2	1	0
PROTECTION_DATA7	PROTECTION_DATA6	PROTECTION_DATA5	PROTECTION_DATA4	PROTECTION_DATA3	PROTECTION_DATA2	PROTECTION_DATA1	PROTECTION_DATA0

Bit	Name	Description
7 - 0	PROTECTION_DATA[7:0]	These bits select a register write protection mode. 00000000 - 10000100, 10000111 - 11111111: Protected mode. No other registers can be written except this register. 10000101: Fully Unprotected mode. All the writable registers can be written. (default) 10000110: Single Unprotected mode. One more register can be written besides this register. After write operation (not including writing a ‘1’ to clear the bit to ‘0’), the device automatically switches to Protected mode.

MPU_SEL_CNFG - Microprocessor Interface Mode Configuration

Address: 7FH
Type: Read / Write
Default Value: XXXXXXXX

7	6	5	4	3	2	1	0
-	-	-	-	-	MPU_SEL_CNFG2	MPU_SEL_CNFG1	MPU_SEL_CNFG0

Bit	Name	Description
7 - 3	-	Reserved.
2 - 0	MPU_SEL_CNFG[2:0]	These bits select a microprocessor interface mode: 000: Reserved. 001: ERPOM mode. 010: Multiplexed mode. 011: Intel mode. 100: Motorola mode. 101: Serial mode. 110, 111: Reserved. The default value of these bits are determined by the MPU_MODE[2:0] pins during reset.

7.2.2 INTERRUPT REGISTERS

INTERRUPT_CNFG - Interrupt Configuration

Address: 0CH
Type: Read / Write
Default Value: XXXXXX10

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HZ_EN	INT_POL

Bit	Name	Description
7 - 2	-	Reserved.
1	HZ_EN	This bit determines the output characteristics of the INT_REQ pin. 0: The output on the INT_REQ pin is high/low when the interrupt is active; the output is the opposite when the interrupt is inactive. 1: The output on the INT_REQ pin is high/low when the interrupt is active; the output is in high impedance state when the interrupt is inactive. (default)
0	INT_POL	This bit determines the active level on the INT_REQ pin for an active interrupt indication. 0: Active low. (default) 1: Active high.

INTERRUPTS1_STS - Interrupt Status 1

Address: 0DH
Type: Read / Write
Default Value: 11111111

7	6	5	4	3	2	1	0
IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1

Bit	Name	Description
7 - 0	INn	This bit indicates the validity changes (from ‘valid’ to ‘invalid’ or from ‘invalid’ to ‘valid’) for the corresponding INn; i.e., whether there is a transition (from ‘0’ to ‘1’ or from ‘1’ to ‘0’) on the corresponding INn bit (b7~0, 4AH). Here n is any one of 8 to 1. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a ‘1’.

INTERRUPTS2_STS - Interrupt Status 2

Address: 0EH
Type: Read / Write
Default Value: 00111111

7	6	5	4	3	2	1	0
T0_OPERAT-ING_MODE	T0_MAIN_REF_-FAILED	IN14	IN13	IN12	IN11	IN10	IN9

Bit	Name	Description
7	T0_OPERATING_MODE	This bit indicates the operating mode switch for T0 DPLL; i.e., whether the value in the T0_DPLL_OPERATING_-MODE[2:0] bits (b2~0, 52H) changes. 0: Has not switched. (default) 1: Has switched. This bit is cleared by writing a ‘1’.
6	T0_MAIN_REF_FAILED	This bit indicates whether the T0 selected input clock has failed. The T0 selected input clock fails when its validity changes from ‘valid’ to ‘invalid’; i.e., when there is a transition from ‘1’ to ‘0’ on the corresponding INn bit (4AH, 4BH). 0: Has not failed. (default) 1: Has failed. This bit is cleared by writing a ‘1’.
5 - 0	INn	This bit indicates the validity changes (from ‘valid’ to ‘invalid’ or from ‘invalid’ to ‘valid’) for the corresponding INn for T0 path, i.e., whether there is a transition (from ‘0’ to ‘1’ or from ‘1’ to ‘0’) on the corresponding INn bit (b5~0, 4BH). Here n is any one of 14 to 9. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a ‘1’.

INTERRUPTS3_STS - Interrupt Status 3

Address: 0FH
Type: Read / Write
Default Value: 11X10000

7	6	5	4	3	2	1	0
EX_SYNC_ALARM	T4_STS	-	INPUT_TO_T4	AMI2_VIOL	AMI2_LOS	AMI1_VIOL	AMI1_LOS

Bit	Name	Description
7	EX_SYNC_ALARM	This bit indicates whether an external sync alarm is raised; i.e., whether there is a transition from '0' to '1' on the EX_SYNC_ALARM_MON bit (b7, 52H). 0: Has not occurred. 1: Has occurred. (default) This bit is cleared by writing a '1'.
6	T4_STS	This bit indicates the T4 DPLL locking status changes (from 'locked' to 'unlocked' or from 'unlocked' to 'locked'); i.e., whether there is a transition (from '0' to '1' or from '1' to '0') on the T4_DPLL_LOCK bit (b6, 52H). 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a '1'.
5	-	Reserved.
4	INPUT_TO_T4	This bit indicates whether all the input clocks for T4 path changes to be unqualified; i.e., whether the HIGHEST_PRIORITY_VALIDATED[3:0] bits (b7~4, 4EH) are set to '0000' when these bits are available for T4 path. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a '1'.
3	AMI2_VIOL	This bit indicates whether IN2 has an AMI violation. 0: Has no AMI violation. (default) 1: Has an AMI violation. This bit is cleared by writing a '1'.
2	AMI2_LOS	This bit indicates whether IN2 has a LOS error. 0: Has no LOS error. (default) 1: Has a LOS error. This bit is cleared by writing a '1'.
1	AMI1_VIOL	This bit indicates whether IN1 has an AMI violation. 0: Has no AMI violation. (default) 1: Has an AMI violation. This bit is cleared by writing a '1'.
0	AMI1_LOS	This bit indicates whether IN1 has a LOS error. 0: Has no LOS error. (default) 1: Has a LOS error. This bit is cleared by writing a '1'.

INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1

Address: 10H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1

Bit	Name	Description
7 - 0	INn	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from ‘valid’ to ‘invalid’ or from ‘invalid’ to ‘valid’), i.e., when the corresponding INn bit (b7~0, 0DH) is ‘1’. Here n is any one of 8 to 1. 0: Disabled. (default) 1: Enabled.

INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2

Address: 11H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
T0_OPERATING_MODE	T0_MAIN_REF_FAILED	IN14	IN13	IN12	IN11	IN10	IN9

Bit	Name	Description
7	T0_OPERATING_MODE	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T0 DPLL operating mode switches, i.e., when the T0_OPERATING_MODE bit (b7, 0EH) is ‘1’. 0: Disabled. (default) 1: Enabled.
6	T0_MAIN_REF_FAILED	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T0 selected input clock has failed; i.e., when the T0_MAIN_REF_FAILED bit (b6, 0EH) is ‘1’. 0: Disabled. (default) 1: Enabled.
5 - 0	INn	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from ‘valid’ to ‘invalid’ or from ‘invalid’ to ‘valid’), i.e., when the corresponding INn bit (b5~0, 0EH) is ‘1’. Here n is any one of 14 to 9. 0: Disabled. (default) 1: Enabled.

INTERRUPTS3_ENABLE_CNFG - Interrupt Control 3

Address: 12H
Type: Read / Write
Default Value: 00X00000

7	6	5	4	3	2	1	0
EX_SYNC_ALARM	T4_STS	-	INPUT_TO_T4	AMI2_VIOL	AMI2_LOS	AMI1_VIOL	AMI1_LOS

Bit	Name	Description
7	EX_SYNC_ALARM	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when an external sync alarm has occurred, i.e., when the EX_SYNC_ALARM bit (b7, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
6	T4_STS	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the T4 DPLL locking status changes (from 'locked' to 'unlocked' or from 'unlocked' to 'locked'), i.e., when the T4_STS bit (b6, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
5	-	Reserved.
4	INPUT_TO_T4	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when all the input clocks for T4 path change to be unqualified, i.e., when the INPUT_TO_T4 bit (b4, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
3	AMI2_VIOL	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when IN2 has AMI violation, i.e., when the AMI2_VIOL bit (b3, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
2	AMI2_LOS	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when IN2 has LOS error, i.e., when the AMI2_LOS bit (b2, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
1	AMI1_VIOL	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when IN1 has AMI violation, i.e., when the AMI1_VIOL bit (b1, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.
0	AMI1_LOS	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when IN1 has LOS error, i.e., when the AMI1_LOS bit (b0, 0FH) is '1'. 0: Disabled. (default) 1: Enabled.

7.2.3 INPUT CLOCK FREQUENCY & PRIORITY CONFIGURATION REGISTERS

IN1_CNFG - Input Clock 1 Configuration

Address: 14H
Type: Read / Write
Default Value: X0000000

7	6	5	4	3	2	1	0
-	400HZ_SEL	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	-	Reserved.
6	400HZ_SEL	This bit should be set to match the clock input on IN1: 0: 64 kHz + 8 kHz. (default) 1: 64 kHz + 8 kHz + 0.4 kHz.
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN1: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN1: 0000: 8 kHz. (default) 0001 ~ 1111: Reserved.

IN2_CNFG - Input Clock 2 Configuration

Address: 15H
Type: Read / Write
Default Value: X0000000

7	6	5	4	3	2	1	0
-	400HZ_SEL	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	-	Reserved.
6	400HZ_SEL	This bit should be set to match the clock input on IN2: 0: 64 kHz + 8 kHz. (default) 1: 64 kHz + 8 kHz + 0.4 kHz.
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN2: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN2: 0000: 8 kHz. (default) 0001 ~ 1111: Reserved.

IN3_CNFG - Input Clock 3 Configuration

Address: 16H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>DIRECT_DIV</td><td>Refer to the description of the LOCK_8K bit (b6, 16H).</td></tr>
<tr><td>6</td><td>LOCK_8K</td><td>This bit, together with the DIRECT_DIV bit (b7, 16H), determines whether the DivN Divider or the Lock 8k Divider is used for IN3:
<table>
<tr><th>DIRECT_DIV bit</th><th>LOCK_8K bit</th><th>Used Divider</th></tr>
<tr><td>0</td><td>0</td><td>Both bypassed (default)</td></tr>
<tr><td>0</td><td>1</td><td>Lock 8k Divider</td></tr>
<tr><td>1</td><td>0</td><td>DivN Divider</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5 - 4</td><td>BUCKET_SEL[1:0]</td><td>These bits select one of the four groups of leaky bucket configuration registers for IN3:
00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)
01: Group 1; the addresses of the configuration registers are 35H ~ 38H.
10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.
11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</td></tr>
<tr><td>3 - 0</td><td>IN_FREQ[3:0]</td><td>These bits set the DPLL required frequency for IN3:
0000: 8 kHz. (default)
0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’).
0010: 6.48 MHz.
0011: 19.44 MHz.
0100: 25.92 MHz.
0101: 38.88 MHz.
0110 ~ 1000: Reserved.
1001: 2 kHz.
1010: 4 kHz.
1011 ~ 1111: Reserved.
For IN3, the required frequency should not be set higher than that of the input clock.</td></tr>
</table>

IN4_CNFG - Input Clock 4 Configuration

Address: 17H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>DIRECT_DIV</td><td>Refer to the description of the LOCK_8K bit (b6, 17H).</td></tr>
<tr><td>6</td><td>LOCK_8K</td><td>This bit, together with the DIRECT_DIV bit (b7, 17H), determines whether the DivN Divider or the Lock 8k Divider is used for IN4:
<table>
<tr><th>DIRECT_DIV bit</th><th>LOCK_8K bit</th><th>Used Divider</th></tr>
<tr><td>0</td><td>0</td><td>Both bypassed (default)</td></tr>
<tr><td>0</td><td>1</td><td>Lock 8k Divider</td></tr>
<tr><td>1</td><td>0</td><td>DivN Divider</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5 - 4</td><td>BUCKET_SEL[1:0]</td><td>These bits select one of the four groups of leaky bucket configuration registers for IN4:
00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)
01: Group 1; the addresses of the configuration registers are 35H ~ 38H.
10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.
11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</td></tr>
<tr><td>3 - 0</td><td>IN_FREQ[3:0]</td><td>These bits set the DPLL required frequency for IN4:
0000: 8 kHz. (default)
0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’).
0010: 6.48 MHz.
0011: 19.44 MHz.
0100: 25.92 MHz.
0101: 38.88 MHz.
0110 ~ 1000: Reserved.
1001: 2 kHz.
1010: 4 kHz.
1011 ~ 1111: Reserved.
For the IN4, the required frequency should not be set higher than that of the input clock.</td></tr>
</table>

IN5_IN6_HF_DIV_CNFG - Input Clock 5 & 6 High Frequency Divider Configuration

Address: 18H
Type: Read / Write
Default Value: 00XXXX00

7	6	5	4	3	2	1	0
IN6_DIV1	IN6_DIV0	-	-	-	-	IN5_DIV1	IN5_DIV0

Bit	Name	Description
7 - 6	IN6_DIV[1:0]	These bits determine whether the HF Divider is used and what the division factor is for IN6 frequency division: 00: Bypassed. (default) 01: Divided by 4. 10: Divided by 5. 11: Reserved.
5 - 2	-	Reserved.
1 - 0	IN5_DIV[1:0]	These bits determine whether the HF Divider is used and what the division factor is for IN5 frequency division: 00: Bypassed. (default) 01: Divided by 4. 10: Divided by 5. 11: Reserved.

IN5_CNFG - Input Clock 5 Configuration

Address: 19H
Type: Read / Write
Default Value: 00000011

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 19H).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 19H), determines whether the DivN Divider or the Lock 8k Divider is used for IN5:
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN5: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN5: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. The required frequency should not be set higher than that of the input clock.

Bit 6 (LOCK_8K), nested table:

DIRECT_DIV bit	LOCK_8K bit	Used Divider
0	0	Both bypassed (default)
0	1	Lock 8k Divider
1	0	DivN Divider
1	1	Reserved

IN6_CNFG - Input Clock 6 Configuration

Address: 1AH
Type: Read / Write
Default Value: 00000011

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1AH).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1AH), determines whether the DivN Divider or the Lock 8k Divider is used for IN6:
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN6: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN6: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. For IN6, the required frequency should not be set higher than that of the input clock.

DIRECT_DIV bit	LOCK_8K bit	Used Divider
0	0	Both bypassed (default)
0	1	Lock 8k Divider
1	0	DivN Divider
1	1	Reserved

IN7_CNFG - Input Clock 7 Configuration

Address: 1BH
Type: Read / Write
Default Value: 00000011

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1BH).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1BH), determines whether the DivN Divider or the Lock 8k Divider is used for IN7:
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN7: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN7: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. For IN7, the required frequency should not be set higher than that of the input clock.

DIRECT_DIV bit	LOCK_8K bit	Used Divider
0	0	Both bypassed (default)
0	1	Lock 8k Divider
1	0	DivN Divider
1	1	Reserved

IN8_CNFG - Input Clock 8 Configuration

Address: 1CH
Type: Read / Write
Default Value: 00000011

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>DIRECT_DIV</td><td>Refer to the description of the LOCK_8K bit (b6, 1CH).</td></tr>
<tr><td>6</td><td>LOCK_8K</td><td>This bit, together with the DIRECT_DIV bit (b7, 1CH), determines whether the DivN Divider or the Lock 8k Divider is used for IN8:
<table>
<tr><th>DIRECT_DIV bit</th><th>LOCK_8K bit</th><th>Used Divider</th></tr>
<tr><td>0</td><td>0</td><td>Both bypassed (default)</td></tr>
<tr><td>0</td><td>1</td><td>Lock 8k Divider</td></tr>
<tr><td>1</td><td>0</td><td>DivN Divider</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5 - 4</td><td>BUCKET_SEL[1:0]</td><td>These bits select one of the four groups of leaky bucket configuration registers for IN8:
00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)
01: Group 1; the addresses of the configuration registers are 35H ~ 38H.
10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.
11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</td></tr>
<tr><td>3 - 0</td><td>IN_FREQ[3:0]</td><td>These bits set the DPLL required frequency for IN8:
0000: 8 kHz.
0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’).
0010: 6.48 MHz.
0011: 19.44 MHz. (default)
0100: 25.92 MHz.
0101: 38.88 MHz.
0110 ~ 1000: Reserved.
1001: 2 kHz.
1010: 4 kHz.
1011 ~ 1111: Reserved.
For IN8, the required frequency should not be set higher than that of the input clock.</td></tr>
</table>

IN9_CNFG - Input Clock 9 Configuration

Address: 1DH
Type: Read / Write
Default Value: 00000011

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>DIRECT_DIV</td><td>Refer to the description of the LOCK_8K bit (b6, 1DH).</td></tr>
<tr><td>6</td><td>LOCK_8K</td><td>This bit, together with the DIRECT_DIV bit (b7, 1DH), determines whether the DivN Divider or the Lock 8k Divider is used for IN9:
<table>
<tr><th>DIRECT_DIV bit</th><th>LOCK_8K bit</th><th>Used Divider</th></tr>
<tr><td>0</td><td>0</td><td>Both bypassed (default)</td></tr>
<tr><td>0</td><td>1</td><td>Lock 8k Divider</td></tr>
<tr><td>1</td><td>0</td><td>DivN Divider</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5 - 4</td><td>BUCKET_SEL[1:0]</td><td>These bits select one of the four groups of leaky bucket configuration registers for IN9:
00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)
01: Group 1; the addresses of the configuration registers are 35H ~ 38H.
10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.
11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</td></tr>
<tr><td>3 - 0</td><td>IN_FREQ[3:0]</td><td>These bits set the DPLL required frequency for IN9:
0000: 8 kHz.
0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’).
0010: 6.48 MHz.
0011: 19.44 MHz. (default)
0100: 25.92 MHz.
0101: 38.88 MHz.
0110 ~ 1000: Reserved.
1001: 2 kHz.
1010: 4 kHz.
1011 ~ 1111: Reserved.
For IN9, the required frequency should not be set higher than that of the input clock.</td></tr>
</table>

IN10_CNFG - Input Clock 10 Configuration

Address: 1EH
Type: Read / Write
Default Value: 00000011

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1EH).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1EH), determines whether the DivN Divider or the Lock 8k Divider is used for IN10:
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN10: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN10: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. For IN10, the required frequency should not be set higher than that of the input clock.

DIRECT_DIV bit	LOCK_8K bit	Used Divider
0	0	Both bypassed (default)
0	1	Lock 8k Divider
1	0	DivN Divider
1	1	Reserved

IN11_CNFG - Input Clock 11 Configuration

Address: 1FH
Type: Read / Write
Default Value: 0000XXXX

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>DIRECT_DIV</td><td>Refer to the description of the LOCK_8K bit (b6, 1FH).</td></tr>
<tr><td>6</td><td>LOCK_8K</td><td>This bit, together with the DIRECT_DIV bit (b7, 1FH), determines whether the DivN Divider or the Lock 8k Divider is used for IN11:
<table>
<tr><th>DIRECT_DIV bit</th><th>LOCK_8K bit</th><th>Used Divider</th></tr>
<tr><td>0</td><td>0</td><td>Both bypassed (default)</td></tr>
<tr><td>0</td><td>1</td><td>Lock 8k Divider</td></tr>
<tr><td>1</td><td>0</td><td>DivN Divider</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5 - 4</td><td>BUCKET_SEL[1:0]</td><td>These bits select one of the four groups of leaky bucket configuration registers for IN11:
00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)
01: Group 1; the addresses of the configuration registers are 35H ~ 38H.
10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.
11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</td></tr>
<tr><td>3 - 0</td><td>IN_FREQ[3:0]</td><td>These bits set the DPLL required frequency for IN11:
0000: 8 kHz.
0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’).
0010: 6.48 MHz.
0011: 19.44 MHz.
0100: 25.92 MHz.
0101: 38.88 MHz.
0110 ~ 1000: Reserved.
1001: 2 kHz.
1010: 4 kHz.
1011 ~ 1111: Reserved.
For IN11, the required frequency should not be set higher than that of the input clock.
The default value of these bits depends on the device application as follows:
In Master / Slave application, when the device is configured as the Master, the default value is ‘0001’; when the device is configured as the Slave, the default value is ‘0010’.</td></tr>
</table>

IN12_CNFG - Input Clock 12 Configuration

Address: 20H
Type: Read / Write
Default Value: 00000001

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>DIRECT_DIV</td><td>Refer to the description of the LOCK_8K bit (b6, 20H).</td></tr>
<tr><td>6</td><td>LOCK_8K</td><td>This bit, together with the DIRECT_DIV bit (b7, 20H), determines whether the DivN Divider or the Lock 8k Divider is used for IN12:
<table>
<tr><th>DIRECT_DIV bit</th><th>LOCK_8K bit</th><th>Used Divider</th></tr>
<tr><td>0</td><td>0</td><td>Both bypassed (default)</td></tr>
<tr><td>0</td><td>1</td><td>Lock 8k Divider</td></tr>
<tr><td>1</td><td>0</td><td>DivN Divider</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>5 - 4</td><td>BUCKET_SEL[1:0]</td><td>These bits select one of the four groups of leaky bucket configuration registers for IN12:
00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default)
01: Group 1; the addresses of the configuration registers are 35H ~ 38H.
10: Group 2; the addresses of the configuration registers are 39H ~ 3CH.
11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.</td></tr>
<tr><td>3 - 0</td><td>IN_FREQ[3:0]</td><td>These bits set the DPLL required frequency for IN12:
0000: 8 kHz.
0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’). (default)
0010: 6.48 MHz.
0011: 19.44 MHz.
0100: 25.92 MHz.
0101: 38.88 MHz.
0110 ~ 1000: Reserved.
1001: 2 kHz.
1010: 4 kHz.
1011 ~ 1111: Reserved.
For IN12, the required frequency should not be set higher than that of the input clock.</td></tr>
</table>

IN13_CNFG - Input Clock 13 Configuration

Address: 21H
Type: Read / Write
Default Value: 00000001

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 21H).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 21H), determines whether the DivN Divider or the Lock 8k Divider is used for IN13:
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN13: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN13: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’). (default) 0010: 6.48 MHz. 0011: 19.44 MHz. 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. For IN13, the required frequency should not be set higher than that of the input clock.

Bit 6 (LOCK_8K), nested table:

DIRECT_DIV bit	LOCK_8K bit	Used Divider
0	0	Both bypassed (default)
0	1	Lock 8k Divider
1	0	DivN Divider
1	1	Reserved

IN14_CNFG - Input Clock 14 Configuration

Address: 22H
Type: Read / Write
Default Value: 00000001

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 22H).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 22H), determines whether the DivN Divider or the Lock 8k Divider is used for IN14:
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN14: 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN14: 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘1’) / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is ‘0’). (default) 0010: 6.48 MHz. 0011: 19.44 MHz. 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011 ~ 1111: Reserved. For IN14, the required frequency should not be set higher than that of the input clock.

Bit 6 (LOCK_8K), divider selection:

DIRECT_DIV bit	LOCK_8K bit	Used Divider
0	0	Both bypassed (default)
0	1	Lock 8k Divider
1	0	DivN Divider
1	1	Reserved

PRE_DIV_CH_CNFG - DivN Divider Channel Selection

Address: 23H
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	PRE_DIV_CH_VALUE3	PRE_DIV_CH_VALUE2	PRE_DIV_CH_VALUE1	PRE_DIV_CH_VALUE0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	PRE_DIV_CH_VALUE[3:0]	This register is an indirect address register for Register 24H and 25H. These bits select an input clock. The value set in the PRE_DIVN_VALUE[14:0] bits (25H, 24H) is available for the selected input clock. 0000: Reserved. (default) 0001, 0010: Reserved. 0011: IN3. 0100: IN4. ...... 1101: IN13. 1110: IN14. 1111: Reserved.

PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1

Address: 24H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
PRE_DIVN_VALUE7	PRE_DIVN_VALUE6	PRE_DIVN_VALUE5	PRE_DIVN_VALUE4	PRE_DIVN_VALUE3	PRE_DIVN_VALUE2	PRE_DIVN_VALUE1	PRE_DIVN_VALUE0

Bit	Name	Description
7 - 0	PRE_DIVN_VALUE[7:0]	Refer to the description of the PRE_DIVN_VALUE[14:8] bits (b6~0, 25H).

PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2

Address: 25H
Type: Read / Write
Default Value: X0000000

7	6	5	4	3	2	1	0
-	PRE_DIVN_VALUE14	PRE_DIVN_VALUE13	PRE_DIVN_VALUE12	PRE_DIVN_VALUE11	PRE_DIVN_VALUE10	PRE_DIVN_VALUE9	PRE_DIVN_VALUE8

Bit	Name	Description
7	-	Reserved.
6 - 0	PRE_DIVN_VALUE[14:8]	If the value in the PRE_DIVN_VALUE[14:0] bits is plus 1, the division factor for an input clock will be gotten. The input clock is selected by the PRE_DIV_CH_VALUE[3:0] bits (b3~0, 23H). A value from ‘0’ to ‘4BEF’ (Hex) can be written into, corresponding to a division factor from 1 to 19440. The others are reserved. So the DivN Divider only supports an input clock whose frequency is lower than (<) 155.52 MHz. The division factor setting should observe the following order: 1. Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits; 2. Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.

IN1_IN2_SEL_PRIORITY_CNFG - Input Clock 1 & 2 Priority Configuration *

Address: 26H
Type: Read / Write
Default Value: T0 - 00110010 / T4 - 00000000

7	6	5	4	3	2	1	0
IN2_SEL_PRIORITY3	IN2_SEL_PRIORITY2	IN2_SEL_PRIORITY1	IN2_SEL_PRIORITY0	IN1_SEL_PRIORITY3	IN1_SEL_PRIORITY2	IN1_SEL_PRIORITY1	IN1_SEL_PRIORITY0

Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 2: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. (T0 default) 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 1: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. (T0 default) 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN3_IN4_SEL_PRIORITY_CNFG - Input Clock 3 & 4 Priority Configuration *

Address: 27H
Type: Read / Write
Default Value: T0 - 01010100 / T4 - 00000000

7	6	5	4	3	2	1	0
IN4_SEL_PRIORITY3	IN4_SEL_PRIORITY2	IN4_SEL_PRIORITY1	IN4_SEL_PRIORITY0	IN3_SEL_PRIORITY3	IN3_SEL_PRIORITY2	IN3_SEL_PRIORITY1	IN3_SEL_PRIORITY0

Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 4. 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. (T0 default) 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 3. 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. (T0 default) 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN5_IN6_SEL_PRIORITY_CNFG - Input Clock 5 & 6 Priority Configuration *

Address: 28H
Type: Read / Write
Default Value: T0/T4 - 01110110

7	6	5	4	3	2	1	0
IN6_SEL_PRIORITY3	IN6_SEL_PRIORITY2	IN6_SEL_PRIORITY1	IN6_SEL_PRIORITY0	IN5_SEL_PRIORITY3	IN5_SEL_PRIORITY2	IN5_SEL_PRIORITY1	IN5_SEL_PRIORITY0

Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 6. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. (default) 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 5. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. (default) 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN7_IN8_SEL_PRIORITY_CNFG - Input Clock 7 & 8 Priority Configuration *

Address: 29H
Type: Read / Write
Default Value: 10011000

7	6	5	4	3	2	1	0
IN8_SEL_PRIORITY3	IN8_SEL_PRIORITY2	IN8_SEL_PRIORITY1	IN8_SEL_PRIORITY0	IN7_SEL_PRIORITY3	IN7_SEL_PRIORITY2	IN7_SEL_PRIORITY1	IN7_SEL_PRIORITY0

Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 8. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. (default) 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 7. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. (default) 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN9_IN10_SEL_PRIORITY_CNFG - Input Clock 9 & 10 Priority Configuration *

Address: 2AH
Type: Read / Write
Default Value: 10111010

7	6	5	4	3	2	1	0
IN10_SEL_PRIORITY3	IN10_SEL_PRIORITY2	IN10_SEL_PRIORITY1	IN10_SEL_PRIORITY0	IN9_SEL_PRIORITY3	IN9_SEL_PRIORITY2	IN9_SEL_PRIORITY1	IN9_SEL_PRIORITY0

Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 10. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. (default) 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 9. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. (default) 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN11_IN12_SEL_PRIORITY_CNFG - Input Clock 11 & 12 Priority Configuration *

Address: 2BH
Type: Read / Write
Default Value: 11011100 (T0 Master)/11010001 (T0 Slave) 00000000 (T4)

7	6	5	4	3	2	1	0
IN12_SEL_PRIORITY3	IN12_SEL_PRIORITY2	IN12_SEL_PRIORITY1	IN12_SEL_PRIORITY0	IN11_SEL_PRIORITY3	IN11_SEL_PRIORITY2	IN11_SEL_PRIORITY1	IN11_SEL_PRIORITY0

Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 12: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. (T0 Master/Slave default) 1110: Priority 14. 1111: Priority 15.
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 11: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. (T0 Slave default) 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. (T0 Master default) 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN13_IN14_SEL_PRIORITY_CNFG - Input Clock 13 & 14 Priority Configuration *

Address: 2CH
Type: Read / Write
Default Value: 11111110 (T0) 00000000 (T4)

7	6	5	4	3	2	1	0
IN14_SEL_PRIORITY3	IN14_SEL_PRIORITY2	IN14_SEL_PRIORITY1	IN14_SEL_PRIORITY0	IN13_SEL_PRIORITY3	IN13_SEL_PRIORITY2	IN13_SEL_PRIORITY1	IN13_SEL_PRIORITY0

Bit	Name	Description
7 - 4	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 14: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15. (T0 default)
3 - 0	INn_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding INn. Here n is 13: 0000: Disable INn for automatic selection. (T4 default) 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. (T0 default) 1111: Priority 15.

7.2.4 INPUT CLOCK QUALITY MONITORING CONFIGURATION & STATUS REGISTERS

FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration

Address: 2EH
Type: Read / Write
Default Value: XXXX1011

7	6	5	4	3	2	1	0
-	-	-	-	FREQ_MON_FACTOR3	FREQ_MON_FACTOR2	FREQ_MON_FACTOR1	FREQ_MON_FACTOR0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	FREQ_MON_FACTOR[3:0]	These bits determine a factor. The factor has a relationship with the frequency hard alarm threshold in ppm (refer to the description of the ALL_FREQ_HARD_THRESHOLD[3:0] bits (b3~0, 2FH)) and with the frequency of the input clock with respect to the master clock in ppm (refer to the description of the IN_FREQ_VALUE[7:0] bits (b7~0, 42H)). The factor represents the accuracy of the frequency monitor and should be set according to the requirements of different applications. 0000: 0.0032. 0001: 0.0064. 0010: 0.0127. 0011: 0.0257. 0100: 0.0514. 0101: 0.103. 0110: 0.206. 0111: 0.412. 1000: 0.823. 1001: 1.646. 1010: 3.292. 1011: 3.81. (default) 1100 - 1111: 4.6.

ALL_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for All Input Clocks Configuration

Address: 2FH
Type: Read / Write
Default Value: XXXX0011

7	6	5	4	3	2	1	0
-	-	-	-	ALL_FREQ_HARD_THRESHOLD3	ALL_FREQ_HARD_THRESHOLD2	ALL_FREQ_HARD_THRESHOLD1	ALL_FREQ_HARD_THRESHOLD0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	ALL_FREQ_HARD_THRESHOLD[3:0]	These bits represent an unsigned integer. The frequency hard alarm threshold in ppm can be calculated as follows: *Frequency Hard Alarm Threshold (ppm) = (ALL_FREQ_HARD_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)* This threshold is symmetrical about zero.

UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0

Address: 31H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_THRESHOLD_0_DATA7	UPPER_THRESHOLD_0_DATA6	UPPER_THRESHOLD_0_DATA5	UPPER_THRESHOLD_0_DATA4	UPPER_THRESHOLD_0_DATA3	UPPER_THRESHOLD_0_DATA2	UPPER_THRESHOLD_0_DATA1	UPPER_THRESHOLD_0_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_0_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0

Address: 32H
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_THRESHOLD_0_DATA7	LOWER_THRESHOLD_0_DATA6	LOWER_THRESHOLD_0_DATA5	LOWER_THRESHOLD_0_DATA4	LOWER_THRESHOLD_0_DATA3	LOWER_THRESHOLD_0_DATA2	LOWER_THRESHOLD_0_DATA1	LOWER_THRESHOLD_0_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_0_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0

Address: 33H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_SIZE_0_DATA7	BUCKET_SIZE_0_DATA6	BUCKET_SIZE_0_DATA5	BUCKET_SIZE_0_DATA4	BUCKET_SIZE_0_DATA3	BUCKET_SIZE_0_DATA2	BUCKET_SIZE_0_DATA1	BUCKET_SIZE_0_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_0_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0

Address: 34H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_0_DATA1	DECAY_RATE_0_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_0_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1

Address: 35H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_THRESHOLD_1_DATA7	UPPER_THRESHOLD_1_DATA6	UPPER_THRESHOLD_1_DATA5	UPPER_THRESHOLD_1_DATA4	UPPER_THRESHOLD_1_DATA3	UPPER_THRESHOLD_1_DATA2	UPPER_THRESHOLD_1_DATA1	UPPER_THRESHOLD_1_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_1_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1

Address: 36H
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_THRESHOLD_1_DATA7	LOWER_THRESHOLD_1_DATA6	LOWER_THRESHOLD_1_DATA5	LOWER_THRESHOLD_1_DATA4	LOWER_THRESHOLD_1_DATA3	LOWER_THRESHOLD_1_DATA2	LOWER_THRESHOLD_1_DATA1	LOWER_THRESHOLD_1_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_1_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1

Address: 37H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_1_DATA7	BUCKET_-SIZE_1_DATA6	BUCKET_-SIZE_1_DATA5	BUCKET_-SIZE_1_DATA4	BUCKET_-SIZE_1_DATA3	BUCKET_-SIZE_1_DATA2	BUCKET_-SIZE_1_DATA1	BUCKET_-SIZE_1_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_1_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1

Address: 38H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_1_DATA1	DECAY_RATE_1_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_1_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2

Address: 39H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_2_DATA7	UPPER_-THRESH-OLD_2_DATA6	UPPER_-THRESH-OLD_2_DATA5	UPPER_-THRESH-OLD_2_DATA4	UPPER_-THRESH-OLD_2_DATA3	UPPER_-THRESH-OLD_2_DATA2	UPPER_-THRESH-OLD_2_DATA1	UPPER_-THRESH-OLD_2_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_2_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2

Address: 3AH
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_THRESHOLD_2_DATA7	LOWER_THRESHOLD_2_DATA6	LOWER_THRESHOLD_2_DATA5	LOWER_THRESHOLD_2_DATA4	LOWER_THRESHOLD_2_DATA3	LOWER_THRESHOLD_2_DATA2	LOWER_THRESHOLD_2_DATA1	LOWER_THRESHOLD_2_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_2_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2

Address: 3BH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_SIZE_2_DATA7	BUCKET_SIZE_2_DATA6	BUCKET_SIZE_2_DATA5	BUCKET_SIZE_2_DATA4	BUCKET_SIZE_2_DATA3	BUCKET_SIZE_2_DATA2	BUCKET_SIZE_2_DATA1	BUCKET_SIZE_2_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_2_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2

Address: 3CH
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_2_DATA1	DECAY_RATE_2_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_2_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3

Address: 3DH
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_3_DATA7	UPPER_-THRESH-OLD_3_DATA6	UPPER_-THRESH-OLD_3_DATA5	UPPER_-THRESH-OLD_3_DATA4	UPPER_-THRESH-OLD_3_DATA3	UPPER_-THRESH-OLD_3_DATA2	UPPER_-THRESH-OLD_3_DATA1	UPPER_-THRESH-OLD_3_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_3_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3

Address: 3EH
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_-THRESH-OLD_3_DATA7	LOWER_-THRESH-OLD_3_DATA6	LOWER_-THRESH-OLD_3_DATA5	LOWER_-THRESH-OLD_3_DATA4	LOWER_-THRESH-OLD_3_DATA3	LOWER_-THRESH-OLD_3_DATA2	LOWER_-THRESH-OLD_3_DATA1	LOWER_-THRESH-OLD_3_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_3_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3

Address: 3FH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_3_DATA7	BUCKET_-SIZE_3_DATA6	BUCKET_-SIZE_3_DATA5	BUCKET_-SIZE_3_DATA4	BUCKET_-SIZE_3_DATA3	BUCKET_-SIZE_3_DATA2	BUCKET_-SIZE_3_DATA1	BUCKET_-SIZE_3_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_3_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3

Address: 40H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_3_DATA1	DECAY_RATE_3_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_3_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection

Address: 41H
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	IN_FREQ_READ_CH3	IN_FREQ_READ_CH2	IN_FREQ_READ_CH1	IN_FREQ_READ_CH0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	IN_FREQ_READ_CH[3:0]	These bits select an input clock, the frequency of which with respect to the reference clock can be read. 0000: Reserved. (default) 0001: IN1. 0010: IN2. ...... 1101: IN13. 1110: IN14. 1111: Reserved.

IN_FREQ_READ_STS - Input Clock Frequency Read Value

Address: 42H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
IN_FREQ_VALUE7	IN_FREQ_VALUE6	IN_FREQ_VALUE5	IN_FREQ_VALUE4	IN_FREQ_VALUE3	IN_FREQ_VALUE2	IN_FREQ_VALUE1	IN_FREQ_VALUE0

Bit	Name	Description
7 - 0	IN_FREQ_VALUE[7:0]	These bits represent a 2's complement signed integer. If the value is multiplied by the value in the FREQ_MON_FACTOR[3:0] bits (b3~0, 2EH), the frequency of an input clock with respect to the reference clock in ppm will be gotten. The input clock is selected by the IN_FREQ_READ_CH[3:0] bits (b3~0, 41H). The value in these bits is updated every 16 seconds, starting when an input clock is selected.

IN1_IN2_STS - Input Clock 1 & 2 Status

Address: 43H
Type: Read
Default Value: X110X110

7	6	5	4	3	2	1	0
-	IN2_FREQ_HARD_ALARM	IN2_NO_ACTIVITY_ALARM	IN2_PH_LOCK_ALARM	-	IN1_FREQ_HARD_ALARM	IN1_NO_ACTIVITY_ALARM	IN1_PH_LOCK_ALARM

Bit	Name	Description
7	-	Reserved.
6	IN2_FREQ_HARD_ALARM	This bit indicates whether IN2 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
5	IN2_NO_ACTIVITY_ALARM	This bit indicates whether IN2 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN2_PH_LOCK_ALARM	This bit indicates whether IN2 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	-	Reserved.
2	IN1_FREQ_HARD_ALARM	This bit indicates whether IN1 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
1	IN1_NO_ACTIVITY_ALARM	This bit indicates whether IN1 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN1_PH_LOCK_ALARM	This bit indicates whether IN1 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

IN3_IN4_STS - Input Clock 3 & 4 Status

Address: 44H
Type: Read
Default Value: X110X110

7	6	5	4	3	2	1	0
-	IN4_FREQ_HARD_ALARM	IN4_NO_ACTIVITY_ALARM	IN4_PH_LOCK_ALARM	-	IN3_FREQ_HARD_ALARM	IN3_NO_ACTIVITY_ALARM	IN3_PH_LOCK_ALARM

Bit	Name	Description
7	-	Reserved.
6	IN4_FREQ_HARD_ALARM	This bit indicates whether IN4 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
5	IN4_NO_ACTIVITY_ALARM	This bit indicates whether IN4 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN4_PH_LOCK_ALARM	This bit indicates whether IN4 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	-	Reserved.
2	IN3_FREQ_HARD_ALARM	This bit indicates whether IN3 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
1	IN3_NO_ACTIVITY_ALARM	This bit indicates whether IN3 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN3_PH_LOCK_ALARM	This bit indicates whether IN3 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

IN5_IN6_STS - Input Clock 5 & 6 Status

Address: 45H
Type: Read
Default Value: X110X110

7	6	5	4	3	2	1	0
-	IN6_FREQ_HARD_ALARM	IN6_NO_ACTIVITY_ALARM	IN6_PH_LOCK_ALARM	-	IN5_FREQ_HARD_ALARM	IN5_NO_ACTIVITY_ALARM	IN5_PH_LOCK_ALARM

Bit	Name	Description
7	-	Reserved.
6	IN6_FREQ_HARD_ALARM	This bit indicates whether IN6 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
5	IN6_NO_ACTIVITY_ALARM	This bit indicates whether IN6 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN6_PH_LOCK_ALARM	This bit indicates whether IN6 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	-	Reserved.
2	IN5_FREQ_HARD_ALARM	This bit indicates whether IN5 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
1	IN5_NO_ACTIVITY_ALARM	This bit indicates whether IN5 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN5_PH_LOCK_ALARM	This bit indicates whether IN5 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

IN7_IN8_STS - Input Clock 7 & 8 Status

Address: 46H
Type: Read
Default Value: X110X110

7	6	5	4	3	2	1	0
-	IN8_FREQ_HARD_ALARM	IN8_NO_ACTIVITY_ALARM	IN8_PH_LOCK_ALARM	-	IN7_FREQ_HARD_ALARM	IN7_NO_ACTIVITY_ALARM	IN7_PH_LOCK_ALARM

Bit	Name	Description
7	-	Reserved.
6	IN8_FREQ_HARD_ALARM	This bit indicates whether IN8 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
5	IN8_NO_ACTIVITY_ALARM	This bit indicates whether IN8 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN8_PH_LOCK_ALARM	This bit indicates whether IN8 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	-	Reserved.
2	IN7_FREQ_HARD_ALARM	This bit indicates whether IN7 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
1	IN7_NO_ACTIVITY_ALARM	This bit indicates whether IN7 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN7_PH_LOCK_ALARM	This bit indicates whether IN7 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

IN9_IN10_STS - Input Clock 9 & 10 Status

Address: 47H
Type: Read
Default Value: X110X110

7	6	5	4	3	2	1	0
-	IN10_FREQ_HARD_ALARM	IN10_NO_ACTIVITY_ALARM	IN10_PH_LOCK_ALARM	-	IN9_FREQ_HARD_ALARM	IN9_NO_ACTIVITY_ALARM	IN9_PH_LOCK_ALARM

Bit	Name	Description
7	-	Reserved.
6	IN10_FREQ_HARD_ALARM	This bit indicates whether IN10 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
5	IN10_NO_ACTIVITY_ALARM	This bit indicates whether IN10 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN10_PH_LOCK_ALARM	This bit indicates whether IN10 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	-	Reserved.
2	IN9_FREQ_HARD_ALARM	This bit indicates whether IN9 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
1	IN9_NO_ACTIVITY_ALARM	This bit indicates whether IN9 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN9_PH_LOCK_ALARM	This bit indicates whether IN9 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

IN11_IN12_STS - Input Clock 11 & 12 Status

Address: 48H
Type: Read
Default Value: X110X110

7	6	5	4	3	2	1	0
-	IN12_FREQ_HARD_ALARM	IN12_NO_ACTIVITY_ALARM	IN12_PH_LOCK_ALARM	-	IN11_FREQ_HARD_ALARM	IN11_NO_ACTIVITY_ALARM	IN11_PH_LOCK_ALARM

Bit	Name	Description
7	-	Reserved.
6	IN12_FREQ_HARD_ALARM	This bit indicates whether IN12 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
5	IN12_NO_ACTIVITY_ALARM	This bit indicates whether IN12 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN12_PH_LOCK_ALARM	This bit indicates whether IN12 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	-	Reserved.
2	IN11_FREQ_HARD_ALARM	This bit indicates whether IN11 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
1	IN11_NO_ACTIVITY_ALARM	This bit indicates whether IN11 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN11_PH_LOCK_ALARM	This bit indicates whether IN11 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

IN13_IN14_STS - Input Clock 13 & 14 Status

Address: 49H
Type: Read
Default Value: X110X110

7	6	5	4	3	2	1	0
-	IN14_FREQ_HARD_ALARM	IN14_NO_ACTIVITY_ALARM	IN14_PH_LOCK_ALARM	-	IN13_FREQ_HARD_ALARM	IN13_NO_ACTIVITY_ALARM	IN13_PH_LOCK_ALARM

Bit	Name	Description
7	-	Reserved.
6	IN14_FREQ_HARD_ALARM	This bit indicates whether IN14 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
5	IN14_NO_ACTIVITY_ALARM	This bit indicates whether IN14 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN14_PH_LOCK_ALARM	This bit indicates whether IN14 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	-	Reserved.
2	IN13_FREQ_HARD_ALARM	This bit indicates whether IN13 is in frequency hard alarm status. 0: No frequency hard alarm. 1: In frequency hard alarm status. (default)
1	IN13_NO_ACTIVITY_ALARM	This bit indicates whether IN13 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN13_PH_LOCK_ALARM	This bit indicates whether IN13 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘0’, this bit is cleared by writing ‘1’ to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is ‘1’, this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

7.2.5 T0 / T4 DPLL INPUT CLOCK SELECTION REGISTERS

INPUT_VALID1_STS - Input Clocks Validity 1

Address: 4AH
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1

Bit	Name	Description
7 - 0	INn	This bit indicates the validity of the corresponding INn. Here n is any one of 8 to 1. 0: Invalid. (default) 1: Valid.

INPUT_VALID2_STS - Input Clocks Validity 2

Address: 4BH
Type: Read
Default Value: XX000000

7	6	5	4	3	2	1	0
-	-	IN14	IN13	IN12	IN11	IN10	IN9

Bit	Name	Description
7 - 6	-	Reserved.
5 - 0	INn	This bit indicates the validity of the corresponding INn. Here n is any one of 14 to 9. 0: Invalid. (default) 1: Valid.

REMOTE_INPUT_VALID1_CNFG - Input Clocks Validity Configuration 1

Address: 4CH
Type: Read / Write
Default Value: 11111111

7	6	5	4	3	2	1	0
IN8_VALID	IN7_VALID	IN6_VALID	IN5_VALID	IN4_VALID	IN3_VALID	IN2_VALID	IN1_VALID

Bit	Name	Description
7 - 0	INn_VALID	This bit controls whether the corresponding INn is allowed to be locked for automatic selection. Here n is any one of 8 to 1. 0: Enabled. 1: Disabled. (default)

REMOTE_INPUT_VALID2_CNFG - Input Clocks Validity Configuration 2

Address: 4DH
Type: Read / Write
Default Value: XX111111

7	6	5	4	3	2	1	0
-	-	IN14_VALID	IN13_VALID	IN12_VALID	IN11_VALID	IN10_VALID	IN9_VALID

Bit	Name	Description
7 - 6	-	Reserved.
5 - 0	INn_VALID	This bit controls whether the corresponding INn is allowed to be locked for automatic selection. Here n is any one of 14 to 9. 0: Enabled. 1: Disabled. (default)

PRIORITY_TABLE1_STS - Priority Status 1 *

Address: 4EH
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
HIGHEST_PRIORITY_VALIDATED3	HIGHEST_PRIORITY_VALIDATED2	HIGHEST_PRIORITY_VALIDATED1	HIGHEST_PRIORITY_VALIDATED0	CURRENTLY_SELECTED_INPUT3	CURRENTLY_SELECTED_INPUT2	CURRENTLY_SELECTED_INPUT1	CURRENTLY_SELECTED_INPUT0

Bit	Name	Description
7 - 4	HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the highest priority. 0000: No input clock is qualified. (default) 0001: IN1. 0010: IN2. ...... 1101: IN13. 1110: IN14. 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b7-0, 4CH) or INn (b5-0, 4DH) bit is ‘0’.
3 - 0	CURRENTLY_SELECTED_INPUT[3:0]	These bits indicate the T0/T4 selected input clock. 0000: No input clock is selected; or the T4 selected input clock is the T0 DPLL output. (default) 0001: IN1 is selected. 0010: IN2 is selected. ...... 1101: IN13 is selected. 1110: IN14 is selected. 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b7-0, 4CH) or INn (b5-0, 4DH) bit is ‘0’.

PRIORITY_TABLE2_STS - Priority Status 2 *

Address: 4FH
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
THIRD_HIGHEST_PRIORITY_VALIDATED3	THIRD_HIGHEST_PRIORITY_VALIDATED2	THIRD_HIGHEST_PRIORITY_VALIDATED1	THIRD_HIGHEST_PRIORITY_VALIDATED0	SECOND_HIGHEST_PRIORITY_VALIDATED3	SECOND_HIGHEST_PRIORITY_VALIDATED2	SECOND_HIGHEST_PRIORITY_VALIDATED1	SECOND_HIGHEST_PRIORITY_VALIDATED0

Bit	Name	Description
7 - 4	THIRD_HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the third highest priority. 0000: No input clock is qualified. (default) 0001: IN1. 0010: IN2. ...... 1101: IN13. 1110: IN14. 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b7-0, 4CH) or INn (b5-0, 4DH) bit is ‘0’.
3 - 0	SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the second highest priority. 0000: No input clock is qualified. (default) 0001: IN1. 0010: IN2. ...... 1101: IN13. 1110: IN14. 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b7-0, 4CH) or INn (b5-0, 4DH) bit is ‘0’.

T0_INPUT_SEL_CNFG - T0 Selected Input Clock Configuration

Address: 50H
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	T0_INPUT_SEL3	T0_INPUT_SEL2	T0_INPUT_SEL1	T0_INPUT_SEL0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	T0_INPUT_SEL[3:0]	This bit determines T0 input clock selection. It is valid only when the EXT_SW bit (b4, 0BH) is ‘0’. 0000: Automatic selection. (default) 0001: Forced selection - IN1 is selected. 0010: Forced selection - IN2 is selected. ...... 1101: Forced selection - IN13 is selected. 1110: Forced selection - IN14 is selected. 1111: Reserved.

T4_INPUT_SEL_CNFG - T4 Selected Input Clock Configuration

Address: 51H
Type: Read / Write
Default Value: X0000000

7	6	5	4	3	2	1	0
-	T4_LOCK_T0	T0_FOR_T4	T4_TEST_T0_PH	T4_INPUT_SEL3	T4_INPUT_SEL2	T4_INPUT_SEL1	T4_INPUT_SEL0

Bit	Name	Description
7	-	Reserved.
6	T4_LOCK_T0	This bit determines whether the T4 DPLL locks to a T0 DPLL output or locks independently from the T0 DPLL. 0: Independently from the T0 path. (default) 1: Locks to a 77.76 MHz or 8 kHz signal from the T0 DPLL 77.76 MHz path.
5	T0_FOR_T4	This bit is valid only when the T4_LOCK_T0 bit (b6, 51H) is ‘1’. It determines whether a 77.76 MHz or 8 kHz signal from the T0 DPLL 77.76 MHz path is selected by the T4 DPLL. 0: 77.76 MHz. (default) 1: 8 kHz.
4	T4_TEST_T0_PH	This bit determines whether T4 selected input clock is compared with the feedback signal of the T4 DPLL for T4 DPLL locking or is compared with the T0 selected input clock to get the phase difference between T0 and T4 selected input clocks. 0: The T4 DPLL output. (default) 1: The T0 selected input clock.
3 - 0	T4_INPUT_SEL[3:0]	These bits are valid only when the T4_LOCK_T0 bit (b6, 51H) is ‘0’. They determines the T4 DPLL input clock selection. 0000: Automatic selection. (default) 0001: Forced selection - IN1 is selected. 0010: Forced selection - IN2 is selected. ...... 1101: Forced selection - IN13 is selected. 1110: Forced selection - IN14 is selected. 1111: Reserved.

7.2.6 T0 / T4 DPLL STATE MACHINE CONTROL REGISTERS

OPERATING_STS - DPLL Operating Status

Address: 52H
Type: Read
Default Value: 10000001

7	6	5	4	3	2	1	0
EX_SYNC_ALARM_MON	T4_DPLL_LOCK	T0_DPLL_SOFT_FREQ_ALARM	T4_DPLL_SOFT_FREQ_ALARM	T0_DPLL_LOCK	T0_DPLL_OPERATING_MODE2	T0_DPLL_OPERATING_MODE1	T0_DPLL_OPERATING_MODE0

Bit	Name	Description
7	EX_SYNC_ALARM_MON	This bit indicates whether the frame sync input signal is in external sync alarm status. 0: No external sync alarm. 1: In external sync alarm status. (default)
6	T4_DPLL_LOCK	This bit indicates the T4 DPLL locking status. 0: Unlocked. (default) 1: Locked.
5	T0_DPLL_SOFT_FREQ_ALARM	This bit indicates whether the T0 DPLL is in soft alarm status. 0: No T0 DPLL soft alarm. (default) 1: In T0 DPLL soft alarm status.
4	T4_DPLL_SOFT_FREQ_ALARM	This bit indicates whether the T4 DPLL is in soft alarm status. 0: No T4 DPLL soft alarm. (default) 1: In T4 DPLL soft alarm status.
3	T0_DPLL_LOCK	This bit indicates the T0 DPLL locking status. 0: Unlocked. (default) 1: Locked.
2 - 0	T0_DPLL_OPERATING_MODE[2:0]	These bits indicate the current operating mode of T0 DPLL. 000: Reserved. 001: Free-Run. (default) 010: Holdover. 011: Reserved. 100: Locked. 101: Pre-Locked2. 110: Pre-Locked. 111: Lost-Phase.

T0_OPERATING_MODE_CNFG - T0 DPLL Operating Mode Configuration

Address: 53H
Type: Read / Write
Default Value: XXXXX000

7	6	5	4	3	2	1	0
-	-	-	-	-	T0_OPERATING_MODE2	T0_OPERATING_MODE1	T0_OPERATING_MODE0

Bit	Name	Description
7 - 3	-	Reserved.
2 - 0	T0_OPERATING_MODE[2:0]	These bits control the T0 DPLL operating mode. 000: Automatic. (default) 001: Forced - Free-Run. 010: Forced - Holdover. 011: Reserved. 100: Forced - Locked. 101: Forced - Pre-Locked2. 110: Forced - Pre-Locked. 111: Forced - Lost-Phase.

T4_OPERATING_MODE_CNFG - T4 DPLL Operating Mode Configuration

Address: 54H
Type: Read / Write
Default Value: XXXXX000

7	6	5	4	3	2	1	0
-	-	-	-	-	T4_OPERATING_MODE2	T4_OPERATING_MODE1	T4_OPERATING_MODE0

Bit	Name	Description
7 - 3	-	Reserved.
2 - 0	T4_OPERATING_MODE[2:0]	These bits control the T4 DPLL operating mode. 000: Automatic. (default) 001: Forced - Free-Run. 010: Forced - Holdover. 011: Reserved. 100: Forced - Locked. 101, 110, 111: Reserved.

7.2.7 T0 / T4 DPLL & APLL CONFIGURATION REGISTERS

T0_DPLL_APLL_PATH_CNFG - T0 DPLL & APLL Path Configuration

Address: 55H
Type: Read / Write
Default Value: 00000X0X

7	6	5	4	3	2	1	0
T0_APLL_-PATH3	T0_APLL_-PATH2	T0_APLL_-PATH1	T0_APLL_-PATH0	T0_GSM_OBSA-I_16E1_16T1_-SEL1	T0_GSM_OBSA-I_16E1_16T1_-SEL0	T0_12E1_24T1_E3_T3_SEL1	T0_12E1_24T1_E3_T3_SEL0

Bit	Name	Description
7 - 4	T0_APLL_PATH[3:0]	These bits select an input to the T0 APLL. 0000: The output of T0 DPLL 77.76 MHz path. (default) 0001: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0010: The output of T0 DPLL 16E1/16T1 path. 0011: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 0100: The output of T4 DPLL 77.76 MHz path. 0101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T4 DPLL 16E1/16T1 path. 0111: The output of T4 DPLL GSM/GPS/16E1/16T1 path. 1XXX: Reserved.
3 - 2	T0_GSM_OBSAI_16E1_16T1_SEL[1:0]	These bits select an output clock from the T0 DPLL GSM/OBSAI/16E1/16T1 path. 00: 16E1. 01: 16T1. 10: GSM. 11: OBSAI. The default value of the T0_GSM_OBSAI_16E1_16T1_SEL0 bit is determined by the SONET/$\overline{\text{SDH}}$ pin during reset.
1 - 0	T0_12E1_24T1_E3_T3_SEL[1:0]	These bits select an output clock from the T0 DPLL 12E1/24T1/E3/T3 path. 00: 12E1. 01: 24T1. 10: E3. 11: T3. The default value of the T0_12E1_24T1_E3_T3_SEL0 bit is determined by the SONET/$\overline{\text{SDH}}$ pin during reset.

T0_DPLL_START_BW_DAMPING_CNFG - T0 DPLL Start Bandwidth & Damping Factor Configuration

Address: 56H
Type: Read / Write
Default Value: 01101111

7	6	5	4	3	2	1	0
T0_DPLL_START_DAMPING2	T0_DPLL_START_DAMPING1	T0_DPLL_START_DAMPING0	T0_DPLL_START_BW4	T0_DPLL_START_BW3	T0_DPLL_START_BW2	T0_DPLL_START_BW1	T0_DPLL_START_BW0

Bit	Name	Description
7 - 5	T0_DPLL_START_DAMPING[2:0]	These bits set the starting damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_START_BW[4:0]	These bits set the starting bandwidth for T0 DPLL. 00000: 0.5 mHz. 00001: 1 mHz. 00010: 2 mHz. 00011: 4 mHz. 00100: 8 mHz. 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_DPLL_ACQ_BW_DAMPING_CNFG - T0 DPLL Acquisition Bandwidth & Damping Factor Configuration

Address: 57H
Type: Read / Write
Default Value: 01101111

7	6	5	4	3	2	1	0
T0_DPLL_ACQ_DAMPING2	T0_DPLL_ACQ_DAMPING1	T0_DPLL_ACQ_DAMPING0	T0_DPLL_ACQ_BW4	T0_DPLL_ACQ_BW3	T0_DPLL_ACQ_BW2	T0_DPLL_ACQ_BW1	T0_DPLL_ACQ_BW0

Bit	Name	Description
7 - 5	T0_DPLL_ACQ_DAMPING[2:0]	These bits set the acquisition damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_ACQ_BW[4:0]	These bits set the acquisition bandwidth for T0 DPLL. 00000: 0.5 mHz. 00001: 1 mHz. 00010: 2 mHz. 00011: 4 mHz. 00100: 8 mHz. 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_DPLL_LOCKED_BW_DAMPING_CNFG - T0 DPLL Locked Bandwidth & Damping Factor Configuration

Address: 58H
Type: Read / Write
Default Value: 01101011

7	6	5	4	3	2	1	0
T0_DPLL_LOCKED_DAMPING2	T0_DPLL_LOCKED_DAMPING1	T0_DPLL_LOCKED_DAMPING0	T0_DPLL_LOCKED_BW4	T0_DPLL_LOCKED_BW3	T0_DPLL_LOCKED_BW2	T0_DPLL_LOCKED_BW1	T0_DPLL_LOCKED_BW0

Bit	Name	Description
7 - 5	T0_DPLL_LOCKED_DAMPING[2:0]	These bits set the locked damping factor for T0 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	T0_DPLL_LOCKED_BW[4:0]	These bits set the locked bandwidth for T0 DPLL. 00000: 0.5 mHz. 00001: 1 mHz. 00010: 2 mHz. 00011: 4 mHz. 00100: 8 mHz. 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. (default) 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

T0_BW_OVERSHOOT_CNFG - T0 DPLL Bandwidth Overshoot Configuration

Address: 59H
Type: Read / Write
Default Value: 1XXX1XXX

7	6	5	4	3	2	1	0
AUTO_BW_SEL	-	-	-	T0_LIMT	-	-	-

Bit	Name	Description
7	AUTO_BW_SEL	This bit determines whether starting or acquisition bandwidth / damping factor is used for T0 DPLL. 0: The starting and acquisition bandwidths / damping factors are not used. Only the locked bandwidth / damping factor is used regardless of the T0 DPLL locking stage. 1: The starting, acquisition or locked bandwidth / damping factor is used automatically depending on different T0 DPLL locking stages. (default)
6 - 4	-	Reserved.
3	T0_LIMT	This bit determines whether the integral path value is frozen when the T0 DPLL hard limit is reached. 0: Not frozen. 1: Frozen. It will minimize the subsequent overshoot when T0 DPLL is pulling in. (default)
2 - 0	-	Reserved.

PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration *

Address: 5AH
Type: Read / Write
Default Value: 10000101

7	6	5	4	3	2	1	0
COARSE_PH_LOS_LIMT_EN	WIDE_EN	MULTI_PH_APP	MULTI_PH_8K_4K_2K_EN	PH_LOS_COARSE_LIMT3	PH_LOS_COARSE_LIMT2	PH_LOS_COARSE_LIMT1	PH_LOS_COARSE_LIMT0

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>COARSE_PH_LOS_LIMT_EN</td><td>This bit controls whether the occurrence of the coarse phase loss will result in the T0/T4 DPLL unlocked.
0: Disabled.
1: Enabled. (default)</td></tr>
<tr><td>6</td><td>WIDE_EN</td><td>Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH).</td></tr>
<tr><td>5</td><td>MULTI_PH_APP</td><td>This bit determines whether the PFD output of T0/T4 DPLL is limited to ±1 UI or is limited to the coarse phase limit.
0: Limited to ±1 UI. (default)
1: Limited to the coarse phase limit. When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits; when the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH) for details.</td></tr>
<tr><td>4</td><td>MULTI_PH_8K_4K_2K_EN</td><td>This bit, together with the WIDE_EN bit (b6, 5AH) and the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH), determines the coarse phase limit when the selected input clock is of 2 kHz, 4 kHz or 8 kHz. When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits.
<table>
<tr><th>Selected Input Clock</th><th>MULTI_PH_8K_4K_2K_EN</th><th>WIDE_EN</th><th>Coarse Phase Limit</th></tr>
<tr><td rowspan="3">2 kHz, 4 kHz or 8 kHz</td><td>0</td><td>don't-care</td><td>±1 UI</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>±1 UI</td></tr>
<tr><td>1</td><td>set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).</td></tr>
<tr><td rowspan="2">other than 2 kHz, 4 kHz and 8 kHz</td><td rowspan="2">don't-care</td><td>0</td><td>±1 UI</td></tr>
<tr><td>1</td><td>set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).</td></tr>
</table>
</td></tr>
<tr><td>3 - 0</td><td>PH_LOS_COARSE_LIMT[3:0]</td><td>These bit set the coarse phase limit. The limit is used only in some cases. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH).
0000: ±1 UI.
0001: ±3 UI.
0010: ±7 UI.
0011: ±15 UI.
0100: ±31 UI.
0101: ±63 UI. (default)
0110: ±127 UI.
0111: ±255 UI.
1000: ±511 UI.
1001: ±1023 UI (T0); Reserved (T4).
1010-1111: Reserved.</td></tr>
</table>

PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration *

Address: 5BH
Type: Read / Write
Default Value: 10XXX010

7	6	5	4	3	2	1	0
FINE_PH_LOS_LIMT_EN	FAST_LOS_SW	-	-	-	PH_LOS_FINE_LIMT2	PH_LOS_FINE_LIMT1	PH_LOS_FINE_LIMT0

Bit	Name	Description
7	FINE_PH_LOS_LIMT_EN	This bit controls whether the occurrence of the fine phase loss will result in the T0/T4 DPLL unlocked. 0: Disabled. 1: Enabled. (default)
6	FAST_LOS_SW	The value in this bit can be switched only when it is available for T0 path; this bit is always ‘1’ when it is available for T4 path. This bit controls whether the occurrence of the fast loss will result in the T0/T4 DPLL unlocked. 0: Does not result in the T0 DPLL unlocked. T0 DPLL will enter Temp-Holdover mode automatically. (default) 1: Results in the T0/T4 DPLL unlocked. For T0 path, T0 DPLL will enter Lost-Phase mode if the T0 DPLL operating mode is switched automatically.
5 - 3	-	Reserved.
2 - 0	PH_LOS_FINE_LIMT[2:0]	These bits set a fine phase limit. 000: 0. 001: ± (45 ° ~ 90 °). 010: ± (90 ° ~ 180 °). (default) 011: ± (180 ° ~ 360 °). 100: ± (20 ns ~ 25 ns). 101: ± (60 ns ~ 65 ns). 110: ± (120 ns ~ 125 ns). 111: ± (950 ns ~ 955 ns).

T0_HOLDOVER_MODE_CNFG - T0 DPLL Holdover Mode Configuration

Address: 5CH
Type: Read / Write
Default Value: 010001XX

7	6	5	4	3	2	1	0
MAN_HOLDOVER	AUTO_AVG	FAST_AVG	READ_AVG	TEMP_HOLDOVER_MODE1	TEMP_HOLDOVER_MODE0	-	-

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>MAN_HOLDOVER</td><td>Refer to the description of the FAST_AVG bit (b5, 5CH).</td></tr>
<tr><td>6</td><td>AUTO_AVG</td><td>Refer to the description of the FAST_AVG bit (b5, 5CH).</td></tr>
<tr><td>5</td><td>FAST_AVG</td><td>This bit, together with the AUTO_AVG bit (b6, 5CH) and the MAN_HOLDOVER bit (b7, 5CH), determines a frequency offset acquiring method in T0 DPLL Holdover Mode.
<table>
<tr><th>MAN_HOLDOVER</th><th>AUTO_AVG</th><th>FAST_AVG</th><th>Frequency Offset Acquiring Method</th></tr>
<tr><td rowspan="3">0</td><td>0</td><td>don’t-care</td><td>Automatic Instantaneous</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>Automatic Slow Averaged (default)</td></tr>
<tr><td>1</td><td>Automatic Fast Averaged</td></tr>
<tr><td>1</td><td colspan="2">don’t-care</td><td>Manual</td></tr>
</table>
</td></tr>
<tr><td>4</td><td>READ_AVG</td><td>This bit controls the holdover frequency offset reading, which is read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH).
0: The value read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is equal to the one written to them. (default)
1: The value read from the T0_HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is not equal to the one written to them. The value is acquired by Automatic Slow Averaged method if the FAST_AVG bit (b5, 5CH) is ‘0’; or is acquired by Automatic Fast Averaged method if the FAST_AVG bit (b5, 5CH) is ‘1’.</td></tr>
<tr><td>3 - 2</td><td>TEMP_HOLDOVER_MODE[1:0]</td><td>These bits determine the frequency offset acquiring method in T0 DPLL Temp-Holdover Mode.
00: The method is the same as that used in T0 DPLL Holdover mode.
01: Automatic Instantaneous. (default)
10: Automatic Fast Averaged.
11: Automatic Slow Averaged.</td></tr>
<tr><td>1 - 0</td><td>-</td><td>Reserved.</td></tr>
</table>

T0_HOLDOVER_FREQ[7:0]_CNFG - T0 DPLL Holdover Frequency Configuration 1

Address: 5DH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
T0_HOLDOVER_FREQ7	T0_HOLDOVER_FREQ6	T0_HOLDOVER_FREQ5	T0_HOLDOVER_FREQ4	T0_HOLDOVER_FREQ3	T0_HOLDOVER_FREQ2	T0_HOLDOVER_FREQ1	T0_HOLDOVER_FREQ0

Bit	Name	Description
7 - 0	T0_HOLDOVER_FREQ[7:0]	Refer to the description of the T0_HOLDOVER_FREQ[23:16] bits (b7~0, 5FH).

T0_HOLDOVER_FREQ[15:8]_CNFG - T0 DPLL Holdover Frequency Configuration 2

Address: 5EH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
T0_HOLDOVER_FREQ15	T0_HOLDOVER_FREQ14	T0_HOLDOVER_FREQ13	T0_HOLDOVER_FREQ12	T0_HOLDOVER_FREQ11	T0_HOLDOVER_FREQ10	T0_HOLDOVER_FREQ9	T0_HOLDOVER_FREQ8

Bit	Name	Description
7 - 0	T0_HOLDOVER_FREQ[15:8]	Refer to the description of the T0_HOLDOVER_FREQ[23:16] bits (b7~0, 5FH).

T0_HOLDOVER_FREQ[23:16]_CNFG - T0 DPLL Holdover Frequency Configuration 3

Address: 5FH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
T0_HOLDOVER_FREQ23	T0_HOLDOVER_FREQ22	T0_HOLDOVER_FREQ21	T0_HOLDOVER_FREQ20	T0_HOLDOVER_FREQ19	T0_HOLDOVER_FREQ18	T0_HOLDOVER_FREQ17	T0_HOLDOVER_FREQ16

Bit	Name	Description
7 - 0	T0_HOLDOVER_FREQ[23:16]	The T0_HOLDOVER_FREQ[23:0] bits represent a 2's complement signed integer. In T0 DPLL Holdover mode, the value written to these bits multiplied by 0.000011 is the frequency offset set manually; the value read from these bits multiplied by 0.000011 is the frequency offset automatically slow or fast averaged or manually set, as determined by the READ_AVG bit (b4, 5CH) and the FAST_AVG bit (b5, 5CH).

T4_DPLL_APLL_PATH_CNFG - T4 DPLL & APLL Path Configuration

Address: 60H
Type: Read / Write
Default Value: 01000X0X

7	6	5	4	3	2	1	0
T4_APLL_-PATH3	T4_APLL_-PATH2	T4_APLL_-PATH1	T4_APLL_-PATH0	T4_GSM_G-PS_16E1_16T1_-SEL1	T4_GSM_G-PS_16E1_16T1_-SEL0	T4_12E1_24T1_E3_T3_SEL1	T4_12E1_24T1_E3_T3_SEL0

Bit	Name	Description
7 - 4	T4_APLL_PATH[3:0]	These bits select an input to the T4 APLL. 0000: The output of T0 DPLL 77.76 MHz path. 0001: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0010: The output of T0 DPLL 16E1/16T1 path. 0011: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 0100: The output of T4 DPLL 77.76 MHz path. (default) 0101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T4 DPLL 16E1/16T1 path. 0111: The output of T4 DPLL GSM/GPS/16E1/16T1 path. 1XXX: Reserved.
3 - 2	T4_GSM_GPS_16E1_16T1_SEL[1:0]	These bits select an output clock from the T4 DPLL GSM/GPS/16E1/16T1 path. 00: 16E1. 01: 16T1. 10: GSM. 11: GPS. The default value of the T0_GSM_GPS_16E1_16T1_SEL0 bit is determined by the SONET/$\overline{\text{SDH}}$ pin during reset.
1 - 0	T4_12E1_24T1_E3_T3_SEL[1:0]	These bits select an output clock from the T4 DPLL 12E1/24T1/E3/T3 path. 00: 12E1. 01: 24T1. 10: E3. 11: T3. The default value of the T4_12E1_24T1_E3_T3_SEL0 bit is determined by the SONET/$\overline{\text{SDH}}$ pin during reset.

T4_DPLL_LOCKED_BW_DAMPING_CNFG - T4 DPLL Locked Bandwidth & Damping Factor Configuration

Address: 61H
Type: Read / Write
Default Value: 011XXX00

7	6	5	4	3	2	1	0
T4_DPLL_LOCKED_DAMPING2	T4_DPLL_LOCKED_DAMPING1	T4_DPLL_LOCKED_DAMPING0	-	-	-	T4_DPLL_LOCKED_BW1	T4_DPLL_LOCKED_BW0

Bit	Name	Description
7 - 5	T4_DPLL_LOCKED_DAMPING[2:0]	These bits set the locked damping factor for T4 DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 2	-	Reserved.
1 - 0	T4_DPLL_LOCKED_BW[1:0]	These bits set the locked bandwidth for T4 DPLL. 00: 18 Hz. (default) 01: 35 Hz. 10: 70 Hz. 11: 560 Hz.

CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1 *

Address: 62H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_DPLL_FREQ7	CURRENT_DPLL_FREQ6	CURRENT_DPLL_FREQ5	CURRENT_DPLL_FREQ4	CURRENT_DPLL_FREQ3	CURRENT_DPLL_FREQ2	CURRENT_DPLL_FREQ1	CURRENT_DPLL_FREQ0

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[7:0]	Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H).

CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2 *

Address: 63H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_DPLL_FREQ15	CURRENT_DPLL_FREQ14	CURRENT_DPLL_FREQ13	CURRENT_DPLL_FREQ12	CURRENT_DPLL_FREQ11	CURRENT_DPLL_FREQ10	CURRENT_DPLL_FREQ9	CURRENT_DPLL_FREQ8

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[15:8]	Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H).

CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3 *

Address: 64H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_DPLL_FREQ23	CURRENT_DPLL_FREQ22	CURRENT_DPLL_FREQ21	CURRENT_DPLL_FREQ20	CURRENT_DPLL_FREQ19	CURRENT_DPLL_FREQ18	CURRENT_DPLL_FREQ17	CURRENT_DPLL_FREQ16

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[23:16]	The CURRENT_DPLL_FREQ[23:0] bits represent a 2's complement signed integer. If the value in these bits is multiplied by 0.000011, the current frequency offset of the T0/T4 DPLL output in ppm with respect to the master clock will be gotten.

DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration

Address: 65H
Type: Read / Write
Default Value: 10001100

7	6	5	4	3	2	1	0
FREQ_LIMT_PH_LOS	DPLL_FREQ_SOFT_LIMT6	DPLL_FREQ_SOFT_LIMT5	DPLL_FREQ_SOFT_LIMT4	DPLL_FREQ_SOFT_LIMT3	DPLL_FREQ_SOFT_LIMT2	DPLL_FREQ_SOFT_LIMT1	DPLL_FREQ_SOFT_LIMT0

Bit	Name	Description
7	FREQ_LIMT_PH_LOS	This bit determines whether the T0/T4 DPLL in hard alarm status will result in it unlocked. 0: Disabled. 1: Enabled. (default)
6 - 0	DPLL_FREQ_SOFT_LIMT[6:0]	These bits represent an unsigned integer. If the value is multiplied by 0.724, the DPLL soft limit for T0 and T4 paths in ppm will be gotten. The DPLL soft limit is symmetrical about zero.

DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1

Address: 66H
Type: Read / Write
Default Value: 10101011

7	6	5	4	3	2	1	0
DPLL_FREQ_HARD_LIMT7	DPLL_FREQ_HARD_LIMT6	DPLL_FREQ_HARD_LIMT5	DPLL_FREQ_HARD_LIMT4	DPLL_FREQ_HARD_LIMT3	DPLL_FREQ_HARD_LIMT2	DPLL_FREQ_HARD_LIMT1	DPLL_FREQ_HARD_LIMT0

Bit	Name	Description
7 - 0	DPLL_FREQ_HARD_LIMT[7:0]	Refer to the description of the DPLL_FREQ_HARD_LIMT[15:8] bits (b7~0, 67H).

DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2

Address: 67H
Type: Read / Write
Default Value: 00011001

7	6	5	4	3	2	1	0
DPLL_FREQ_HARD_LIMT15	DPLL_FREQ_HARD_LIMT14	DPLL_FREQ_HARD_LIMT13	DPLL_FREQ_HARD_LIMT12	DPLL_FREQ_HARD_LIMT11	DPLL_FREQ_HARD_LIMT10	DPLL_FREQ_HARD_LIMT9	DPLL_FREQ_HARD_LIMT8

Bit	Name	Description
7 - 0	DPLL_FREQ_HARD_LIMT[15:8]	The DPLL_FREQ_HARD_LIMT[15:0] bits represent an unsigned integer. If the value is multiplied by 0.0014, the DPLL hard limit for T0 and T4 paths in ppm will be gotten. The DPLL hard limit is symmetrical about zero.

CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1 *

Address: 68H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_PH_DATA7	CURRENT_PH_DATA6	CURRENT_PH_DATA5	CURRENT_PH_DATA4	CURRENT_PH_DATA3	CURRENT_PH_DATA2	CURRENT_PH_DATA1	CURRENT_PH_DATA0

Bit	Name	Description
7 - 0	CURRENT_PH_DATA[7:0]	Refer to the description of the CURRENT_PH_DATA[15:8] bits (b7~0, 69H).

CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2 *

Address: 69H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_PH_DATA15	CURRENT_PH_DATA14	CURRENT_PH_DATA13	CURRENT_PH_DATA12	CURRENT_PH_DATA11	CURRENT_PH_DATA10	CURRENT_PH_DATA9	CURRENT_PH_DATA8

Bit	Name	Description
7 - 0	CURRENT_PH_DATA[15:8]	The CURRENT_PH_DATA[15:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.61, the averaged phase error of the T0/T4 DPLL feedback with respect to the selected input clock in ns will be gotten.

T0_T4_APLL_BW_CNFG - T0 / T4 APLL Bandwidth Configuration

Address: 6AH
Type: Read / Write
Default Value: XX01XX01

7	6	5	4	3	2	1	0
-	-	T0_APLL_BW1	T0_APLL_BW0	-	-	T4_APLL_BW1	T4_APLL_BW0

Bit	Name	Description
7 - 6	-	Reserved.
5 - 4	T0_APLL_BW[1:0]	These bits set the bandwidth for T0 APLL. 00: 100 kHz. 01: 500 kHz. (default) 10: 1 MHz. 11: 2 MHz.
3 - 2	-	Reserved.
1 - 0	T4_APLL_BW[1:0]	These bits set the bandwidth for T4 APLL. 00: 100 kHz. 01: 500 kHz. (default) 10: 1 MHz. 11: 2 MHz.

7.2.8 OUTPUT CONFIGURATION REGISTERS

OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration

Address: 6BH
Type: Read / Write
Default Value: 00001011

7	6	5	4	3	2	1	0
OUT1_PATH_SEL3	OUT1_PATH_SEL2	OUT1_PATH_SEL1	OUT1_PATH_SEL0	OUT1_DIVIDER3	OUT1_DIVIDER2	OUT1_DIVIDER1	OUT1_DIVIDER0

Bit	Name	Description
7 - 4	OUT1_PATH_SEL[3:0]	These bits select an input to OUT1. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.
3 - 0	OUT1_DIVIDER[3:0]	These bits select a division factor of the divider for OUT1. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT1_PATH_SEL[3:0] bits (b7~4, 6BH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 24 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 25 for the division factor selection.

OUT2_FREQ_CNFG - Output Clock 2 Frequency Configuration

Address: 6CH
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
OUT2_PATH_SEL3	OUT2_PATH_SEL2	OUT2_PATH_SEL1	OUT2_PATH_SEL0	OUT2_DIVIDER3	OUT2_DIVIDER2	OUT2_DIVIDER1	OUT2_DIVIDER0

Bit	Name	Description
7 - 4	OUT2_PATH_SEL[3:0]	These bits select an input to OUT2. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.
3 - 0	OUT2_DIVIDER[3:0]	These bits select a division factor of the divider for OUT2. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT2_PATH_SEL[3:0] bits (b7~4, 6CH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 24 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 25 for the division factor selection.

OUT3_FREQ_CNFG - Output Clock 3 Frequency Configuration

Address: 6DH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
OUT3_PATH_SEL3	OUT3_PATH_SEL2	OUT3_PATH_SEL1	OUT3_PATH_SEL0	OUT3_DIVIDER3	OUT3_DIVIDER2	OUT3_DIVIDER1	OUT3_DIVIDER0

Bit	Name	Description
7 - 4	OUT3_PATH_SEL[3:0]	These bits select an input to OUT3. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.
3 - 0	OUT3_DIVIDER[3:0]	These bits select a division factor of the divider for OUT3. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT3_PATH_SEL[3:0] bits (b7~4, 6DH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 24 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 25 for the division factor selection.

OUT4_FREQ_CNFG - Output Clock 4 Frequency Configuration

Address: 6EH
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
OUT4_PATH_SEL3	OUT4_PATH_SEL2	OUT4_PATH_SEL1	OUT4_PATH_SEL0	OUT4_DIVIDER3	OUT4_DIVIDER2	OUT4_DIVIDER1	OUT4_DIVIDER0

Bit	Name	Description
7 - 4	OUT4_PATH_SEL[3:0]	These bits select an input to OUT4. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.
3 - 0	OUT4_DIVIDER[3:0]	These bits select a division factor of the divider for OUT4. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT4_PATH_SEL[3:0] bits (b7~4, 6EH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 24 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 25 for the division factor selection.

OUT5_FREQ_CNFG - Output Clock 5 Frequency Configuration

Address: 6FH
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
OUT5_PATH_-SEL3	OUT5_PATH_-SEL2	OUT5_PATH_-SEL1	OUT5_PATH_-SEL0	OUT5_DIVID-ER3	OUT5_DIVID-ER2	OUT5_DIVID-ER1	OUT5_DIVID-ER0

Bit	Name	Description
7 - 4	OUT5_PATH_SEL[3:0]	These bits select an input to OUT5. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.
3 - 0	OUT5_DIVIDER[3:0]	These bits select a division factor of the divider for OUT5. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT5_PATH_SEL[3:0] bits (b7~4, 6FH)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 24 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 25 for the division factor selection.

OUT6_FREQ_CNFG - Output Clock 6 Frequency Configuration

Address:70H Type: Read / Write Default Value: 00000110

7	6	5	4	3	2	1	0
OUT6_PATH_-SEL3	OUT6_PATH_-SEL2	OUT6_PATH_-SEL1	OUT6_PATH_-SEL0	OUT6_DIVID-ER3	OUT6_DIVID-ER2	OUT6_DIVID-ER1	OUT6_DIVID-ER0

Bit	Name	Description
7 - 4	OUT6_PATH_SEL[3:0]	These bits select an input to OUT6. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.
3 - 0	OUT6_DIVIDER[3:0]	These bits select a division factor of the divider for OUT6. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT6_PATH_SEL[3:0] bits (b7~4, 70H)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 24 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 25 for the division factor selection.

OUT7_FREQ_CNFG - Output Clock 7 Frequency Configuration

Address:71H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
OUT7_PATH_SEL3	OUT7_PATH_SEL2	OUT7_PATH_SEL1	OUT7_PATH_SEL0	OUT7_DIVIDER3	OUT7_DIVIDER2	OUT7_DIVIDER1	OUT7_DIVIDER0

Bit	Name	Description
7 - 4	OUT7_PATH_SEL[3:0]	These bits select an input to OUT7. 0000 ~ 0011: The output of T0 APLL. (default: 0000) 0100: The output of T0 DPLL 77.76 MHz path. 0101: The output of T0 DPLL 12E1/24T1/E3/T3 path. 0110: The output of T0 DPLL 16E1/16T1 path. 0111: The output of T0 DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1011: The output of T4 APLL. 1100: The output of T4 DPLL 77.76 MHz path. 1101: The output of T4 DPLL 12E1/24T1/E3/T3 path. 1110: The output of T4 DPLL 16E1/16T1 path. 1111: The output of T4 DPLL GSM/GPS/16E1/16T1 path.
3 - 0	OUT7_DIVIDER[3:0]	These bits select a division factor of the divider for OUT7. The output frequency is determined by the division factor and the signal derived from T0/T4 DPLL or T0/T4 APLL output (selected by the OUT7_PATH_SEL[3:0] bits (b7~4, 71H)). If the signal is derived from one of the T0/T4 DPLL outputs, please refer to Table 24 for the division factor selection. If the signal is derived from the T0/T4 APLL output, please refer to Table 25 for the division factor selection.

OUT8_FREQ_CNFG - Output Clock 8 Frequency Configuration & Output Clock 6, 7 & 9 Invert Configuration

Address:72H
Type: Read / Write
Default Value: 01000000

7	6	5	4	3	2	1	0
OUT8_PATH_-SEL	OUT8_EN	T4_INPUT_-FAIL	AMI_OUT_DUTY	400HZ_SEL	OUT9_INV	OUT7_INV	OUT6_INV

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>OUT8_PATH_SEL</td><td>These bits select an input to OUT8.
0: The output of T4 DPLL 77.76 MHz path. (default)
1: The output of T0 DPLL 77.76 MHz path.</td></tr>
<tr><td>6</td><td>OUT8_EN</td><td>Refer to the description of the T4_INPUT_FAIL bit (b5, 72H).</td></tr>
<tr><td>5</td><td>T4_INPUT_FAIL</td><td>This bit, together with the OUT8_EN bit (b6, 72H), determines whether a clock is enabled to be output on OUT8.
<table>
<tr><th>OUT8_EN</th><th>T4_INPUT_FAIL</th><th>Output on OUT8</th></tr>
<tr><td>0</td><td>don't-care</td><td>Output is disabled (output low).</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>Output is enabled. (default)</td></tr>
<tr><td>1</td><td>Output is enabled when the T4 selected input clock does not fail.
Output is disabled (output low) when the T4 selected input clock fails.</td></tr>
</table>
</td></tr>
<tr><td>4</td><td>AMI_OUT_DUTY</td><td>This bit determines the duty cycle of the output on OUT8.
0: 50:50. (default)
1: 5:8.</td></tr>
<tr><td>3</td><td>400HZ_SEL</td><td>This bit determines the frequency of the output on OUT8.
0: 64 kHz + 8 kHz. (default)
1: 64 kHz + 8 kHz + 0.4 kHz.</td></tr>
<tr><td>2</td><td>OUT9_INV</td><td>This bit determines whether the output on OUT9 is inverted.
0: Not inverted. (default)
1: Inverted.</td></tr>
<tr><td>1</td><td>OUT7_INV</td><td>This bit determines whether the output on OUT7 is inverted.
0: Not inverted. (default)
1: Inverted.</td></tr>
<tr><td>0</td><td>OUT6_INV</td><td>This bit determines whether the output on OUT6 is inverted.
0: Not inverted. (default)
1: Inverted.</td></tr>
</table>

OUT9_FREQ_CNFG - Output Clock 9 Frequency Configuration & Output Clock 1 ~ 5 Invert Configuration

Address:73H
Type: Read / Write
Default Value: 01000000

7	6	5	4	3	2	1	0
OUT9_PATH_-SEL	OUT9_EN	T4_INPUT_-FAIL	OUT5_INV	OUT4_INV	OUT3_INV	OUT2_INV	OUT1_INV

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>OUT9_PATH_SEL</td><td>These bits select an input to OUT9.
0: The output of T4 DPLL 16E1/16T1 path. (default)
1: The output of T0 DPLL 16E1/16T1 path.</td></tr>
<tr><td>6</td><td>OUT9_EN</td><td>Refer to the description of the T4_INPUT_FAIL bit (b5, 73H).</td></tr>
<tr><td>5</td><td>T4_INPUT_FAIL</td><td>This bit, together with the OUT9_EN bit (b6, 73H), determines whether clock is enabled to output on OUT9.
<table>
<tr><th>OUT9_EN</th><th>T4_INPUT_FAIL</th><th>Output on OUT9</th></tr>
<tr><td>0</td><td>don’t-care</td><td>Output is disabled (output low).</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>Output is enabled. (default)</td></tr>
<tr><td>1</td><td>Output is enabled when the T4 selected input clock does not fail.
Output is disabled (output low) when the T4 selected input clock fails.
(Whether the T4 selected input clock is switched or not, as long as the T4 selected input clock does not change to be invalid, the T4 selected input clock does not fail).</td></tr>
</table></td></tr>
<tr><td>4</td><td>OUT5_INV</td><td>This bit determines whether the output on OUT5 is inverted.
0: Not inverted. (default)
1: Inverted.</td></tr>
<tr><td>3</td><td>OUT4_INV</td><td>This bit determines whether the output on OUT4 is inverted.
0: Not inverted. (default)
1: Inverted.</td></tr>
<tr><td>2</td><td>OUT3_INV</td><td>This bit determines whether the output on OUT3 is inverted.
0: Not inverted. (default)
1: Inverted.</td></tr>
<tr><td>1</td><td>OUT2_INV</td><td>This bit determines whether the output on OUT2 is inverted.
0: Not inverted. (default)
1: Inverted.</td></tr>
<tr><td>0</td><td>OUT1_INV</td><td>This bit determines whether the output on OUT1 is inverted.
0: Not inverted. (default)
1: Inverted.</td></tr>
</table>

FR_MFR_SYNC_CNFG - Frame Sync & Multiframe Sync Output Configuration

Address:74H
Type: Read / Write
Default Value: 01100000

7	6	5	4	3	2	1	0
IN_2K_4K_8K_INV	8K_EN	2K_EN	2K_8K_PUL_POSITION	8K_INV	8K_PUL	2K_INV	2K_PUL

Bit	Name	Description
7	IN_2K_4K_8K_INV	This bit determines whether the input clock is inverted before locked by the T0/T4 DPLL when the input clock is 2 kHz, 4 kHz or 8 kHz. 0: Not inverted. (default) 1: Inverted.
6	8K_EN	This bit determines whether an 8 kHz signal is enabled to be output on FRSYNC_8K. 0: Disabled. FRSYNC_8K outputs low. 1: Enabled. (default)
5	2K_EN	This bit determines whether a 2 kHz signal is enabled to be output on MFRSYNC_2K. 0: Disabled. MFRSYNC_2K outputs low. 1: Enabled. (default)
4	2K_8K_PUL_POSITION	This bit is valid only when FRSYNC_8K and/or MFRSYNC_2K output pulse; i.e., when one of the 8K_PUL bit (b2, 74H) and the 2K_PUL bit (b0, 74H) is ‘1’ or when the 8K_PUL bit (b2, 74H) and the 2K_PUL bit (b0, 74H) are both ‘1’. It determines the pulse position referring to the standard 50:50 duty cycle. 0: Pulsed on the falling edge of the standard 50:50 duty cycle position. (default) 1: Pulsed on the rising edge of the standard 50:50 duty cycle position.
3	8K_INV	This bit determines whether the output on FRSYNC_8K is inverted. 0: Not inverted. (default) 1: Inverted.
2	8K_PUL	This bit determines whether the output on FRSYNC_8K is 50:50 duty cycle or pulsed. 0: 50:50 duty cycle. (default) 1: Pulsed. The pulse width is defined by the period of the output on OUT3.
1	2K_INV	This bit determines whether the output on MFRSYNC_2K is inverted. 0: Not inverted. (default) 1: Inverted.
0	2K_PUL	This bit determines whether the output on MFRSYNC_2K is 50:50 duty cycle or pulsed. 0: 50:50 duty cycle. (default) 1: Pulsed. The pulse width is defined by the period of the output on OUT3.

7.2.9 PBO & PHASE OFFSET CONTROL REGISTERS

PHASE_MON_PBO_CNFG - Phase Transient Monitor & PBO Configuration

Address:78H
Type: Read / Write
Default Value: 0X000110

7	6	5	4	3	2	1	0
IN_NOISE_WINDOW	-	PH_MON_EN	PH_MON_PBO_EN	PH_TR_MON_LIMT3	PH_TR_MON_LIMT2	PH_TR_MON_LIMT1	PH_TR_MON_LIMT0

Bit	Name	Description
7	IN_NOISE_WINDOW	This bit determines whether the input clock whose edge respect to the reference clock is outside ±5% is enabled to be selected for T0/T4 DPLL. 0: Disabled. (default) 1: Enabled.
6	-	Reserved.
5	PH_MON_EN	This bit is valid only when the PH_MON_PBO_EN bit (b4, 78H) is ‘1’. It determines whether the Phase Transient Monitor is enabled to monitor the phase-time changes on the T0 selected input clock. 0: Disabled. (default) 1: Enabled.
4	PH_MON_PBO_EN	This bit determines whether a PBO event is triggered when the phase-time changes on the T0 selected input clock are greater than a programmable limit over an interval of less than 0.1 seconds with the PH_MON_EN bit being ‘1’. The limit is programmed by the PH_TR_MON_LIMT[3:0] bits (b3~0, 78H). 0: Disabled. (default) 1: Enabled.
3 - 0	PH_TR_MON_LIMT[3:0]	These bits represent an unsigned integer. The Phase Transient Monitor limit in ns can be calculated as follows: *Limit (ns) = (PH_TR_MON_LIMT[3:0] + 7) X 156.*

PHASE_OFFSET[7:0]_CNFG - Phase Offset Configuration 1

Address:7AH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
PH_OFFSET7	PH_OFFSET6	PH_OFFSET5	PH_OFFSET4	PH_OFFSET3	PH_OFFSET2	PH_OFFSET1	PH_OFFSET0

Bit	Name	Description
7 - 0	PH_OFFSET[7:0]	Refer to the description of the PH_OFFSET[9:8] bits (b1~0, 7BH).

PHASE_OFFSET[9:8]_CNFG - Phase Offset Configuration 2

Address:7BH
Type: Read / Write
Default Value: 0XXXXX00

7	6	5	4	3	2	1	0
PH_OFF-SET_EN	-	-	-	-	-	PH_OFFSET9	PH_OFFSET8

Bit	Name	Description
7	PH_OFFSET_EN	This bit determines whether the input-to-output phase offset is enabled. If the device is configured as the Master, the input-to-output phase offset: 0: Disabled. (default) 1: Enabled. If the device is configured as the Slave, the input-to-output phase offset is always enabled.
6 - 2	-	Reserved.
1 - 0	PH_OFFSET[9:8]	These bits represent a 2’s complement signed integer. If the value is multiplied by 0.61, the input-to-output phase offset in ns to adjust will be gotten.

7.2.10 SYNCHRONIZATION CONFIGURATION REGISTERS

SYNC_MONITOR_CNFG - Sync Monitor Configuration

Address:7CH
Type: Read / Write
Default Value: X0101011

7	6	5	4	3	2	1	0
-	SYNC_MON_LIMT2	SYNC_MON_LIMT1	SYNC_MON_LIMT0	-	-	-	-

Bit	Name	Description
7	-	Reserved.
6 - 4	SYNC_MON_LIMT[2:0]	These bits set the limit for the external sync alarm. 000: ±1 UI. 001: ±2 UI. 010: ±3 UI. (default) 011: ±4 UI. 100: ±5 UI. 101: ±6 UI. 110: ±7 UI. 111: ±8 UI.
3 - 0	-	These bits must be set to ‘1011’.

SYNC_PHASE_CNFG - Sync Phase Configuration

Address:7DH
Type: Read / Write
Default Value: XXXXXX00

7	6	5	4	3	2	1	0
-	-	-	-	-	-	SYNC_PH11	SYNC_PH10

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	SYNC_PH1[1:0]	These bits set the sampling of EX_SYNC1 when EX_SYNC1 is enabled to synchronize the frame sync output signal. Nominally, the falling edge of EX_SYNC1 is aligned with the rising edge of the T0 selected input clock. 00: On target. (default) 01: 0.5 UI early. 10: 1 UI late. 11: 0.5 UI late.

8 THERMAL MANAGEMENT

The device operates over the industry temperature range -40°C ~ +85°C. To ensure the functionality and reliability of the device, the maximum junction temperature T_{jmax} should not exceed 125°C. In some applications, the device will consume more power and a thermal solution should be provided to ensure the junction temperature T_j does not exceed the T_{jmax}.

8.1 JUNCTION TEMPERATURE

Junction temperature T_j is the temperature of package typically at the geographical center of the chip where the device's electrical circuits are. It can be calculated as follows:

Equation 1: $T_j = T_A + P \ X \ \theta_{JA}$

Where:

θ_{JA} = *Junction-to-Ambient Thermal Resistance of the Package*

T_j = *Junction Temperature*

T_A = *Ambient Temperature*

P = Device Power Consumption

In order to calculate junction temperature, an appropriate θ_{JA} must be used. The θ_{JA} is shown in Table 44:

Power consumption is the core power excluding the power dissipated in the loads. Table 43 provides power consumption in special environments.

Table 43: Power Consumption and Maximum Junction Temperature

Package	Power Consumption (W)	Operating Voltage (V)	T_A (°C)	Maximum Junction Temperature (°C)
TQFP/PNG100	1.9	3.6	85	125
TQFP/EQG100	1.9	3.6	85	125

8.2 EXAMPLE OF JUNCTION TEMPERATURE CALCULATION

Assume:

T_A = 85°C

θ_{JA} = 18.9°C/W (TQFP/EQG100 Soldered & when airflow rate is 0 m/s)

P = 1.9W

The junction temperature T_j can be calculated as follows:

$T_j = T_A + P \ X \ \theta_{JA} = 85°C + 1.9W \ X \ 18.9°C/W = 120.9°C$

The junction temperature of 120.9°C is below the maximum junction temperature of 125°C so no extra heat enhancement is required.

In some operation environments, the calculated junction temperature might exceed the maximum junction temperature of 125°C and an external thermal solution such as a heatsink is required.

8.3 HEATSINK EVALUATION

A heatsink is expanding the surface area of the device to which it is attached. θ_{JA} is now a combination of device case and heat-sink thermal resistance, as the heat flowing from the die junction to ambient goes through the package and the heatsink. θ_{JA} can be calculated as follows:

Equation 2: $\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$

Where:

θ_{JC} = *Junction-to-Case Thermal Resistance*

θ_{CH} = *Case-to-Heatsink Thermal Resistance*

θ_{HA} = *Heatsink-to-Ambient Thermal Resistance*

$\theta_{CH} + \theta_{HA}$ determines which heatsink and heatsink attachment can be selected to ensure the junction temperature does not exceed the maximum junction temperature. According to Equation 1 and 2,

$\theta_{CH} + \theta_{HA}$ can be calculated as follows:

Equation 3: $\theta_{CH} + \theta_{HA} = (T_j - T_A) / P - \theta_{JC}$

Assume:

T_j = 125°C (T_{jmax})

T_A = 85°C

P = 1.9W

θ_{JC} = 16.1°C/W (TQFP/EQG100)

$\theta_{CH} + \theta_{HA}$ can be calculated as follows:

$\theta_{CH} + \theta_{HA} = (125°C - 85°C) / 1.9W - 16.1°C/W = 5.0°C/W$

That is, if a heatsink and heatsink attachment whose $\theta_{CH} + \theta_{HA}$ is below or equal to 5.0°C/W is used in such operation environment, the junction temperature will not exceed the maximum junction temperature.

Table 44: Thermal Data

Package	Pin Count	Thermal Pad	θ_{JC} (°C/W)	θ_{JB} (°C/W)	θ_{JA} (°C/W) Air Flow in m/s					
					0	1	2	3	4	5
TQFP/PNG100	100	No	11.0	34.2	39.3	36.2	34.3	33.5	32.9	32.6
TQFP/EQG100	100	Yes/Exposed	16.1	34.2	35.8	31.1	29.5	28.6	27.9	27.4
TQFP/EQG100	100	Yes/Soldered*	16.1	1.3	18.9	14.6	13.5	12.9	12.6	12.4

*note: Simulated with 3 x 3 array of thermal vias.

8.4 TQFP EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 27. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

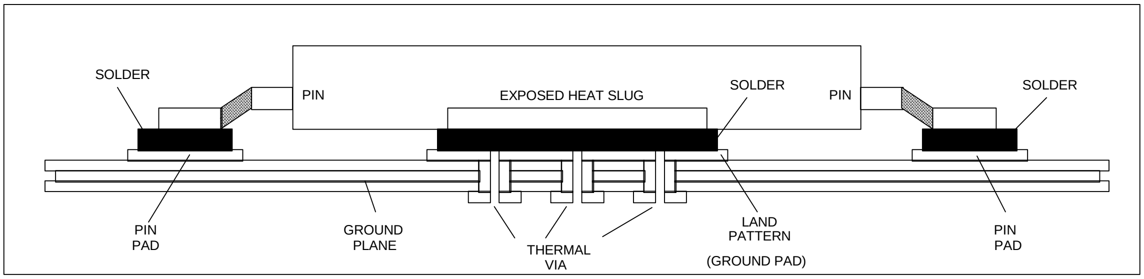


Figure 27. Assembly for Expose Pad thermal Release Path (Side View)

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as ‘heat pipes’. The number of vias (i.e. ‘heat pipes’) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1 oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

9 ELECTRICAL SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATING

Table 45: Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage VDD	-0.5	3.6	V
V_{IN}	Input Voltage (non-supply pins)		5.5	V
V_{OUT}	Output Voltage (non-supply pins)		5.5	V
T_A	Ambient Operating Temperature Range	-40	+85	°C
T_{STOR}	Storage Temperature	-50	+150	°C

9.2 RECOMMENDED OPERATION CONDITIONS

Table 46: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power Supply (DC voltage) VDD	3.0	3.3	3.6	V	
T_A	Ambient Temperature Range	-40		+85	°C	
I_{DD}	Supply Current		455	528	mA	Exclude the loading current and power
P_{TOT}	Total Power Dissipation		1.5	1.9	W	

9.3 I/O SPECIFICATIONS

9.3.1 AMI INPUT / OUTPUT PORT

9.3.1.1 Structure

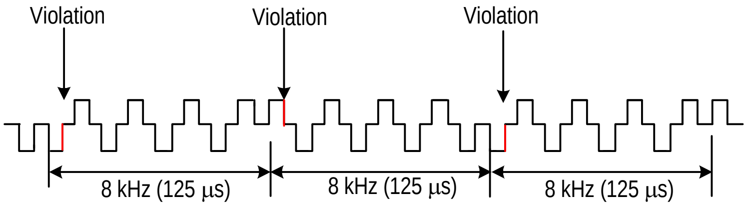


Figure 28. 64 kHz + 8 kHz Signal Structure

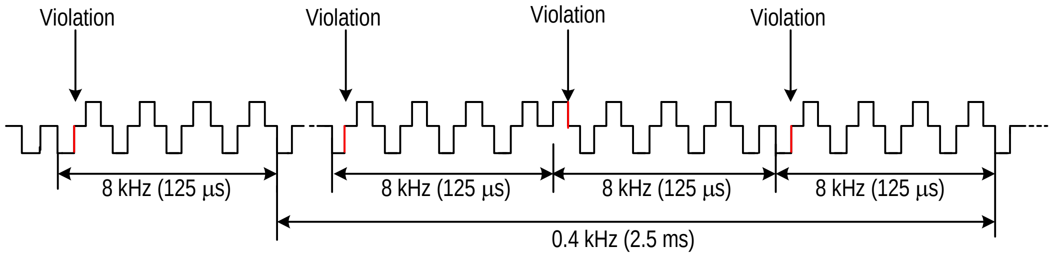
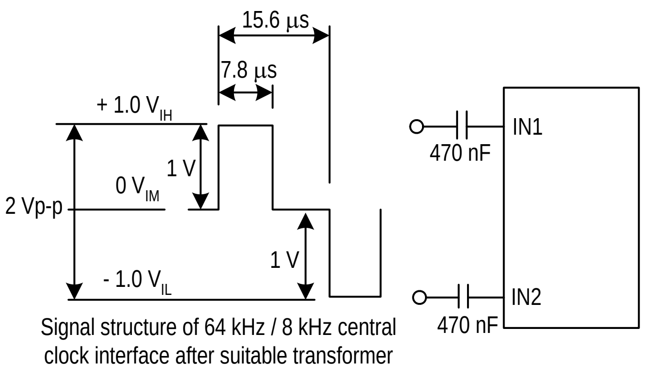


Figure 29. 64 kHz + 8 kHz + 0.4 kHz Signal Structure

9.3.1.2 I/O Level



Signal structure of 64 kHz / 8 kHz central clock interface after suitable transformer

Figure 30. 64 kHz + 8 kHz / 64 kHz + 8 kHz + 0.4 kHz Signal Input Level

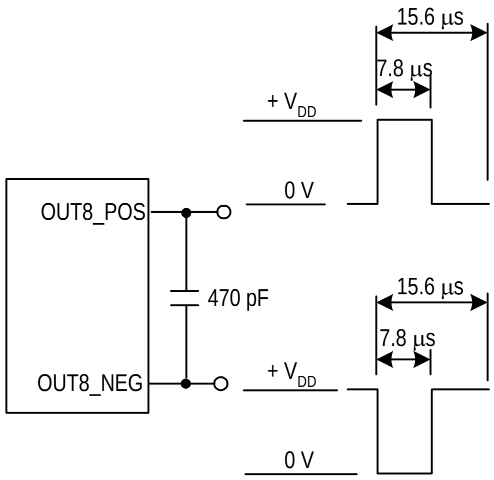
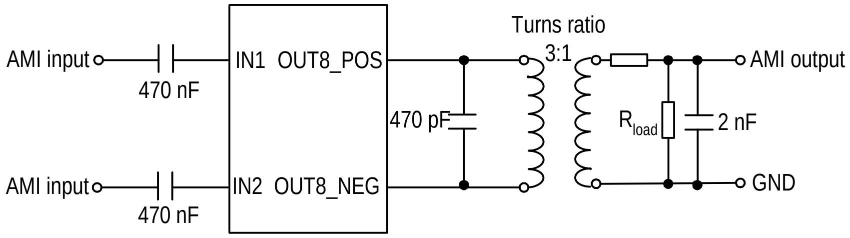


Figure 31. 64 kHz + 8 kHz / 64 kHz + 8 kHz + 0.4 kHz Signal Output Level



For a transformer with a turns ratio of 1:1, a 3:1 ratio potential divider R_{load} must be used to achieve the required 1 V pk-pk voltage level for the positive and negative pulses.

Figure 32. AMI Input / Output Port Line Termination (Recommended)

Table 47: AMI Input / Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
t_{PW}	Input Pulse Width	1.56	7.8	14.04	µS
$t_{R/F}$	Input Pulse Rise/Fall Time			5	µS
V_{IH}	Input Voltage High	2.13		V_{DD} + 0.3	V
V_{IM}	Input Voltage Middle	1.5	1.65	1.8	V
V_{IL}	Input Voltage Low	0		1.4	V
I_{OUT}	Output Current Drive			20	mA
V_{OH}	Output Voltage High, Output Current = 20 mA	V_{DD} - 0.16			V
V_{OL}	Output Voltage Low, Output Current = 20 mA			0.16	V
R_{TEST}	Nominal Test Load Impedance		110		Ω
V_{MARK}	‘Mark’ Amplitude after Transformer	0.9	1.0	1.1	V
V_{SPACE}	“Space” Amplitude after Transformer	-0.1	0	0.1	V

9.3.1.3 Over-Voltage Protection

The device may require over-voltage protection on AMI input ports according to ITU Recommendation K.41.

9.3.2 CMOS INPUT / OUTPUT PORT

From Table 48 to Table 51, V_{DD} is 3.3 V.

Table 48: CMOS Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	$0.7V_{DD}$			V	
V_{IL}	Input Voltage Low			$0.2V_{DD}$	V	
I_{IN}	Input Current			10	µA	
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 49: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	$0.7V_{DD}$			V	
V_{IL}	Input Voltage Low			$0.2V_{DD}$	V	
P_U	Pull-Up Resistor	10		80	KΩ	
I_{IN}	Input Current			250	µA	
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 50: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	$0.7V_{DD}$			V	
V_{IL}	Input Voltage Low			$0.2V_{DD}$	V	
P_D	Pull-Down Resistor	10		80	KΩ	other CMOS input port with internal pull-down resistor
		5		40		$\overline{\text{TRST}}$ and TCK pin
		100		300		A[6:0], AD[7:0] pins
I_{IN}	Input Current			350	µA	other CMOS input port with internal pull-down resistor
				700		$\overline{\text{TRST}}$ and TCK pin
				40		A[6:0], AD[7:0] pins
V_{IN}	Input Voltage	-0.5		5.5	V	

Table 51: CMOS Output Port Electrical Characteristics

Application Pin	Parameter	Description	Min	Typ	Max	Unit	Test Condition
Output Clock	V_{OH}	Output Voltage High	2.4		V_{DD}	V	I_{OH} = 8 mA
	V_{OL}	Output Voltage Low	0		0.4	V	I_{OL} = 8 mA
	t_R	Rise time		3	4	ns	15 pF
	t_F	Fall time		3	4	ns	15 pF
Other Output	V_{OH}	Output Voltage High	2.5		V_{DD}	V	I_{OH} = 4 mA
	V_{OL}	Output Voltage Low	0		0.4	V	I_{OL}= 4 mA
	t_R	Rise Time			10	ns	50 pF
	t_F	Fall Time			10	ns	50 pF

9.3.3 PECL / LVDS INPUT / OUTPUT PORT

9.3.3.1 PECL Input / Output Port

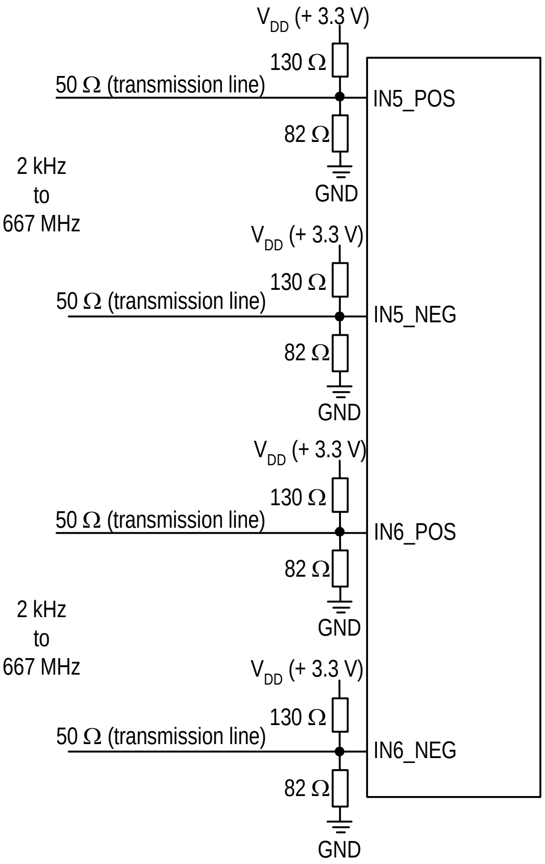


Figure 33. Recommended PECL Input Port Line Termination

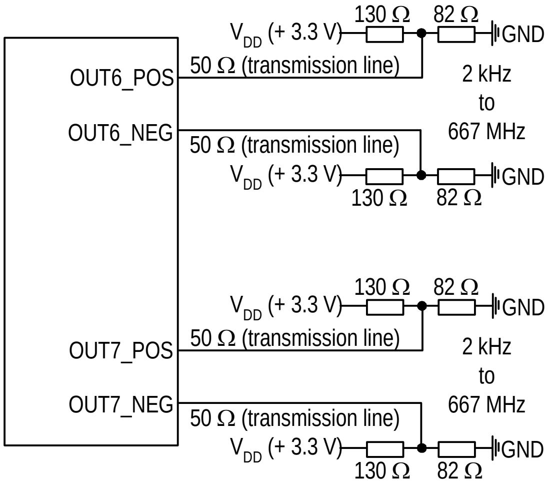


Figure 34. Recommended PECL Output Port Line Termination

Table 52: PECL Input / Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IL}	Input Low Voltage, Differential Inputs [1]	V_{DD} - 2.5		V_{DD} - 0.5	V	
V_{IH}	Input High Voltage, Differential Inputs [1]	V_{DD} - 2.4		V_{DD} - 0.4	V	
V_{ID}	Input Differential Voltage	0.1		1.4	V	
V_{IL_S}	Input Low Voltage, Single-ended Input [2]	V_{DD} - 2.4		V_{DD} - 1.5	V	
V_{IH_S}	Input High Voltage, Single-ended Input [2]	V_{DD} - 1.3		V_{DD} - 0.5	V	
I_{IH}	Input High Current, Input Differential Voltage V_{ID} = 1.4 V	-10		10	µA	
I_{IL}	Input Low Current, Input Differential Voltage V_{ID} = 1.4 V	-10		10	µA	
V_{OL}	Output Voltage Low [3]	V_{DD} - 2.1		V_{DD} - 1.62	V	
V_{OH}	Output Voltage High [3]	V_{DD} - 1.25		V_{DD} - 0.88	V	
V_{OD}	Output Differential Voltage[3]	580		900	mV	
t_{RISE}	Output Rise time (20% to 80%)	200		300	pS	
t_{FALL}	Output Fall time (20% to 80%)	200		300	pS	
t_{SKEW}	Output Differential Skew			50	pS	

Note:

1. Assuming a differential input voltage of at least 100 mV.
2. Unused differential input terminated to V_{DD}-1.4 V.
3. With 50 Ω load on each pin to V_{DD}-2 V, i.e. 82 to GND and 130 to V_{DD}.

9.3.3.2 LVDS Input / Output Port

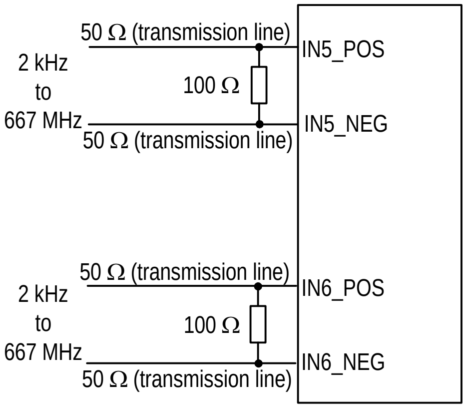


Figure 35. Recommended LVDS Input Port Line Termination

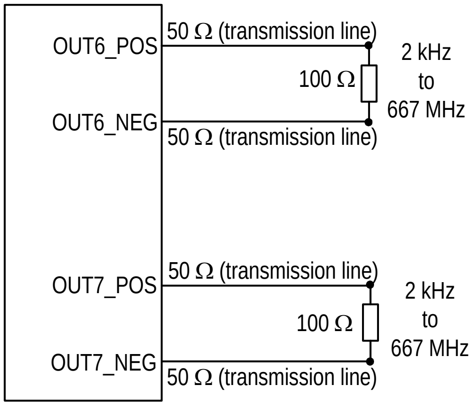


Figure 36. Recommended LVDS Output Port Line Termination

Table 53: LVDS Input / Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{CM}	Input Common-mode Voltage Range	0	1200	2400	mV	
V_{DIFF}	Input Peak Differential Voltage	100		900	mV	
V_{IDTH}	Input Differential Threshold	-100		100	mV	
R_{TERM}	External Differential Termination Impedance	95	100	105	Ω	
V_{OH}	Output Voltage High	1350		1475	mV	R_{LOAD} = 100 Ω ± 1%
V_{OL}	Output Voltage Low	925		1100	mV	R_{LOAD} = 100 Ω ± 1%
V_{OD}	Differential Output Voltage	250		400	mV	R_{LOAD} = 100 Ω ± 1%
V_{OS}	Output Offset Voltage	1125		1275	mV	R_{LOAD} = 100 Ω ± 1%
R_O	Differential Output Impedance	80	100	120	Ω	V_{CM} = 1.0 V or 1.4 V
ΔR_O	R_O Mismatch between A and B			20	%	V_{CM} = 1.0 V or 1.4 V
ΔV_{OD}	Change in V_{OD} between Logic 0 and Logic 1			25	mV	R_{LOAD} = 100 Ω ± 1%
ΔV_{OS}	Change in V_{OS} between Logic 0 and Logic 1			25	mV	R_{LOAD} = 100 Ω ± 1%
I_{SA}, I_{SB}	Output Current			24	mA	Driver shorted to GND
I_{SAB}	Output Current			12	mA	Driver shorted together
t_{RISE}	Output Rise time (20% to 80%)	200		300	pS	R_{LOAD} = 100 Ω ± 1%
t_{FALL}	Output Fall time (20% to 80%)	200		300	pS	R_{LOAD} = 100 Ω ± 1%
t_{SKEW}	Output Differential Skew			50	pS	R_{LOAD} = 100 Ω ± 1%

9.3.3.3 Single-Ended Input for Differential Input

This is a recommended and tested interface circuit to drive differential input with a single-ended signal.

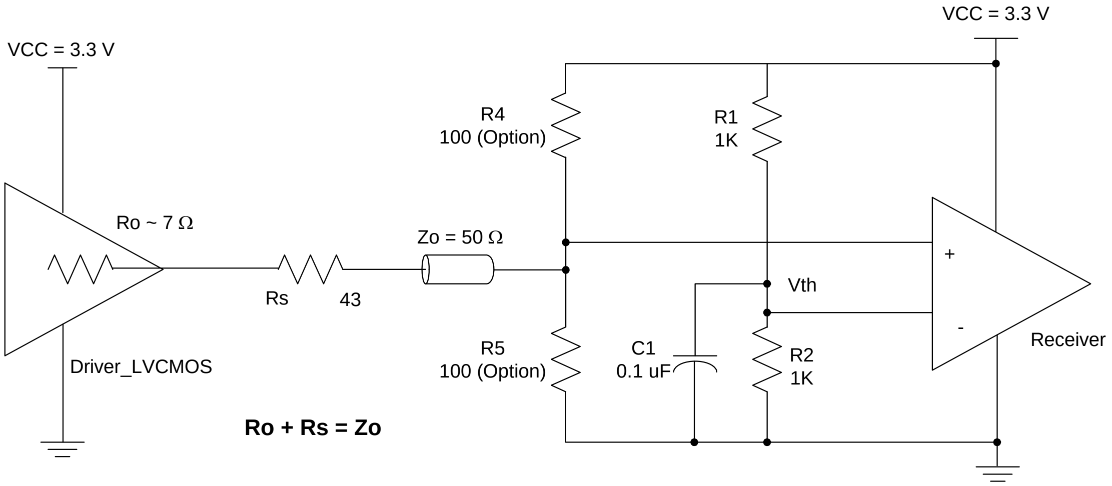


Figure 37. Example of Single-Ended Signal to Drive Differential Input

Vth = VCC*[R2/(R1+R2)]

For the example in Figure 37, R1 = R2, so Vth = VCC/2 =1.65 V

The suggested single-ended signal input:

V_{IHmax} = VCC

V_{ILmin} = 0 V

V_{swing} = 0.6 V ~ VCC

DC offset (Swing Center) = Vth/2 +/- V_{swing}*10%

9.4 JITTER & WANDER PERFORMANCE

Table 54: Output Clock Jitter Generation

Test Definition [1]	Peak to Peak Typ	RMS Typ	Note	Test Filter
N x 2.048MHz without APLL	<2 ns	<200 ps		20 Hz - 100 kHz
N x 2.048MHz with T0/T4 APLL	<1 ns	<100 ps	See Table 55: Output Clock Phase Noise for details	20 Hz - 100 kHz
N x 1.544 MHz without APLL	<2 ns	<200 ps		10 Hz - 40 kHz
N x 1.544 MHz with T0/T4 APLL	<1 ns	<100 ps	See Table 55: Output Clock Phase Noise for details	10 Hz - 40 kHz
44.736 MHz with T0/T4 APLL	<1 ns	<100 ps	See Table 55: Output Clock Phase Noise for details	100 Hz - 800 kHz
44.736 MHz without APLL	<2 ns	<200 ps		100 Hz - 800 kHz
34.368 MHz with T0/T4 APLL	<1 ns	<100 ps	See Table 55: Output Clock Phase Noise for details	10 Hz - 400 kHz
34.368 MHz without APLL	<2 ns	<200 ps		10 Hz - 400 kHz
OC-3 (Chip T0 DPLL + T0/T4 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz output	0.004 UI p-p	0.001 UI RMS	GR-253, G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
	0.004 UI p-p	0.001 UI RMS	G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-6430 ps)	500 Hz - 1.3 MHz
	0.001 UI p-p	0.001 UI RMS	G.813 Option 1 limit 0.1 UI p-p (1 UI-6430 ps)	65 kHz - 1.3 MHz
OC-12 (Chip T0 DPLL + T0/T4 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz output + Intel GD16523 + Optical transceiver)	0.018 UI p-p	0.007 UI RMS	GR-253, G.813 Option 2 limit 0.1 UI p-p (1 UI-1608 ps)	12 kHz - 5 MHz
	0.028 UI p-p	0.009 UI RMS	G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-1608 ps)	1 kHz - 5 MHz
	0.002 UI p-p	0.001 UI RMS	G.813 Option 1, G.812 limit 0.1 UI p-p (1 UI-1608 ps)	250 kHz - 5 MHz
STM-16 (Chip T0 DPLL + T0/T4 APLL) 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz output + Intel GD16523 + Optical transceiver)	0.162 UI p-p	0.03 UI RMS	G.813 Option 1, G.812 limit 0.5 UI p-p (1 UI-402 ps)	5 kHz - 20 MHz
	0.01 UI p-p	0.009 UI RMS	G.813 Option 1, G.812 limit 0.1 UI p-p (1 UI-402 ps)	1 MHz - 20 MHz

Note:
1. CMAC E2747 TCXO is used.

Table 55: Output Clock Phase Noise

Output Clock [1]	@100Hz Offset Typ	@1kHz Offset Typ	@10kHz Offset Typ	@100kHz Offset Typ	@1MHz Offset Typ	@5MHz Offset Typ	Unit
622.08 MHz (T0 DPLL + T0/T4 APLL)	-70	-86	-95	-100	-107	-128	dBC/Hz
155.52 MHz (T0 DPLL + T0/T4 APLL)	-82	-98	-107	-112	-119	-140	dBC/Hz
38.88 MHz (T0 DPLL + T0/T4 APLL)	-94	-110	-118	-124	-131	-143	dBC/Hz
16E1 (T0/T4 APLL)	-94	-110	-118	-125	-131	-142	dBC/Hz
16T1 (T0/T4 APLL)	-95	-112	-120	-127	-132	-143	dBC/Hz
E3 (T0/T4 APLL)	-93	-109	-116	-124	-131	-138	dBC/Hz
T3 (T0/T4 APLL)	-92	-108	-116	-122	-126	-141	dBC/Hz
77.76 MHz (T4 DPLL)	-92	-108	-110	-117	-116	-121	dBC/Hz

Note:
[1] CMAC E2747 TCXO is used.

Table 56: Input Jitter Tolerance (155.52 MHz)

Jitter Frequency	Jitter Tolerance Amplitude (UI p-p)
12 μHz	> 2800
178 μHz	> 2800
1.6 mHz	> 311
15.6 mHz	> 311
0.125 Hz	> 39
19.3 Hz	> 39
500 Hz	> 1.5
6.5 kHz	> 1.5
65 kHz	> 0.15
1.3 MHz	> 0.15

Table 57: Input Jitter Tolerance (1.544 MHz)

Jitter Frequency	Jitter Tolerance Amplitude (UI p-p)
1 Hz	150
5 Hz	140
20 Hz	130
300 Hz	38
400 Hz	25
700 Hz	15
2400 Hz	5
10 kHz	1.2
40 kHz	0.5

Table 58: Input Jitter Tolerance (2.048 MHz)

Jitter Frequency	Jitter Tolerance Amplitude (UI p-p)
1 Hz	150
5 Hz	140
20 Hz	130
300 Hz	40
400 Hz	33
700 Hz	18
2400 Hz	5.5
10 kHz	1.3
50 kHz	0.4
100 kHz	0.4

Table 59: Input Jitter Tolerance (8 kHz)

Jitter Frequency	Jitter Tolerance Amplitude (UI p-p)
1 Hz	0.8
5 Hz	0.7
20 Hz	0.6
300 Hz	0.16
400 Hz	0.14
700 Hz	0.07
2400 Hz	0.02
3600 Hz	0.01

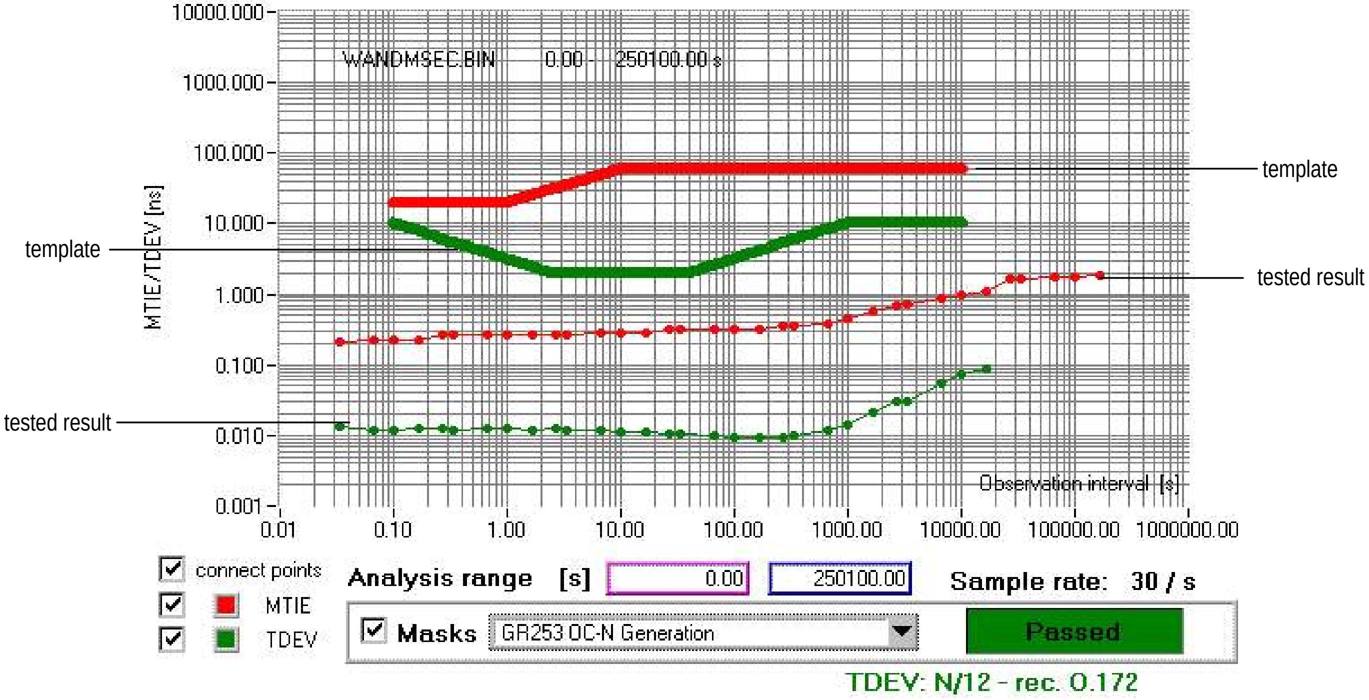
Table 60: T0 DPLL Jitter Transfer & Damping Factor

3 dB Bandwidth	Programmable Damping Factor
0.5 mHz	1.2, 2.5, 5, 10, 20
1 mHz	1.2, 2.5, 5, 10, 20
2 mHz	1.2, 2.5, 5, 10, 20
4 mHz	1.2, 2.5, 5, 10, 20
8 mHz	1.2, 2.5, 5, 10, 20
15 mHz	1.2, 2.5, 5, 10, 20
30 mHz	1.2, 2.5, 5, 10, 20
60 mHz	1.2, 2.5, 5, 10, 20
0.1 Hz	1.2, 2.5, 5, 10, 20
0.3 Hz	1.2, 2.5, 5, 10, 20
0.6 Hz	1.2, 2.5, 5, 10, 20
1.2 Hz	1.2, 2.5, 5, 10, 20
2.5 Hz	1.2, 2.5, 5, 10, 20
4 Hz	1.2, 2.5, 5, 10, 20
8 Hz	1.2, 2.5, 5, 10, 20
18 Hz	1.2, 2.5, 5, 10, 20
35 Hz	1.2, 2.5, 5, 10, 20
70 Hz	1.2, 2.5, 5, 10, 20
560 Hz	1.2, 2.5, 5, 10, 20

Table 61: T4 DPLL Jitter Transfer & Damping Factor

3 dB Bandwidth	Programmable Damping Factor
18 Hz	1.2, 2.5, 5, 10, 20
35 Hz	1.2, 2.5, 5, 10, 20
70 Hz	1.2, 2.5, 5, 10, 20
560 Hz	1.2, 2.5, 5, 10, 20

9.5 OUTPUT WANDER GENERATION



☑ connect points

☑ 🟥 MTIE

☑ 🟩 TDEV

Analysis range [s] 0.00 250100.00

Sample rate: 30 / s

☑ Masks GR253 OC-N Generation

TDEV: N/12 - rec. 0.172

Figure 38. Output Wander Generation

9.6 INPUT / OUTPUT CLOCK TIMING

The inputs and outputs are aligned ideally. But due to the circuit delays, there is delay between the inputs and outputs.

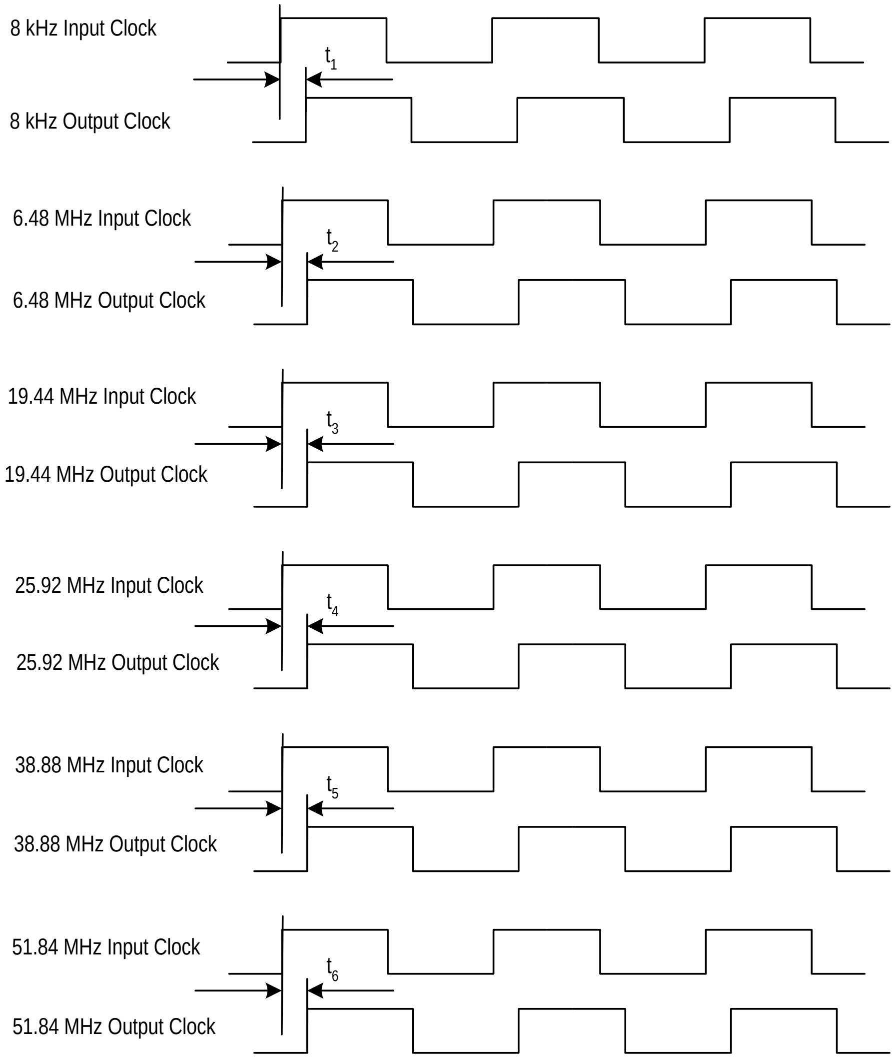


Figure 39. Input / Output Clock Timing

Table 62: Input/Output Clock Timing [3]

Symbol	Typical Delay [1] (ns)	Peak to Peak Delay Variation [2] (ns)
t_1	4	1.6
t_2	1	1.6
t_3	1	1.6
t_4	2	1.6
t_5	1.4	1.6
t_6	3	1.6

Note:
1. Typical delay provided as reference only.
2. 'Peak to Peak Delay Variation' is the delay variation that is guaranteed not to be exceeded for IN11 in Master/Slave operation.
3. Tested when IN11 is selected.

9.7 OUTPUT CLOCK TIMING

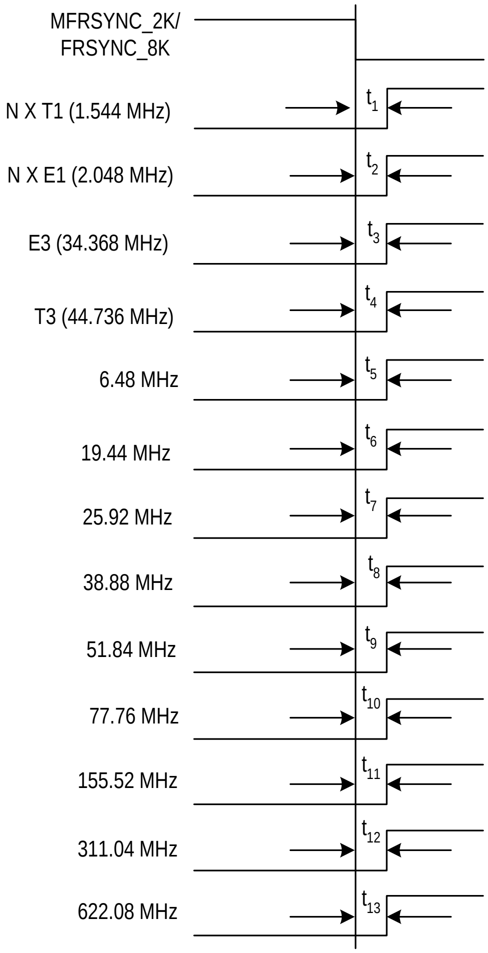


Table 63: Output Clock Timing

Symbol	Typical Delay (ns)	Peak to Peak Delay Variation (ns)
t_1	0	2
t_2	0	2
t_3	0	2
t_4	0	2
t_5	0	2
t_6	0	2
t_7	0	2
t_8	0	2
t_9	0	2
t_{10}	0	2
t_{11}	0	1.5
t_{12}	0	1.5 (not recommended to use)
t_{13}	0	1.5 (not recommended to use)

Glossary

3G	---	Third Generation
ADSL	---	Asymmetric Digital Subscriber Line
APLL	---	Analog Phase Locked Loop
ATM	---	Asynchronous Transfer Mode
BITS	---	Building Integrated Timing Supply
CMOS	---	Complementary Metal-Oxide Semiconductor
DCO	---	Digital Controlled Oscillator
DPLL	---	Digital Phase Locked Loop
DSL	---	Digital Subscriber Line
DSLAM	---	Digital Subscriber Line Access MUX
DWDM	---	Dense Wavelength Division Multiplexing
EPROM	---	Erasable Programmable Read Only Memory
GPS	---	Global Positioning System
GSM	---	Global System for Mobile Communications
IIR	---	Infinite Impulse Response
IP	---	Internet Protocol
ISDN	---	Integrated Services Digital Network
JTAG	---	Joint Test Action Group
LPF	---	Low Pass Filter
LVDS	---	Low Voltage Differential Signal
MTIE	---	Maximum Time Interval Error
MUX	---	Multiplexer
OBSAI	---	Open Base Station Architecture Initiative
OC-n	---	Optical Carried rate, n = 1, 3, 12, 48, 192, 768; 51 Mbit/s, 155 Mbit/s, 622 Mbit/s, 2.5 Gbit/s, 10 Gbit/s, 40 Gbit/s.
PBO	---	Phase Build-Out
PDH	---	Plesiochronous Digital Hierarchy

PECL	---	Positive Emitter Coupled Logic
PFD	---	Phase & Frequency Detector
PLL	---	Phase Locked Loop
RMS	---	Root Mean Square
PRS	---	Primary Reference Source
SDH	---	Synchronous Digital Hierarchy
SEC	---	SDH / SONET Equipment Clock
SMC	---	SONET Minimum Clock
SONET	---	Synchronous Optical Network
SSU	---	Synchronization Supply Unit
STM	---	Synchronous Transfer Mode
TCM-ISDN	---	Time Compression Multiplexing Integrated Services Digital Network
TDEV	---	Time Deviation
UI	---	Unit Interval
WLL	---	Wireless Local Loop

Index

PACKAGE DIMENSIONS

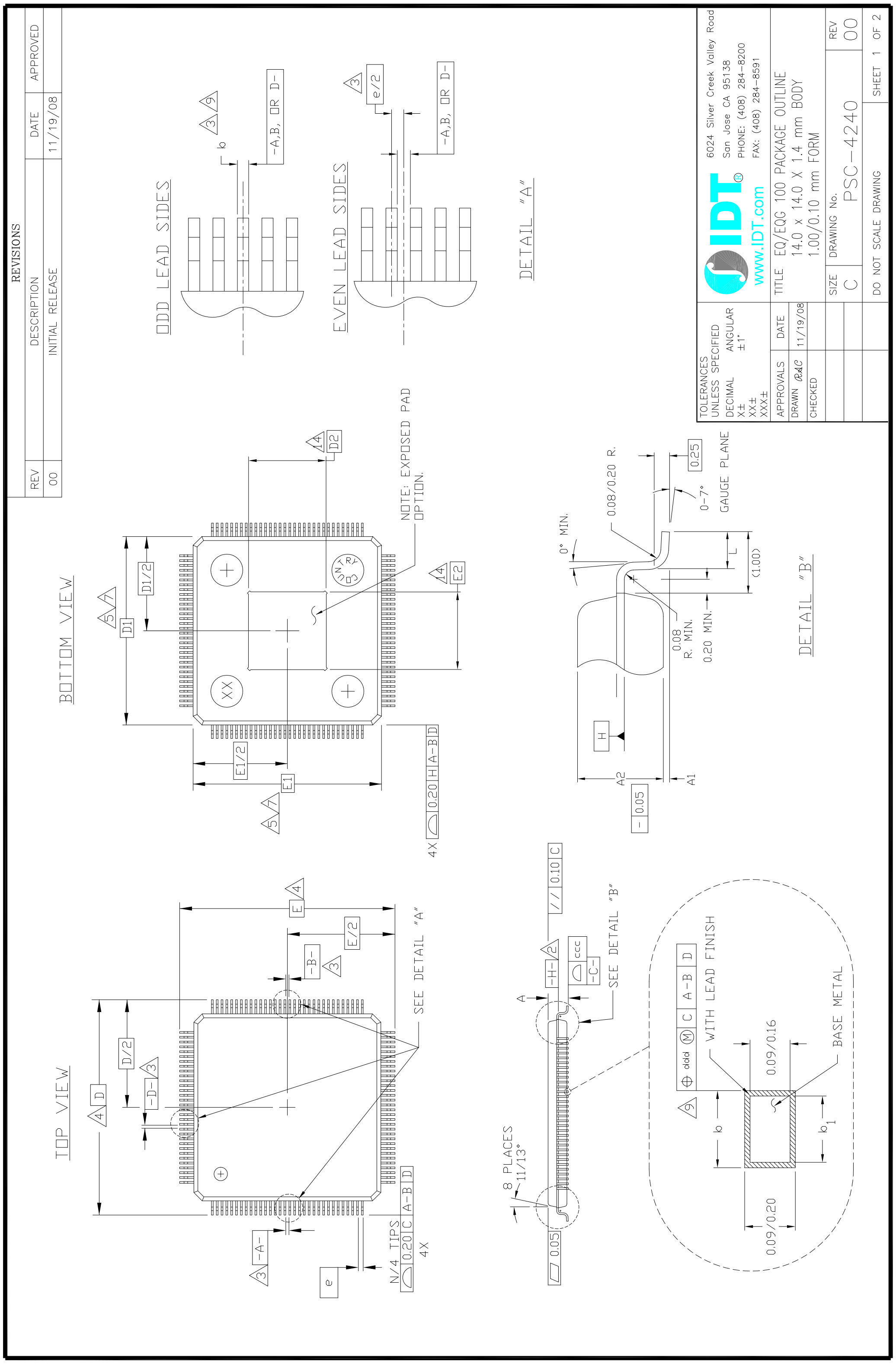
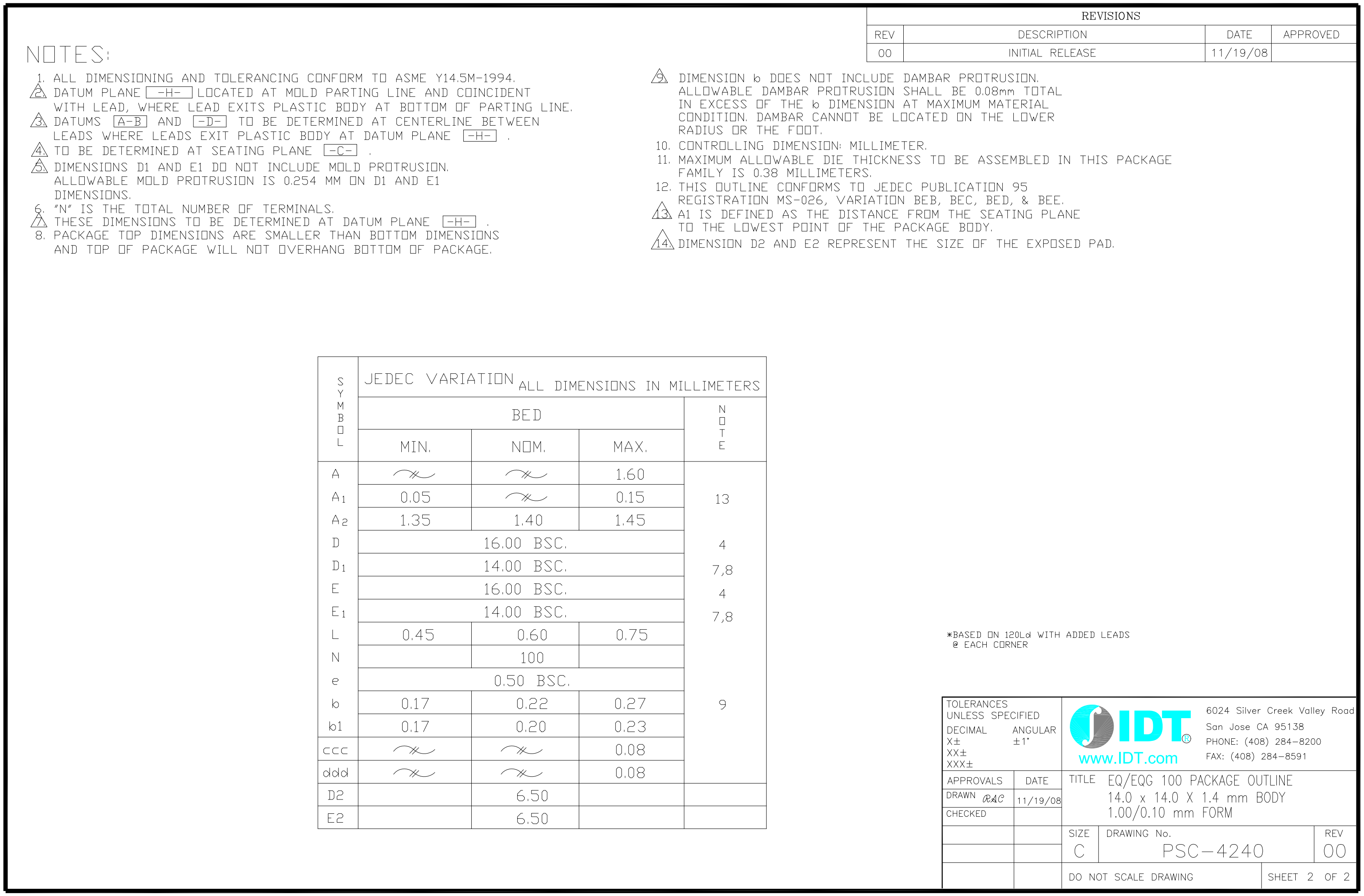


Figure 40. 100-Pin EQG Package Dimensions (a) (in Millimeters)



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/19/08	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
△2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
△3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
△4. TO BE DETERMINED AT SEATING PLANE -C- .
△5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
△7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
△9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION BEB, BEC, BED, & BEE.
△13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
△14. DIMENSION D2 AND E2 REPRESENT THE SIZE OF THE EXPOSED PAD.

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS

SYMBOL	BED			NOTE
	MIN.	NOM.	MAX.	
A	⁓	⁓	1.60	
A_1	0.05	⁓	0.15	13
A_2	1.35	1.40	1.45	
D		16.00 BSC.		4
D_1		14.00 BSC.		7,8
E		16.00 BSC.		4
E_1		14.00 BSC.		7,8
L	0.45	0.60	0.75	
N		100		
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	⁓	⁓	0.08	
ddd	⁓	⁓	0.08	
D2		6.50		
E2		6.50		

*BASED ON 120Ld WITH ADDED LEADS
@ EACH CORNER

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± ±1°
XX±
XXX±

IDT®
www.IDT.com
6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

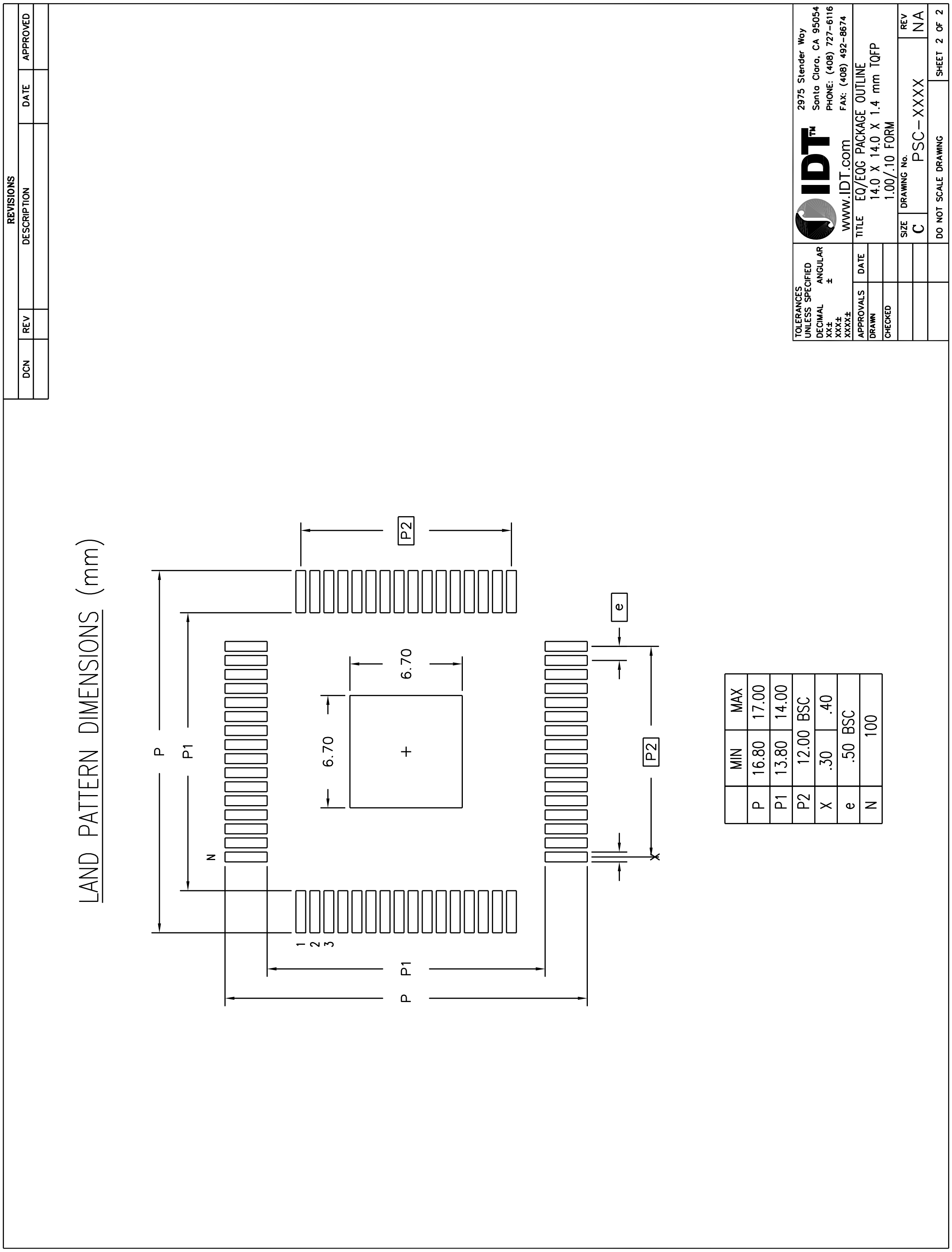
APPROVALS		DATE
DRAWN	RAC	11/19/08
CHECKED		

TITLE EQ/EQG 100 PACKAGE OUTLINE
14.0 x 14.0 X 1.4 mm BODY
1.00/0.10 mm FORM

SIZE C
DRAWING No. PSC-4240
REV 00

DO NOT SCALE DRAWING
SHEET 2 OF 2

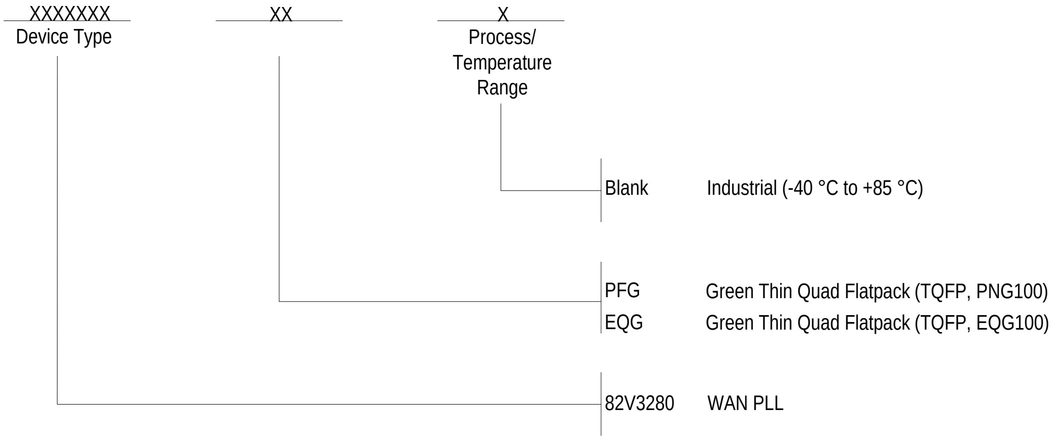
Figure 41. 100-Pin EQG Package Dimensions (b) (in Millimeters)



	MIN	MAX
P	16.80	17.00
P1	13.80	14.00
P2	12.00 BSC	
X	.30	.40
e	.50 BSC	
N	100	

Figure 42. EQG100 Recommended Land Pattern with Exposed Pad (in Millimeters)

ORDERING INFORMATION



DATASHEET DOCUMENT HISTORY

09/28/2005 pgs. 152.

06/19/2006 pgs. 46

03/14/2007 pgs. 149

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2025 Renesas Electronics Corporation. All rights reserved.