ICS932S801

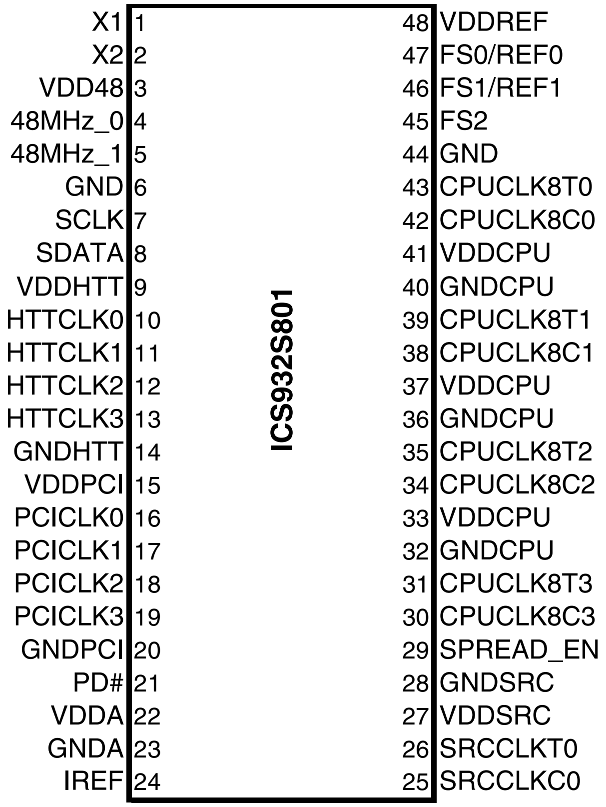
K8 Clock Chip for Serverworks GC-HT 2-Way Servers

Recommended Application:
Serverworks GC-HT systems using AMD K8 processors

Output Features:
- 4 - Pairs of AMD K8 clocks
- 1 - Pair of SRC/PCI Express* clock
- 2 - 14.318 MHz REF clocks
- 2 - USB_48MHz clocks
- 4 - HyperTransport 66 MHz clocks
- 4 - PCI 33 MHz clocks

Features:
- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- M/N programming via SMBus

Pin Configuration



48-SSOP, TSSOP

Power Groups

Pin Number		Description
VDD	GND	
3	6	48MHz
9	14	66MHz HTT Clocks
15	20	33 MHz PCI Clocks
22	23	IREF, Analog Core
27	28	SRC PLL, SRCCLK
33,37,41	32,36,40	K8 CPU Clocks, CPU PLL
48	44	REF Clocks, Xtal Oscillator

Functionality

FS2	FS1	FS0	CPU MHz	HTT MHz	PCI MHz
0	0	0	Hi-Z	Hi-Z	Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	73.12	36.56
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	0	166.67	66.66	33.33
1	1	1	200.00	66.66	33.33

*Other names and brands may be claimed as the property of others.

Pin Descriptions

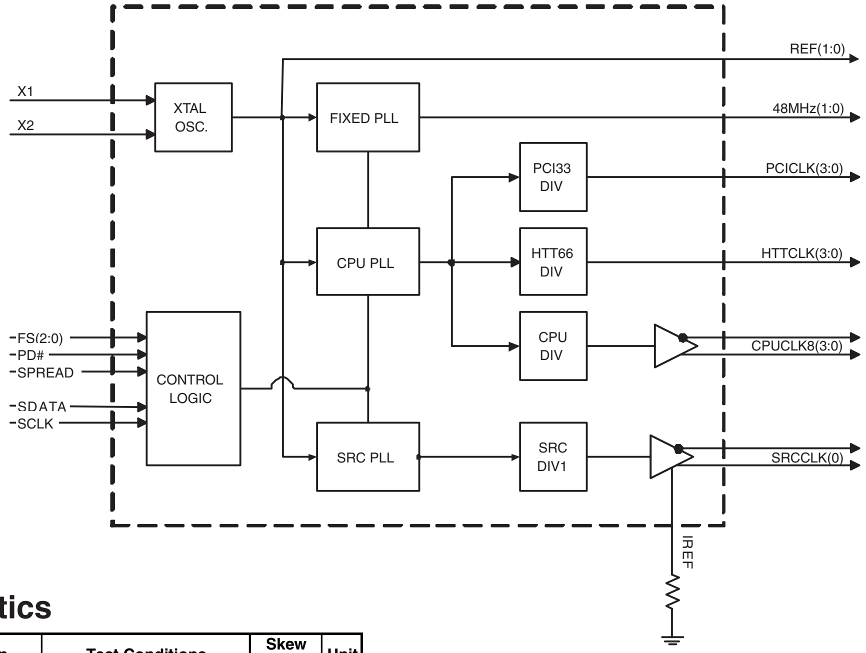
PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	X1	IN	Crystal input, Nominally 14.318MHz.
2	X2	OUT	Crystal output, Nominally 14.318MHz
3	VDD48	PWR	Power pin for the 48MHz output.3.3V
4	48MHz_0	OUT	48MHz clock output.
5	48MHz_1	OUT	48MHz clock output.
6	GND	PWR	Ground pin.
7	SCLK	I/O	Clock pin of SMBus circuitry, 5V tolerant.
8	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
9	VDDHTT	PWR	Supply for HTT clocks, nominal 3.3V.
10	HTTCLK0	OUT	3.3V Hyper Transport output
11	HTTCLK1	OUT	3.3V Hyper Transport output
12	HTTCLK2	OUT	3.3V Hyper Transport output
13	HTTCLK3	OUT	3.3V Hyper Transport output
14	GNDHTT	PWR	Ground pin for the HTT outputs
15	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
16	PCICLK0	OUT	PCI clock output.
17	PCICLK1	OUT	PCI clock output.
18	PCICLK2	OUT	PCI clock output.
19	PCICLK3	OUT	PCI clock output.
20	GNDPCI	PWR	Ground pin for the PCI outputs
21	PD#	IN	Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped.
22	VDDA	PWR	3.3V power for the PLL core.
23	GNDA	OUT	Ground pin for the PLL core.
24	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
25	SRCCLKC0	OUT	Complement clock of differential SRC clock pair.
26	SRCCLKT0	OUT	True clock of differential SRC clock pair.
27	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
28	GNDSRC	PWR	Ground pin for the SRC outputs
29	SPREAD_EN	IN	Asynchronous, active high input to enable spread spectrum functionality.
30	CPUCLK8C3	OUT	Complementary clock of differential 3.3V push-pull K8 pair.
31	CPUCLK8T3	OUT	True clock of differential 3.3V push-pull K8 pair.
32	GNDCPU	PWR	Ground pin for the CPU outputs
33	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
34	CPUCLK8C2	OUT	Complementary clock of differential 3.3V push-pull K8 pair.
35	CPUCLK8T2	OUT	True clock of differential 3.3V push-pull K8 pair.
36	GNDCPU	PWR	Ground pin for the CPU outputs
37	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
38	CPUCLK8C1	OUT	Complementary clock of differential 3.3V push-pull K8 pair.
39	CPUCLK8T1	OUT	True clock of differential 3.3V push-pull K8 pair.
40	GNDCPU	PWR	Ground pin for the CPU outputs
41	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
42	CPUCLK8C0	OUT	Complementary clock of differential 3.3V push-pull K8 pair.
43	CPUCLK8T0	OUT	True clock of differential 3.3V push-pull K8 pair.
44	GND	PWR	Ground pin.
45	FS2	IN	Frequency select pin.
46	FS1/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
47	FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
48	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V

General Description

The **ICS932S801** is a main clock synthesizer chip that, when paired with ICS9DB108, provides all clocks required by Serverworks GC-HT-based servers.

An SMBus interface allows full control of the device.

Block Diagram



Skew Characteristics

	Parameter	Description	Test Conditions	Skew Window	Unit
Time Independent	Tsk_CPU_CPU	CPU to CPU Skew	Measured at crossing points of CPUCLKT rising edges	250	ps
	Tsk_CPU_PCI	CPU to PCI skew	Meastured at crossing point for CPUCLKT and 1.5V for PCI clock	2000	ps
	Tsk_PCI33-HT66	PCI33 to HT66 skew	Measured between rising edges at 1.5V	500	ps
	Tsk_CPU_HT66	CPU to HT66 skew	Meastured at crossing point for CPUCLKT and 1.5V for HT66 clock	2000	ps
Time Variant	Tsk_CPU_CPU	CPU to CPU Skew	Measured at crossing points of CPUCLKT rising edges	200	ps
	Tsk_CPU_PCI	CPU to PCI skew	Meastured at crossing point for CPUCLKT and 1.5V for PCI clock	200	ps
	Tsk_PCI33-HT66	PCI33 to HT66 skew	Measured between rising edges at 1.5V	200	ps
	Tsk_CPU_HT66	CPU to HT66 skew	Meastured at crossing point for CPUCLKT and 1.5V for HT66 clock	200	ps

Table1: SRC Frequency Selection Table

SRCFS1 B5b3	SRCFS0 B5b2	SRCCLK (MHz)
0	0	100.00
0	1	101.00
1	0	102.00
1	1	104.00

Table 2: CPU Divider Ratios

	Divider (3:2)								
Divider (1:0)	**Bit**	**00**		**01**		**10**		**11**	**MSB**
	00	0000	**2**	0100	**4**	1000	**8**	1100	**16**
	01	0001	**3**	0101	**6**	1001	**12**	1101	**24**
	10	0010	**5**	0110	**10**	1010	**20**	1110	**40**
	11	0011	**15**	0111	**30**	1011	**60**	1111	**120**
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

Table 3: HTT Divider Ratios

	Divider (3:2)								
Divider (1:0)	**Bit**	**00**		**01**		**10**		**11**	**MSB**
	00	0000	**4**	0100	**8**	1000	**16**	1100	**32**
	01	0001	**3**	0101	**6**	1001	**12**	1101	**24**
	10	0010	**5**	0110	**10**	1010	**20**	1110	**40**
	11	0011	**15**	0111	**30**	1011	**60**	1111	**120**
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

Table 4: SRC Divider Ratios

	Divider (3:2)								
Divider (1:0)	**Bit**	**00**		**01**		**10**		**11**	**MSB**
	00	0000	**2**	0100	**4**	1000	**8**	1100	**16**
	01	0001	**3**	0101	**6**	1001	**12**	1101	**24**
	10	0010	**5**	0110	**10**	1010	**20**	1110	**40**
	11	0011	**7**	0111	**14**	1011	**28**	1111	**56**
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

Absolute Maximum Ratings

Supply Voltage	3.8V
Logic Inputs	GND –0.5 V to V_{DD} +3.8 V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +150°C
ESD Protection	Input ESD protection usung human body model > 1KV

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			325	mA	
Powerdown Current	$I_{DD3.3PD}$				100	mA	
Input Frequency[3]	F_i	V_{DD} = 3.3 V		14.31818		MHz	3
Pin Inductance[1]	L_{pin}				7	nH	1
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization[1,2]	T_{STAB}	From V_{DD} Power-Up or de-assertion of PD# to 1st clock			3	ms	1,2
Modulation Frequency		Triangular Modulation	30		33	kHz	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SCLK/SDATA Clock/Data Rise Time[3]	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time[3]	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See timing diagrams for timing requirements.

[3] Input frequency should be measured at the REFOUT pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - K8 Push Pull Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =AMD64 Processor Test Load

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Rate	$\delta V/\delta t$	Measured at the AMD64 processor's test load. 0 V +/- 400 mV (differential measurement)	2		10	V/ns	1
Falling Edge Rate	$\delta V/\delta t$		2		10	V/ns	1
Differential Voltage	V_{DIFF}	Measured at the AMD64 processor's test load. (single-ended measurement)	0.4	1.25	2.3	V	1
Change in V_{DIFF_DC} Magnitude	ΔV_{DIFF}		-150		150	mV	1
Common Mode Voltage	V_{CM}		1.05	1.25	1.45	V	1
Change in Common Mode Voltage	ΔV_{CM}		-200		200	mV	1
Jitter, Cycle to cycle	$t_{jcyc\text{-}cyc}$	Measurement from differential wavefrom. Maximum difference of cycle time between 2 adjacent cycles.	0	100	200	ps	1
Jitter, Accumulated	t_{ja}	Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50 ps, Sample Duration = 10 us	-1000		1000		1,2,3
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		53	%	1
Output Impedance	R_{ON}	Average value during switching transition. Used for determining series termination value.	15	35	55	Ω	1
Group Skew	$t_{src\text{-}skew}$	Measurement from differential wavefrom			250	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All accumulated jitter specifications are guaranteed assuming that REF is at 14.31818MHz

[3] Spread Spectrum is off

Electrical Characteristics - SRC 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00 MHz nominal	9.9970	10.0000	10.0030	ns	2
		100.00 MHz spread	9.9970		10.0530	ns	2
Absolute min period	Tabsmin	@100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r			30	125	ps	1
Fall Time Variation	d-t_f			30	125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Group Skew	$t_{src\text{-}skew}$	Measurement from differential wavefrom			N/A	ps	
Jitter, Phase	$t_{jphase\text{-}pcie1}$	PCI Express Gen 1 phase jitter CPU=200MHz, Spread off		38	86	ps	1, 4
		PCI Express Gen 1 phase jitter CPU=200MHz, Spread on		52	86	ps	1, 4
Jitter, Cycle to cycle	$t_{jcyc\text{-}cyc}$	Measurement from differential wavefrom			100	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

[3] $I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[4] Per PCI SIG method for PCI Express Gen 1. Visit http://www.pcisig.com for details.

Electrical Characteristics - PCICLK 33 MHz, HTTCLK 66 MHz Clocks

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
PCI33 Clock period	T_{period}	33.33MHz output nominal	29.9910		30.0090	ns	2
		33.33MHz output spread	29.9910		30.1598	ns	2
HTT66 Clock period	T_{period}	66.67MHz output nominal	14.9955		15.0045	ns	2
		66.67MHz output spread	14.9955		15.0799	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@ MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	δV/δt	Rising edge rate	1		4	V/ns	1
Edge Rate	δV/δt	Falling edge rate	1		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Skew	t_{sk1}	V_T = 1.5 V			200	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

Electrical Characteristics - 48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8257		20.8340	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @ MIN = 1.0 V	-33			mA	1
		V_{OH}@ MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	δV/δt	Rising edge rate	1		4	V/ns	1
Edge Rate	δV/δt	Falling edge rate	1		4	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Skew	t_{sk1}	V_T = 1.5 V			50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			200	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

Electrical Characteristics - REF-14.318MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 27 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Edge Rate	$\delta V/\delta t$	Rising edge rate	1		2	V/ns	1
Edge Rate	$\delta V/\delta t$	Falling edge rate	1		2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Skew	t_{sk1}	V_T = 1.5 V			50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

General SMBus serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1*** (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Frequency Select and Spread Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Latched Input or SMBus Frequency Select	RW	Latched Inputs	SMBus	0
Bit 6	-	CPU SS_EN	Spread Enable for CPU and SRC PLLs. **Setting SPREAD_EN to '1', forces Spread ON for both PLLs.**	RW	OFF	ON	0
Bit 5	-	SRC SS_EN		RW	OFF	ON	0
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 3	-	FS3	Freq Select Bit 3	RW	See Functionality Table on Page 1		0
Bit 2	-	FS2	Freq Select Bit 2	RW			Latched
Bit 1	-	FS1	Freq Select Bit 1	RW			Latched
Bit 0	-	FS0	Freq Select Bit 0	RW			Latched

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		PCICLK3	Output Enable	RW	Disable (Low)	Enable	1
Bit 6		PCICLK2	Output Enable	RW	Disable (Low)	Enable	1
Bit 5		PCICLK1	Output Enable	RW	Disable (Low)	Enable	1
Bit 4		PCICLK0	Output Enable	RW	Disable (Low)	Enable	1
Bit 3		HTTCLK3	Output Enable	RW	Disable (Low)	Enable	1
Bit 2		HTTCLK2	Output Enable	RW	Disable (Low)	Enable	1
Bit 1		HTTCLK1	Output Enable	RW	Disable (Low)	Enable	1
Bit 0		HTTCLK0	Output Enable	RW	Disable (Low)	Enable	1

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		48MHz_1	Output Enable	RW	Disable (Low)	Enable	1
Bit 6		48MHz_0	Output Enable	RW	Disable (Low)	Enable	1
Bit 5		REF1	Output Enable	RW	Disable (Low)	Enable	1
Bit 4		REF0	Output Enable	RW	Disable (Low)	Enable	1
Bit 3		CPUCLK8(3)	Output Enable When Disabled CPUCLKT = 0 CPUCLKC = 1	RW	Disable	Enable	1
Bit 2		CPUCLK8(2)		RW	Disable	Enable	1
Bit 1		CPUCLK8(1)		RW	Disable	Enable	1
Bit 0		CPUCLK8(0)		RW	Disable	Enable	1

SMBus Table: SRCCLK(0) Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 6	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 3	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 1	-	SRCCLK0 PD	SRCCLK Power Down Drive Mode	RW	Driven	Hi-Z	0
Bit 0		SRCCLK0	Output Enable	RW	Disable (Hi-Z)	Enable	1

SMBus Table: 48MHz Drive Strength Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 6	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 3	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 1	5	48MHz_1 DS	Drive Strength Control	RW	1X	2X	0
Bit 0	4	48MHz_0 DS	Drive Strength Control	RW	1X	2X	0

SMBus Table: SRC Frequency Select Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 6	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 3	-	SRCFS1	SRC FS bit 1	RW	See Table 1: SRC Frequency Select		0
Bit 2	-	SRCFS0	SRC FS bit 0	RW			0
Bit 1	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 0	-	Reserved	Reserved	RW	Reserved	Reserved	0

SMBus Table: Device ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	DevID 7	Device ID MSB	R	-	-	1
Bit 6	-	DevID 6	Device ID 6	R	-	-	0
Bit 5	-	DevID 5	Device ID 5	R	-	-	0
Bit 4	-	DevID 4	Device ID4	R	-	-	0
Bit 3	-	DevID 3	Device ID3	R	-	-	0
Bit 2	-	DevID 2	Device ID2	R	-	-	0
Bit 1	-	DevID 1	Device ID1	R	-	-	0
Bit 0	-	DevID 0	Device ID LSB	R	-	-	1

SMBus Table: Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	Revision ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID (0001 = ICS)	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 9 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			1

SMBus Table: Reserved Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 6	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 3	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 1	-	Reserved	Reserved	RW	Reserved	Reserved	0
Bit 0	-	Reserved	Reserved	RW	Reserved	Reserved	0

SMBus Table: M/N Programming Enable

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	CPU and SRC PLL M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

SMBus Table: CPU Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bit (5:0)	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: CPU Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming Byte12 bit(7:0) and Byte11 bit(7:6)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the CPU VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: CPU Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming bit(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of CPU		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: CPU Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming bit(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage of CPU		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: SRC Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 15 and 16 will configure the SRC VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: SRC Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 15 and 16 will configure the SRC VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: SRC Spread Spectrum Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread pecentage of SRC		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: SRC Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 17 and 18 will program the spread pecentage of SRC		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: Programmable Output Divider Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUDiv3	CPU Divider Ratio Programming Bits	RW	See Table 2: CPU Divider Ratios		X
Bit 6	-	CPUDiv2		RW			X
Bit 5	-	CPUDiv1		RW			X
Bit 4	-	CPUDiv0		RW			X
Bit 3	-	HTTDiv3	HTT Divider Ratio Programming Bits (PCI divider is always 2x the HTT divider or 1/2 freq.)	RW	See Table 3: HTT Divider Ratios		X
Bit 2	-	HTTDiv2		RW			X
Bit 1	-	HTTDiv1		RW			X
Bit 0	-	HTTDiv0		RW			X

SMBus Table: Programmable Output Divider Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	X
Bit 6	-	Reserved	Reserved	R	-	-	X
Bit 5	-	Reserved	Reserved	R	-	-	X
Bit 4	-	Reserved	Reserved	R	-	-	X
Bit 3	-	SRC_Div3	SRC_ Divider Ratio Programming Bits	RW	See Table 4: SRC Divider Ratios		X
Bit 2	-	SRC_Div2		RW			X
Bit 1	-	SRC_Div1		RW			X
Bit 0	-	SRC_Div0		RW			X

SMBusTable: Test Byte Register

Byte 21	Test	Test Function	Type	Test Result	PWD
Bit 7	`	ICS ONLY TEST	RW	Reserved	0
Bit 6		ICS ONLY TEST	RW	Reserved	0
Bit 5		ICS ONLY TEST	RW	Reserved	0
Bit 4		ICS ONLY TEST	RW	Reserved	0
Bit 3		ICS ONLY TEST	RW	Reserved	0
Bit 2		ICS ONLY TEST	RW	Reserved	0
Bit 1		ICS ONLY TEST	RW	Reserved	0
Bit 0		ICS ONLY TEST	RW	Reserved	0

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS932S801** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

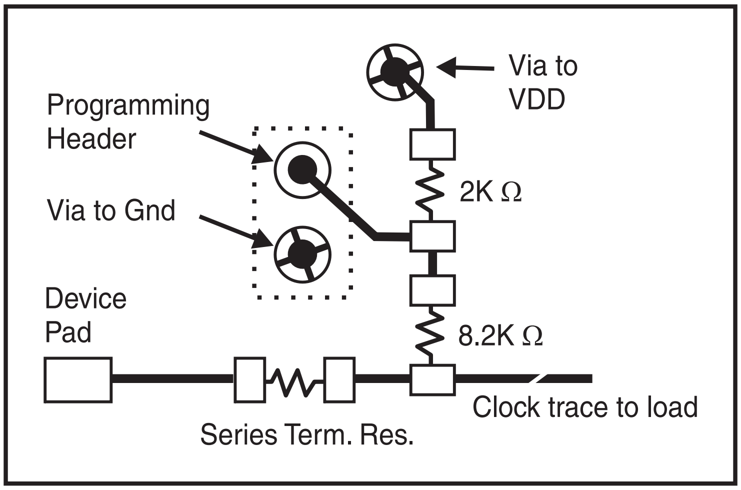
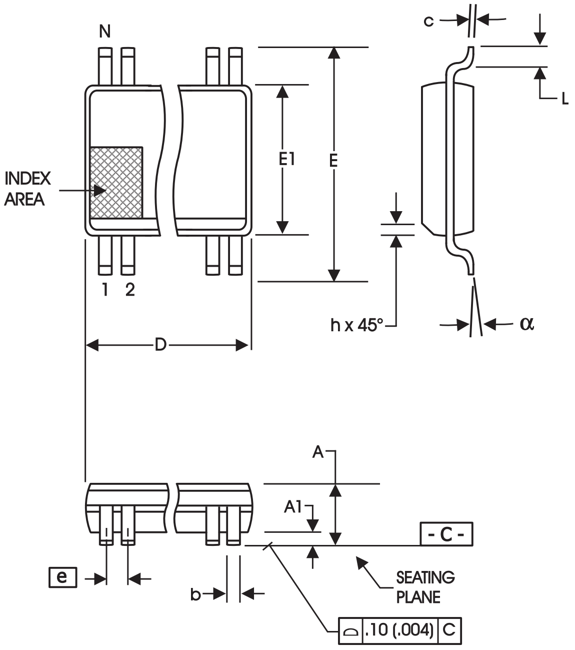


Fig. 1



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS932S801yFLFT

Example:

ICS XXXX y F - LF T

Designation for tape and reel packaging

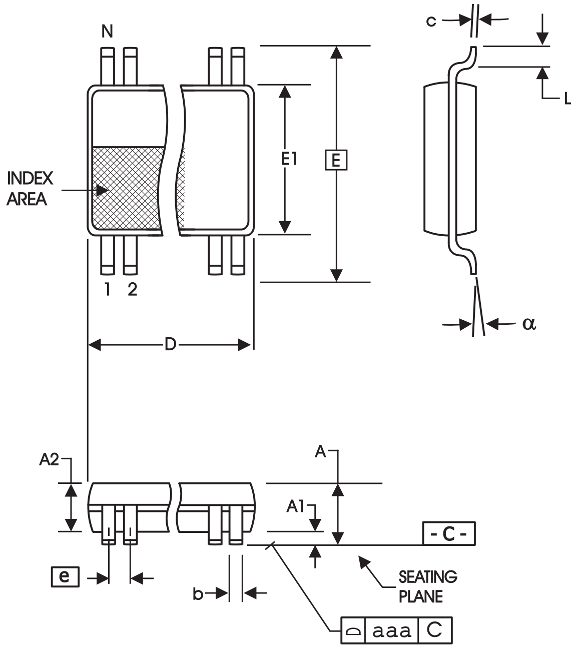
RoHS Compliant

Package Type
F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device



	(240 mil)		**(20 mil)**	
SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS932S801yGLFT

Example:

ICS XXXX y G - LF T

Designation for tape and reel packaging

RoHS Compliant

Package Type
G = TSSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device

Revision History

Rev.	Issue Date	Description	Page #
B	5/18/2005	1. Updated Electrical Characteristics Tables: i) Changed SRC jitter from 125ps to 100ps; ii) Changed PCI/HTT Skew from 500ps to 200ps; iii) Added USB Skew, 50ps. iv) Change REF Skew from 500ps to 50ps. 2. Updated LF Ordering Information from "Lead Free" to "RoHS Compliant".	14-16 18-19
C	3/13/2006	1. Correct pin description of PD# (Pin 21). It does not contain a pull up resistor. 2. Added PCIe Gen 1 phase noise numbers to SRC output characterisitics	2, 7

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