# Programmable Timing Control Hub™ for PII/III™

**Recommended Application:**

VIA Mobile PL133T and PLE133T Chipsets.

**Output Features:**

- 2 - CPU clocks @ 2.5V
- 1 - Pairs of differential CPU clocks @ 3.3V
- 7 - PCI including 1 free running @ 3.3V
- 7 - SDRAM @ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 1 - 24_48MHz selectable @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz

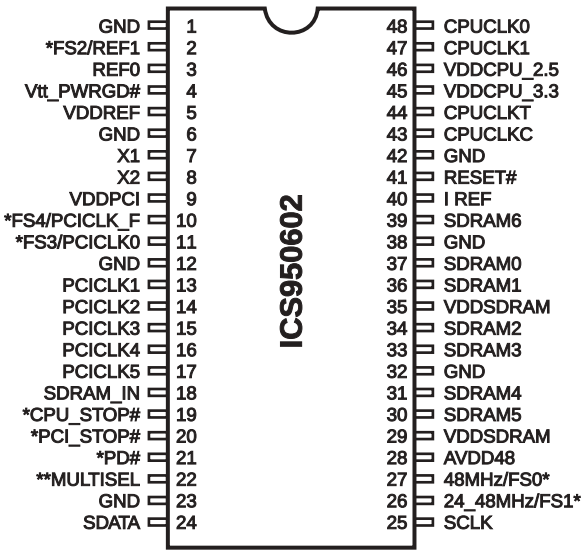
**Features/Benefits:**

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support $I^2C$ Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

**Key Specifications:**

- CPU Output Jitter <200ps
- CPU Output Skew <175ps
- PCI to PCI Output Skew <500ps

## Pin Configuration

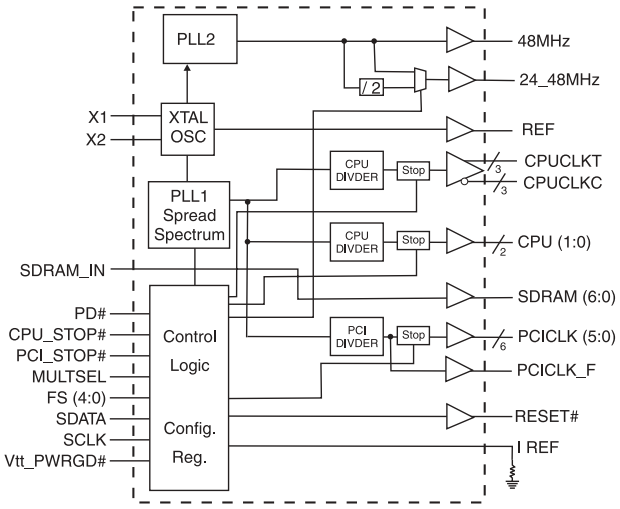



## 48-Pin SSOP & TSSOP

* Internal Pull-up resistor of 120K to VDD

** these inputs have 120K internal pull-down to GND

## Block Diagram




## Host Swing Select Functions

| MULTISEL0 | Board Target Trace/Term Z | Reference R, Iref = $V_{DD}$/(3*Rr) | Output Current | Voh @ Z |
|---|---|---|---|---|
| 0 | 50 ohms | Rr = 221 1%, Iref = 5.00mA | Ioh = 4* I REF | 1.0V @ 50 |
| 1 | 50 ohms | Rr = 475 1%, Iref = 2.32mA | Ioh = 6* I REF | 0.7V @ 50 |

## General Description

The **ICS950602** is a single chip clock solution for VIA Mobile PL133T and PLE133T chipsets. It provides all necessary clock signals for such a system.

The **ICS950602** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable $I^2C$ interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment. With all these programmable features, ICS' TCH makes motherboard testing, tuning and improvement very simple.

## Pin Description

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1, 6, 12, 23, 32, 38, 42, | GND | PWR | Ground pins for 3.3V supply |
| 5, 9, 29, 35 | VDD | PWR | 3.3V power supply |
| 2 | FS2 | IN | Logic input frequency select bit. Input latched at power on. |
| | REF1 | OUT | 3.3V, 14.318MHz reference clock output. |
| 3 | REF0 | OUT | 3.3V, 14.318MHz reference clock output. |
| 4 | Vtt_PWRGD# | IN | This 3.3V LVTTL input is a level sensitive strobe used to determine when FS (4:0) are valid and are ready to be sampled (active low) |
| 7 | X1 | IN | Crystal input, has internal load cap (33pF) and feedback resistor from X2 |
| 8 | X2 | OUT | Crystal output, nominally 14.318MHz. Has internal load cap (33pF) |
| 10 | FS4 | IN | Logic input frequency select bit. Input latched at power on. |
| | PCICLK_F | OUT | 3.3V PCI clock output |
| 11 | FS3 | IN | Logic input frequency select bit. Input latched at power on. |
| | PCICLK0 | OUT | 3.3V PCI clock output |
| 17, 16, 15, 14, 13 | PCICLK (5:1) | OUT | 3.3V PCI clock outputs |
| 18 | SDRAM_IN | IN | SDRAM buffer input pin. |
| 19 | CPU_STOP# | IN | Stops all CPUCLKs clocks at logic 0 level, when input low |
| 20 | PCI_STOP# | IN | Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low |
| 21 | PD# | IN | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 22 | MULTSEL | IN | 3.3V LVTTL input for selecting the current multiplier for CPU outputs. |
| 24 | SDATA | I/O | Data pin for $I^2C$ circuitry 5V tolerant |
| 25 | SCLK | IN | Clock pin for $I^2C$ circuitry 5V tolerant |
| 26 | FS1 | IN | Logic input frequency select bit. Input latched at power on. |
| | 48_24MHz | OUT | Selectable 48 or 24MHz output |
| 27 | FS0 | IN | Logic input frequency select bit. Input latched at power on. |
| | 48MHz | OUT | 3.3V Fixed 48MHz clock output. |
| 28 | AVDD48 | PWR | 3.3V analog power supply for 48 or 24MHz outputs. |
| 30, 31, 33, 34, 36, 37, 39 | SDRAM (5:0, 6) | OUT | SDRAM clock outputs. |
| 40 | I REF | OUT | This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. |
| 41 | RESET# | OUT | Real time system reset signal for frequency value or watchdog timer timeout. This signal is active low. |
| 43 | CPUCLKC | OUT | "Complementary" clock of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias. |
| 44 | CPUCLKT | OUT | "True" clock of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias. |
| 45 | VDDCPU_3.3 | PWR | 3.3V power for CPU differential clocks. |
| 46 | VDDCPU_2.5 | PWR | 2.5V power for CPU clocks. |
| 47, 48 | CPUCLK (1:0) | OUT | CPU clock outputs. |

# General I²C serial interface information

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

**Index Block Write Operation**

| Controller (Host) | | | ICS (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| | ○ | | |
| | ○ | | ○ |
| | ○ | | ○ |
| | | | ○ |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Index Block Read Operation**

| Controller (Host) | | ICS (Slave/Receiver) | |
|---|---|---|---|
| T | starT bit | | |
| Slave Address D2(H) | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address D3(H) | | | |
| RD | ReaD | | |
| | | ACK | |
| | | | |
| | | Data Byte Count = X | |
| ACK | | | |
| | | | Beginning Byte N |
| ACK | | | |
| | | | ○ |
| | ○ | | ○ |
| | ○ | | ○ |
| | ○ | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

*See notes on the following page.

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**Byte 0: Functionality and frequency select register (Default=0)**

| Bit | Description | | | | | | | | PWD |
|---|---|---|---|---|---|---|---|---|---|
| Bit (2:1,6:4) | Bit2 | Bit1 | Bit6 | Bit5 | Bit4 | CPUCLK MHz | PCICLK MHz | Spread % | Note 1 |
| | FS4 | FS3 | FS2 | FS1 | FS0 | | | | |
| | 0 | 0 | 0 | 0 | 0 | 200.00 | 33.30 | +/-0.25% center spread | |
| | 0 | 0 | 0 | 0 | 1 | 190.00 | 38.00 | +/-0.25% center spread | |
| | 0 | 0 | 0 | 1 | 0 | 180.00 | 36.00 | +/-0.25% center spread | |
| | 0 | 0 | 0 | 1 | 1 | 170.00 | 34.00 | +/-0.25% center spread | |
| | 0 | 0 | 1 | 0 | 0 | 166.00 | 33.20 | +/-0.25% center spread | |
| | 0 | 0 | 1 | 0 | 1 | 160.00 | 32.00 | +/-0.25% center spread | |
| | 0 | 0 | 1 | 1 | 0 | 150.00 | 37.50 | +/-0.25% center spread | |
| | 0 | 0 | 1 | 1 | 1 | 145.00 | 36.30 | +/-0.25% center spread | |
| | 0 | 1 | 0 | 0 | 0 | 140.00 | 35.00 | +/-0.25% center spread | |
| | 0 | 1 | 0 | 0 | 1 | 136.00 | 34.00 | +/-0.25% center spread | |
| | 0 | 1 | 0 | 1 | 0 | 130.00 | 32.50 | +/-0.25% center spread | |
| | 0 | 1 | 0 | 1 | 1 | 124.00 | 31.00 | +/-0.25% center spread | |
| | 0 | 1 | 1 | 0 | 0 | 67.20 | 33.60 | +/-0.25% center spread | |
| | 0 | 1 | 1 | 0 | 1 | 100.90 | 33.63 | +/-0.25% center spread | |
| | 0 | 1 | 1 | 1 | 0 | 118.00 | 39.30 | +/-0.25% center spread | |
| | 0 | 1 | 1 | 1 | 1 | 134.40 | 33.60 | +/-0.25% center spread | |
| | 1 | 0 | 0 | 0 | 0 | 67.00 | 33.50 | +/-0.25% center spread | |
| | 1 | 0 | 0 | 0 | 1 | 100.50 | 33.50 | +/-0.25% center spread | |
| | 1 | 0 | 0 | 1 | 0 | 115.00 | 38.30 | +/-0.25% center spread | |
| | 1 | 0 | 0 | 1 | 1 | 133.90 | 33.47 | +/-0.25% center spread | |
| | 1 | 0 | 1 | 0 | 0 | 66.80 | 33.40 | +/-0.25% center spread | |
| | 1 | 0 | 1 | 0 | 1 | 100.20 | 33.40 | +/-0.25% center spread | |
| | 1 | 0 | 1 | 1 | 0 | 110.00 | 36.70 | +/-0.25% center spread | |
| | 1 | 0 | 1 | 1 | 1 | 133.60 | 33.40 | +/-0.25% center spread | |
| | 1 | 1 | 0 | 0 | 0 | 105.00 | 35.00 | +/-0.25% center spread | |
| | 1 | 1 | 0 | 0 | 1 | 90.00 | 30.00 | +/-0.25% center spread | |
| | 1 | 1 | 0 | 1 | 0 | 85.00 | 28.30 | +/-0.25% center spread | |
| | 1 | 1 | 0 | 1 | 1 | 78.00 | 39.00 | +/-0.25% center spread | |
| | 1 | 1 | 1 | 0 | 0 | 66.60 | 33.30 | +/-0.25% center spread | |
| | 1 | 1 | 1 | 0 | 1 | 100.00 | 33.30 | 0 to -0.5% down spread | |
| | 1 | 1 | 1 | 1 | 0 | 75.00 | 37.50 | +/-0.25% center spread | |
| | 1 | 1 | 1 | 1 | 1 | 133.30 | 33.30 | 0 to -0.5% down spread | |
| Bit 3 | 0 - Frequency is selected by hardware select, latched inputs<br>1 - Frequency is selected by Bit 2,7:4 | | | | | | | | 0 |
| Bit 0 | 0 - Normal<br>1 - Spread spectrum enable | | | | | | | | 0 |
| Bit 7 | 0 - Watch dog safe frequency will be selected by latch inputs<br>1 - Watch dog safe frequency will be programmed by Byte 10 bit (4:0) | | | | | | | | 0 |

**Notes:**

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

**Byte 1: Output Control Register**
**(1 = enable, 0 = disable)**

| Bit | Pin# | PWD | Description |
|---|---|---|---|
| Bit7 | - | X | FS4 Read back |
| Bit6 | - | X | FS3 Read back |
| Bit5 | - | X | FS2 Read back |
| Bit4 | - | X | FS1 Read back |
| Bit3 | - | X | FS0 Read back |
| Bit2 | 48 | 1 | CPUCLK0 |
| Bit1 | 47 | 1 | CPUCLK1 |
| Bit0 | 44, 43 | 1 | CPUCLKT, CPUCLKC |

**Byte 2: Output Control Register**
**(1 = enable, 0 = disable)**

| Bit | Pin# | PWD | Description |
|---|---|---|---|
| Bit7 | 39 | 1 | SDRAM6 |
| Bit6 | 10 | 1 | PCICLK_F |
| Bit5 | 17 | 1 | PCICLK5 |
| Bit4 | 16 | 1 | PCICLK4 |
| Bit3 | 15 | 1 | PCICLK3 |
| Bit2 | 14 | 1 | PCICLK2 |
| Bit1 | 13 | 1 | PCICLK1 |
| Bit0 | 11 | 1 | PCICLK0 |

**Byte 3: Output Control Register**
**(1 = enable, 0 = disable)**

| Bit | Pin# | PWD | Description |
|---|---|---|---|
| Bit7 | - | 0 | RESET gear shift detect 1 = Enable, 0 = Disable |
| Bit6 | - | 0 | SEL24_48: 0 = 24, 1 = 48 |
| Bit5 | 27 | 1 | 48MHz |
| Bit4 | 26 | 1 | 24_48MHz |
| Bit3 | - | 0 | Reserved |
| Bit2 | 31, 30 | 1 | SDRAM (4:5) |
| Bit1 | 34, 33 | 1 | SDRAM (2:3) |
| Bit0 | 37, 36 | 1 | SDRAM (0:1) |

**Byte 4: Output Control Register**
**(1 = enable, 0 = disable)**

| Bit | Pin# | PWD | Description |
|---|---|---|---|
| Bit 7 | - | X | MULTSEL Read back |
| Bit 6 | - | X | Reserved |
| Bit 5 | - | X | Reserved |
| Bit 4 | - | X | Reserved |
| Bit 3 | - | X | Reserved |
| Bit 2 | - | X | Reserved |
| Bit 1 | - | X | Reserved |
| Bit 0 | - | X | Reserved |

**Byte 5: Output Control Register**
**(1 = enable, 0 = disable)**

| Bit | Pin# | PWD | Description |
|---|---|---|---|
| Bit 7 | - | 0 | Reserved |
| Bit 6 | - | 0 | Reserved |
| Bit 5 | - | 0 | Reserved |
| Bit 4 | - | 0 | CPUCLK0 Free running control,<br>0 = Not free running 1 = Free running |
| Bit 3 | - | 0 | CPUCLK1 Free running control,<br>0 = Not free running 1 = Free running |
| Bit 2 | - | 0 | CPUCLKT/C Free running control,<br>0 = Not free running 1 = Free running |
| Bit 1 | 2 | 1 | REF1 |
| Bit 0 | 3 | 1 | REF0 |

**Byte 6: Reserved Register**
**(1 = enable, 0 = disable)**

| Bit | Pin# | PWD | Description |
|---|---|---|---|
| Bit 7 | - | 0 | Reserved |
| Bit 6 | - | 0 | Reserved |
| Bit 5 | - | 0 | Reserved |
| Bit 4 | - | 0 | Reserved |
| Bit 3 | - | 0 | Reserved |
| Bit 2 | - | 0 | Reserved |
| Bit 1 | - | 0 | Reserved |
| Bit 0 | - | 0 | Reserved |

**Byte 7: Byte Count Read Back Register**

| Bit | Name | PWD | Description |
|---|---|---|---|
| Bit 7 | Byte7 | 0 | Default Byte count read back is 15 Byte. |
| Bit 6 | Byte6 | 0 | |
| Bit 5 | Byte5 | 0 | |
| Bit 4 | Byte4 | 0 | |
| Bit 3 | Byte3 | 1 | |
| Bit 2 | Byte2 | 1 | |
| Bit 1 | Byte1 | 1 | |
| Bit 0 | Byte0 | 1 | |

**Byte 8: Vendor ID Register**

| Bit | Name | PWD | Description |
|---|---|---|---|
| Bit 7 | Revision ID Bit3 | X | Revision ID values will be based on individual device's revision |
| Bit 6 | Revision ID Bit2 | X | |
| Bit 5 | Revision ID Bit1 | X | |
| Bit 4 | Revision ID Bit0 | X | |
| Bit 3 | Vendor ID Bit3 | 0 | (Reserved) |
| Bit 2 | Vendor ID Bit2 | 0 | (Reserved) |
| Bit 1 | Vendor ID Bit1 | 0 | (Reserved) |
| Bit 0 | Vendor ID Bit0 | 1 | (Reserved) |

**Byte 9: Watchdog Timer Count Register**

| Bit | Name | PWD | Description |
|---|---|---|---|
| Bit 7 | WD7 | 0 | The decimal representation of these 8 bits correspond to X • 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16 • 290ms = 4.64 seconds. |
| Bit 6 | WD6 | 0 | |
| Bit 5 | WD5 | 0 | |
| Bit 4 | WD4 | 1 | |
| Bit 3 | WD3 | 0 | |
| Bit 2 | WD2 | 0 | |
| Bit 1 | WD1 | 0 | |
| Bit 0 | WD0 | 0 | |

**Byte 10: Programming Enable bit 8 Watchdog Control Register**

| Bit | Name | PWD | Description |
|---|---|---|---|
| Bit 7 | Program Enable | 0 | Programming Enable bit<br>0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all I²C programing. |
| Bit 6 | WD Enable | 0 | Watchdog Enable bit.<br>This bit will over write WDEN latched value. 0 = disable, 1 = Enable. |
| Bit 5 | WD Alarm | 0 | Watchdog Alarm Status 0 = normal 1= alarm status |
| Bit 4 | SF4 | 1 | Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corrsponding to Byte 0 Bit 2, 7:4 table |
| Bit 3 | SF3 | 1 | |
| Bit 2 | SF2 | 1 | |
| Bit 1 | SF1 | 1 | |
| Bit 0 | SF0 | 1 | |

**Byte 11: VCO Frequency M Divider (Reference divider) Control Register**

| Bit | Name | PWD | Description |
|---|---|---|---|
| Bit 7 | Ndiv 8 | X | N divider bit 8 |
| Bit 6 | Mdiv 6 | X | The decimal respresentation of Mdiv (6:0) corresposd to the reference divider value. Default at power up is equal to the latched inputs selection. |
| Bit 5 | Mdiv 5 | X | |
| Bit 4 | Mdiv 4 | X | |
| Bit 3 | Mdiv 3 | X | |
| Bit 2 | Mdiv 2 | X | |
| Bit 1 | Mdiv 1 | X | |
| Bit 0 | Mdiv 0 | X | |

**Byte 12: VCO Frequency N Divider (VCO divider) Control Register**

| Bit | Name | PWD | Description |
|---|---|---|---|
| Bit 7 | Ndiv 7 | X | The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selecton. Notice Ndiv 8 is located in Byte 11. |
| Bit 6 | Ndiv 6 | X | |
| Bit 5 | Ndiv 5 | X | |
| Bit 4 | Ndiv 4 | X | |
| Bit 3 | Ndiv 3 | X | |
| Bit 2 | Ndiv 2 | X | |
| Bit 1 | Ndiv 1 | X | |
| Bit 0 | Ndiv 0 | X | |

**Byte 13: Spread Spectrum Control Register**

| Bit | Name | PWD | Description |
|---|---|---|---|
| Bit 7 | SS 7 | X | The Spread Spectrum will program the spread precentage. Spread precent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use ICS software for spread programming. Default power on is latched FS divider. |
| Bit 6 | SS 6 | X | |
| Bit 5 | SS 5 | X | |
| Bit 4 | SS 4 | X | |
| Bit 3 | SS 3 | X | |
| Bit 2 | SS 2 | X | |
| Bit 1 | SS 1 | X | |
| Bit 0 | SS 0 | X | |

**Byte 14: Spread Spectrum Control Register**

| Bit | Name | PWD | Description |
|---|---|---|---|
| Bit 7 | Reserved | X | Reserved |
| Bit 6 | Reserved | X | Reserved |
| Bit 5 | Reserved | X | Reserved |
| Bit 4 | SS 12 | X | Spread Spectrum Bit 12 |
| Bit 3 | SS 11 | X | Spread Spectrum Bit 11 |
| Bit 2 | SS 10 | X | Spread Spectrum Bit 10 |
| Bit 1 | SS 9 | X | Spread Spectrum Bit 9 |
| Bit 0 | SS 8 | X | Spread Spectrum Bit 8 |

## Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to $V_{DD}$ +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Case Temperature . . . . . 115°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70°C; Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | 2 | | $V_{DD}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | | $V_{SS}$ - 0.3 | | 0.8 | V |
| Input High Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | -5 | | 5 | mA |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | mA |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | |
| Operating Supply Current | $I_{DD3.3OP}$ | $C_L$ = 0 pF; Select @ 67 MHz | | | 100 | mA |
| | | $C_L$ =Full load, SDRAM not running | | 144 | 280 | |
| Powerdown Current | $I_{DD3.3PD}$ | IREF = 2.32 mA | | | 20 | mA |
| | | IREF = 5 mA | | 22 | 37 | |
| Input Frequency | $F_i$ | $V_{DD}$ = 3.3 V | | 14.32 | | MHz |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH |
| Input Capacitance[1] | $C_{IN}$ | Logic Inputs | | | 5 | pF |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF |
| | $C_{INX}$ | X1 & X2 pins | 27 | | 45 | pF |
| Transition time[1] | $T_{trans}$ | To 1st crossing of target frequency | | | 3 | ms |
| Settling time[1] | $T_s$ | From 1st crossing to 1% target frequency | | | 3 | ms |
| Clk Stabilization[1] | $T_{STAB}$ | From $V_{DD}$ = 3.3 V to 1% target frequency | | | 3 | ms |
| Delay[1] | $t_{PZH}$,$t_{PZL}$ | Output enable delay (all outputs) | 1 | | 10 | ns |
| | $t_{PHZ}$,$t_{PLZ}$ | Output disable delay (all outputs) | 1 | | 10 | ns |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - CPUCLK(T,C)

$T_A$ = 0 - 70°C; $V_{DD}$=3.3V +/-5%; loads from Intel CK408B spec, Rev 1.1 (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Current Source Output Impedance[1] | $Z_{O2A}$ | $V_O = V_x$ | 3000 | | | Ω |
| Output High Voltage | $V_{OH2A}$ | $V_R$ = 475Ω ±1%; IREF = 2.32 mA; $I_{OH}$ = 6*IREF | | 0.71 | 1.2 | V |
| Output High Current | $I_{OH32A}$ | | | -13.92 | | mA |
| Rise Time[1] | $t_{r2A}$ | $V_{OL}$ = -0.35V, $V_{OH}$ = 0.35V | 175 | 220 | 467 | ps |
| Fall Time[1] | $t_{f2A}$ | $V_{OH}$ = 0.35V, $V_{OL}$ = -0.35V | 175 | 230 | 467 | ps |
| Differential Crossover Voltage[1] | $V_{2A}$ | Rs = 33.2Ω, Rp = 63.4Ω to gnd, $R_{T-C}$ = 475Ω | 510 | 700 | 900 | mV |
| Duty Cycle[1] | $d_{t2A}$ | $V_T$ = crossing point | 45 | 49 | 55 | % |
| Skew, CPUT,C to CPU[1] | $t_{sk2A}$ | $V_T$ (CPU) = crossing point, $V_T$ (PCI) = 1.25 V 100 MHz | | 250 | 300 | ps |
| | | 133 MHz | | 170 | 200 | |
| Skew, CPUT,C to PCI[1] | $t_{sk2A1}$ | $V_T$ (CPU) = crossing point, $V_T$ (PCI) = 1.5 V | 2 | 3.2 | 4 | ns |
| Jitter, Cycle to cycle[1] | $t_{jcyc-cyc2A}$ | $V_T$ = crossing point CPU,SD = 100MHz | | 50 | 200 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - CPUCLK(1:0)

$T_A$ = 0 - 70°C; $V_{DD}$=3.3V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Impedance[1] | $R_{DSP2B}$ | $V_O = V_{DD}$*(0.5) | 13.5 | | 45 | Ω |
| Output Impedance[1] | $R_{DSN2B}$ | $V_O = V_{DD}$*(0.5) | 13.5 | | 45 | |
| Output High Voltage | $V_{OH2B}$ | $I_{OH}$ = -1 mA | 2 | | | V |
| Output Low Voltage | $V_{OL2B}$ | $I_{OL}$ = 1 mA | | | 0.4 | |
| Output High Current | $I_{OH2B}$ | $V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 2.375 V | -27 | | 27 | V |
| Output Low Current | $I_{OL2B}$ | $V_{OL@MIN}$ = 1.2 V, $V_{OL@MIN}$ = 0.3 V | 27 | | 30 | |
| Rise Time[1] | $t_{r2B}$ | $V_{OL}$ = 0.4V, $V_{OH}$ = 2.0V | 0.4 | 0.7 | 1.6 | ns |
| Fall Time[1] | $t_{f2B}$ | $V_{OH}$ = 2.0V $V_{OL}$ = 0.4V | | 0.8 | | |
| Duty Cycle[1] | $d_{t2B}$ | $V_T$ = 50% 100MHz | 45 | 50 | 55 | % |
| | | 133 MHz | | 54 | | |
| Skew, CPU to CPU[1] | $t_{sk2B}$ | $V_T$ = 1.25 V | | 60 | 175 | ps |
| Skew, CPU to PCI[1] | $t_{sk2B1}$ | $V_T$ (CPU) = 1.25 V, $V_T$ (PCI) = 1.5 V | 2 | 3.2 | 4 | ns |
| Jitter, Cycle to cycle[1] | $t_{jcyc-cyc2B}$ | $V_T$ = 1.25V CPU,SD = 100MHz | | 140 | 250 | ps |
| | | CPU,SD = 133 MHz | | 100 | 250 | |
| | | CPU = 100, SD = 133 MHz | | 220 | 275 | |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - PCICLK

$T_A$ = 0 - 70°C; $V_{DD}$=3.3V +/-5%; $C_L$ = 10-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Frequency | $F_{O1}$ | | | 33.33 | | MHz |
| Output Impedance | $R_{DSP1}$[1] | $V_O = V_{DD}*(0.5)$ | 12 | | 55 | Ω |
| Output High Voltage | $V_{OH1}$[1] | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL1}$[1] | $I_{OL}$ = 1 mA | | | 0.55 | V |
| Output High Current | $I_{OH1}$[1] | $V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V | -33 | | -33 | mA |
| Output Low Current | $I_{OL1}$[1] | $V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V | 30 | | 38 | mA |
| Rise Time | $t_{r1}$[1] | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.5 | 2.4 | 2.5 | ns |
| Fall Time | $t_{f1}$[1] | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.5 | 2.25 | 2.5 | ns |
| Duty Cycle | $d_{t1}$[1] | $V_T$ = 1.5 V | 45 | 53 | 55 | % |
| Skew | $t_{sk1}$[1] | $V_T$ = 1.5 V | | 220 | 500 | ps |
| Jitter,cycle to cycle | $t_{jcyc-cyc}$[1] | $V_T$ = 1.5 V | | 300 | 450 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 48MHz, 24_48MHz

$T_A$ = 0 - 70°C; $V_{DD}$=3.3V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Frequency | $F_{O3}$[1] | | | 48 | | MHz |
| Output Impedance | $R_{DSP3}$[1] | $V_O = V_{DD}*(0.5)$ | 12 | | 55 | Ω |
| Output High Voltage | $V_{OH3}$[1] | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL3}$[1] | $I_{OL}$ = 1 mA | | | 0.55 | V |
| Output High Current | $I_{OH3}$[1] | $V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V | -29 | | -23 | mA |
| Output Low Current | $I_{OL3}$[1] | $V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V | 29 | | 27 | mA |
| Rise Time | $t_{r3A}$[1] | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.1 | 2 | ns |
| Fall Time | $t_{f3B}$[1] | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.25 | 2 | ns |
| Duty Cycle | $d_{t3A}$[1] | $V_T$ = 1.5 V | 45 | 52 | 55 | % |
| Jitter, cycle-to-cycle | $t_{jcyc-cyc3}$[1] | $V_T$ = 1.5 V | | 200 | 350 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - SDRAM

$T_A$ = 0 - 70°C; $V_{DD}$=3.3V +/-5%; $C_L$ = 10-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Impedance[1] | $R_{DSP5}$ | Vo=$V_{DD}$*(0.5) | 10 | | 24 | Ω |
| Output Impedance[1] | $R_{DSN5}$ | Vo=$V_{DD}$*(0.5) | 10 | | 24 | Ω |
| Output High Voltage | $V_{OH5}$ | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL5}$ | $I_{OL}$ = 1 mA | | | 0.4 | V |
| Output High Current | $I_{OH5}$ | $V_{OH@MIN}$ = 2 V | | | -46 | mA |
| | | $V_{OH@MAX}$ = 3.135V | -54 | | | |
| Output Low Current | $I_{OL5}$ | $V_{OL@MIN}$ = 1 V | 54 | | | mA |
| | | $V_{OL@MAX}$ =0.4V | | | 53 | |
| Rise Time | $t_{r5}$[1] | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 0.4 | 1.1 | 1.6 | ns |
| Fall Time | $t_{f5}$[1] | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 0.4 | 0.75 | 1.6 | ns |
| Duty Cycle | $d_{t5}$[1] | $V_T$ = 1.5 V | 45 | 50 | 55 | % |
| Skew | $t_{sk5}$[1] | $V_T$ = 1.5 V | | 30 | 250 | ps |
| Propagation delay SDRAM_IN to SDRAM | $t_{pdel5}$[1] | $V_T$ = 1.5 V | | 2.95 | 4 | ns |

[1]Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - REF

$T_A$ = 0 - 70°C; $V_{DD}$=3.3V +/-5%; $C_L$ = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Output Frequency | $F_{O4}$[1] | | | 14.318 | | MHz |
| Output Impedance | $R_{DSP4}$[1] | $V_O$ = $V_{DD}$*(0.5) | 20 | | 60 | Ω |
| Output High Voltage | $V_{OH4}$[1] | $I_{OH}$ = -1 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL4}$[1] | $I_{OL}$ = 1 mA | | | 0.4 | V |
| Output High Current | $I_{OH4}$[1] | $V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V | -29 | | -23 | mA |
| Output Low Current | $I_{OL4}$[1] | $V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V | 29 | | 27 | mA |
| Rise Time | $t_{r4}$[1] | $V_{OL}$ = 0.4 V, $V_{OH}$ = 2.4 V | 1 | 1.85 | 4 | ns |
| Fall Time | $t_{f4}$[1] | $V_{OH}$ = 2.4 V, $V_{OL}$ = 0.4 V | 1 | 1.95 | 4 | ns |
| Duty Cycle | $d_{t1}$[1] | $V_T$ = 1.5 V | 45 | 55.7 | 56 | % |
| Jitter, cycle-to-cycle | $t_{jcyc-cyc4}$[1] | $V_T$ = 1.5 V | | 365 | 550 | ps |

[1]Guaranteed by design, not 100% tested in production.

## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

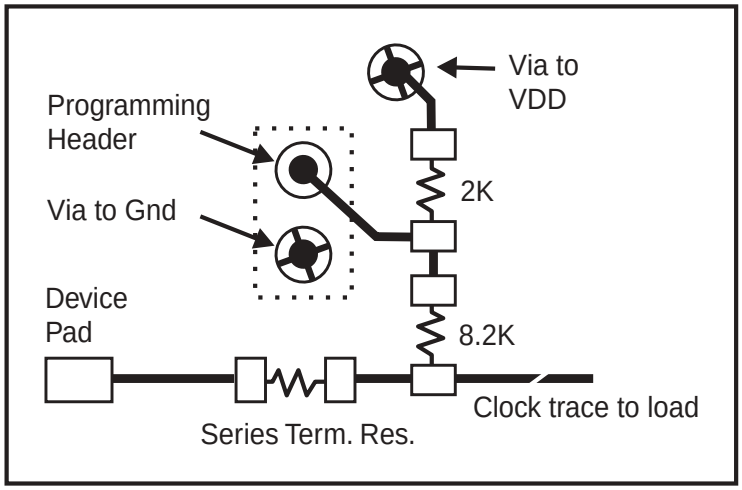
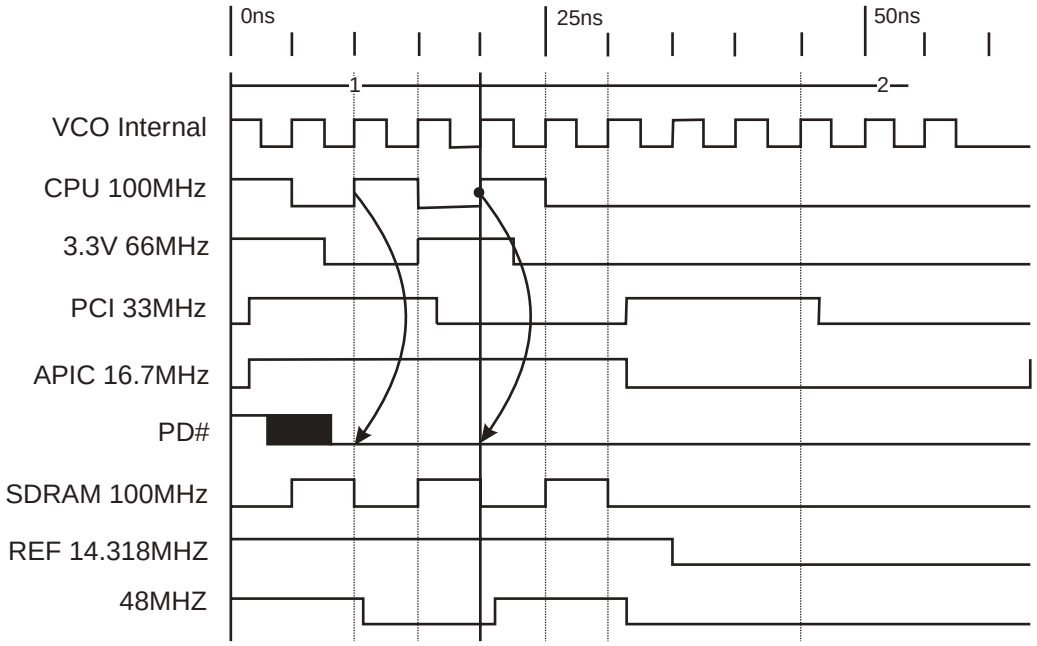



**Fig. 1**

## Power Down Waveform

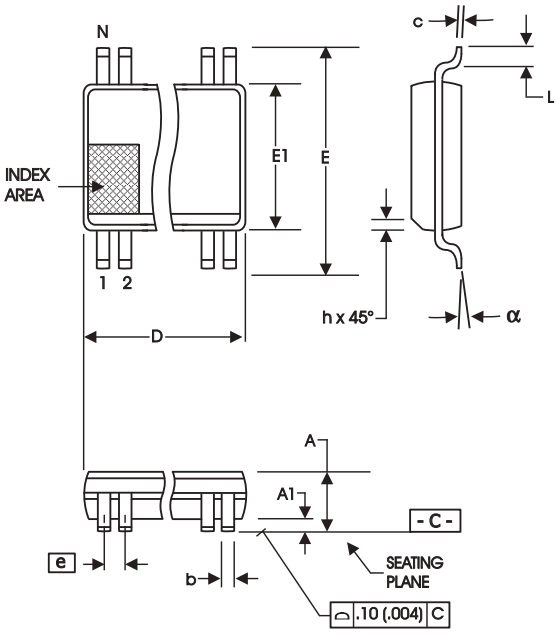



**Note**

**1.** After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

**2**. Power-up latency <3ms.

**3.** Waveform shown for 100MHz




**300 mil SSOP Package**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 15.75 | 16.00 | .620 | .630 |

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

## Ordering Information

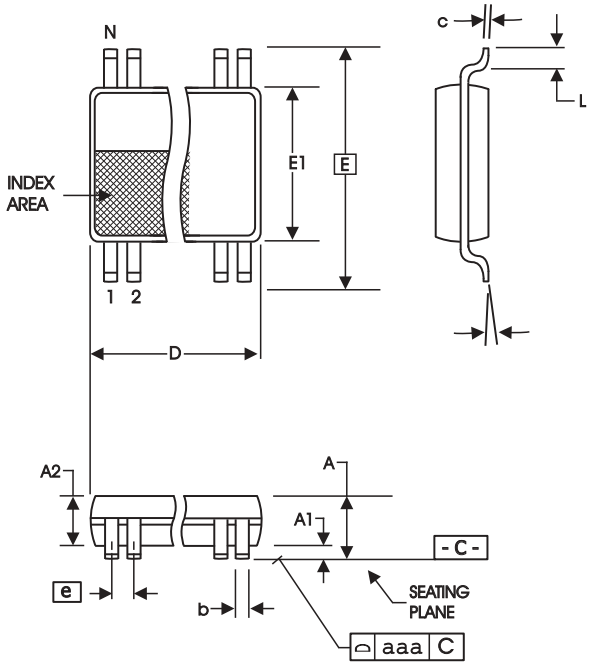
**ICS950602yFT**

Example:

**ICS XXXX y F - T**

- **Designation for tape and reel packaging**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device

0469B—12/18/02




**6.10 mm. Body, 0.50 mm. pitch TSSOP**
**(240 mil) (20 mil)**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 48 | 12.40 | 12.60 | .488 | .496 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

## Ordering Information

**ICS950602yGT**

Example:

**ICS XXXX y G - T**

- **Designation for tape and reel packaging**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device

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