Programmable System Clock Chip for ATI RS/RD690 K8™ - based Systems

ICS951464

Recommended Application:

ATI RS/RD690 systems using AMD K8 processors & SB600 Southbridge

Output Features:

- 2 - 0.7V current-mode differential CPU pairs
- 6 - 0.7V current-mode differential SRC pairs
- 2 - 0.7V current-mode differential ATIG pairs
- 1 - HyperTransport clock seed
- 2 - 48MHz USB clock
- 3 - 14.318MHz Reference clock

Key Specifications:

- CPU outputs cycle-to-cycle jitter < 85ps
- SRC outputs cycle-to-cycle jitter < 125ps
- ATIG outputs cycle-to-cycle jitter < 125ps
- +/- 300ppm frequency accuracy on CPU, SRC & ATIG clocks

Features/Benefits:

- 3 - Programmable Clock Request pins for SRC and ATIG clocks
- ATIGCLKs are programmable for frequency
- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- External crystal load capacitors for maximum frequency accuracy

Pin Configuration

95146 4AGLF

Signal	Pin	Pin	Signal
GNDREF	1	56	FS0/REF0
VDDREF	2	55	FS1/REF1
X1	3	54	FS2/REF2
X2	4	53	**PD
VDD48	5	52	VDDHTT
48MHz_0	6	51	HTTCLK0
48MHz_1	7	50	GNDHTT
GND48	8	49	*CLKREQA#
SMBCLK	9	48	CPUCLK8T0
SMBDAT	10	47	CPUCLK8C0
RESET_IN#	11	46	VDDCPU
SRCCLKT7	12	45	GNDCPU
SRCCLKC7	13	44	CPUCLK8T1
VDDSRC	14	43	CPUCLK8C1
GNDSRC	15	42	VDDA
SRCCLKT6	16	41	GNDA
SRCCLKC6	17	40	IREF
SRCCLKT5	18	39	SRCCLKT0
SRCCLKC5	19	38	SRCCLKC0
SRCCLKT4	20	37	GNDSRC
SRCCLKC4	21	36	VDDSRC
GNDSRC	22	35	ATIGCLKT0
VDDSRC	23	34	ATIGCLKC0
SRCCLKT2	24	33	VDDATIG
SRCCLKC2	25	32	GNDATIG
VDDSRC	26	31	ATIGCLKT1
GNDSRC	27	30	ATIGCLKC1
*CLKREQB#	28	29	*CLKREQC#

56-Pin SSOP/TSSOP

Note: Pins preceeded by * have a 120 Kohm Internal Pull Up resistor
Pins preceeded by ** have a 120 Kohm Internal Pull Down resistor

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	GNDREF	PWR	Ground pin for the REF outputs.
2	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
3	X1	IN	Crystal input, Nominally 14.318MHz.
4	X2	OUT	Crystal output, Nominally 14.318MHz
5	VDD48	PWR	Power pin for the 48MHz output.3.3V
6	48MHz_0	OUT	48MHz clock output.
7	48MHz_1	OUT	48MHz clock output.
8	GND48	PWR	Ground pin for the 48MHz outputs
9	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
10	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
11	RESET_IN#	IN	Real time active low input. When active, SMBus is reset to power up default.
12	SRCCLKT7	OUT	True clock of differential SRC clock pair.
13	SRCCLKC7	OUT	Complement clock of differential SRC clock pair.
14	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
15	GNDSRC	PWR	Ground pin for the SRC outputs
16	SRCCLKT6	OUT	True clock of differential SRC clock pair.
17	SRCCLKC6	OUT	Complement clock of differential SRC clock pair.
18	SRCCLKT5	OUT	True clock of differential SRC clock pair.
19	SRCCLKC5	OUT	Complement clock of differential SRC clock pair.
20	SRCCLKT4	OUT	True clock of differential SRC clock pair.
21	SRCCLKC4	OUT	Complement clock of differential SRC clock pair.
22	GNDSRC	PWR	Ground pin for the SRC outputs
23	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
24	SRCCLKT2	OUT	True clock of differential SRC clock pair.
25	SRCCLKC2	OUT	Complement clock of differential SRC clock pair.
26	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
27	GNDSRC	PWR	Ground pin for the SRC outputs
28	*CLKREQB#	IN	Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = enabled, 1 = tri-stated

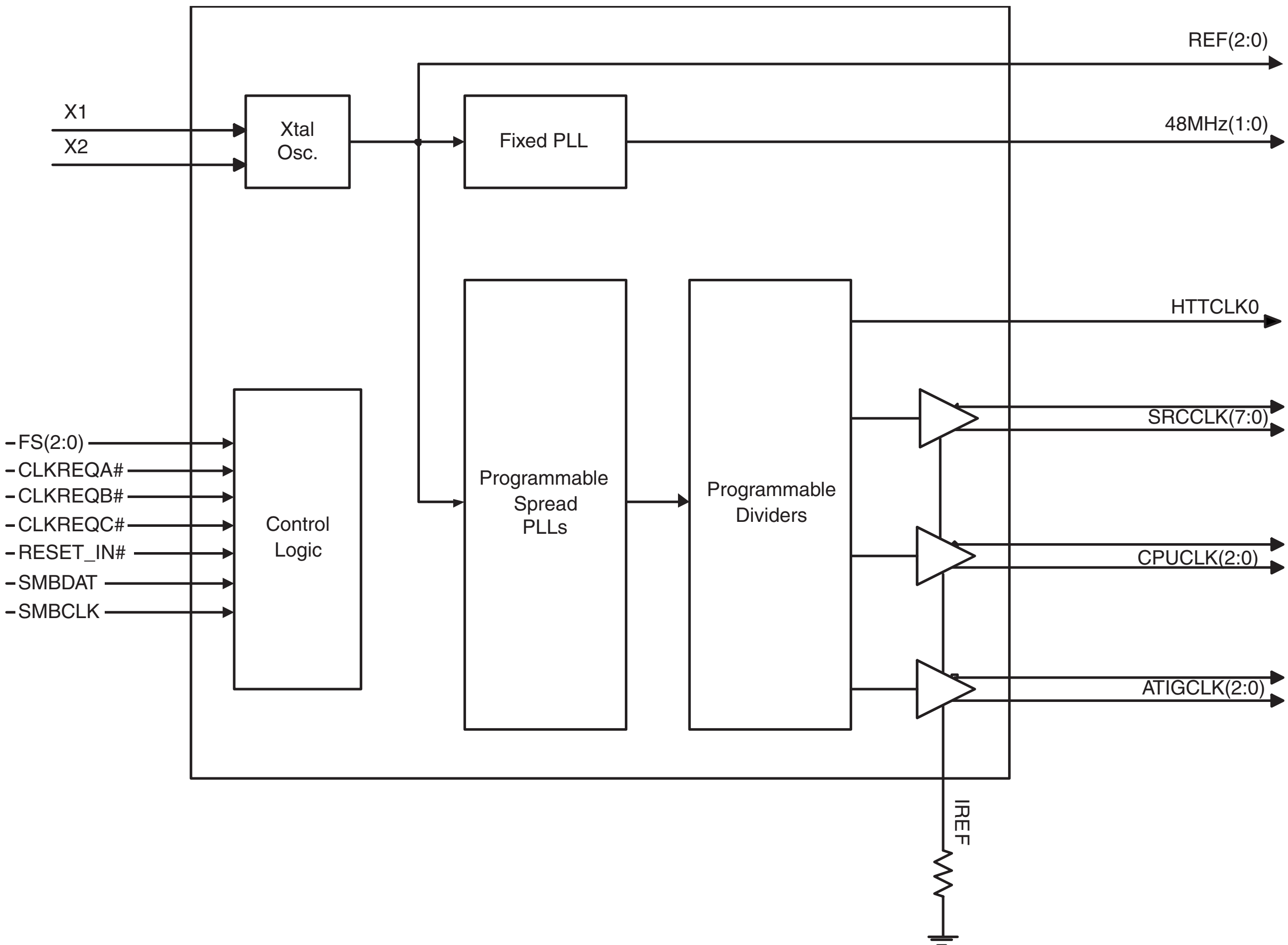
Pin Description (Continued)

PIN #	PIN NAME	TYPE	DESCRIPTION
29	*CLKREQC#	IN	Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = enabled, 1 = tri-stated
30	ATIGCLKC1	OUT	Complementary clock of differential ATIGCLK clock pair.
31	ATIGCLKT1	OUT	True clock of differential ATIGCLK clock pair.
32	GNDATIG	PWR	Ground for ATIG clocks
33	VDDATIG	PWR	Power supply ATIG clocks, nominal 3.3V
34	ATIGCLKC0	OUT	Complementary clock of differential ATIGCLK clock pair.
35	ATIGCLKT0	OUT	True clock of differential ATIGCLK clock pair.
36	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
37	GNDSRC	PWR	Ground pin for the SRC outputs
38	SRCCLKC0	OUT	Complement clock of differential SRC clock pair.
39	SRCCLKT0	OUT	True clock of differential SRC clock pair.
40	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
41	GNDA	PWR	Ground pin for the PLL core.
42	VDDA	PWR	3.3V power for the PLL core.
43	CPUCLK8C1	OUT	Complementary clock of differential 3.3V push-pull K8 pair.
44	CPUCLK8T1	OUT	True clock of differential 3.3V push-pull K8 pair.
45	GNDCPU	PWR	Ground pin for the CPU outputs
46	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
47	CPUCLK8C0	OUT	Complementary clock of differential 3.3V push-pull K8 pair.
48	CPUCLK8T0	OUT	True clock of differential 3.3V push-pull K8 pair.
49	*CLKREQA#	IN	Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = enabled, 1 = tri-stated
50	GNDHTT	PWR	Ground pin for the HTT outputs
51	HTTCLK0	OUT	3.3V Hyper Transport output
52	VDDHTT	PWR	Supply for HTT clocks, nominal 3.3V.
53	**PD	IN	Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped.
54	FS2/REF2	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
55	FS1/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
56	FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.

General Description

The **ICS951464** is a main clock synthesizer chip that provides all clocks required for ATI RS/RD690-based systems. An SMBus interface allows full control of the device.

Block Diagram



951464 Power Group Table

VDD Pin#	GND Pin#	Description
2	1	Crsytal, REF VDD & VSS I/O & Core
5	8	48M Core and Output; FIX PLL Analog/Digital
14,26	15,27	SRC I/O & Core
23	22	SRC I/O & Core; SRC PLL Digital
36	37	SRC I/O & Core; SRC PLL Analog
33	32	ATIG I/O & Core; ATIG PLL Analog/Digital
42	41	CPU PLL Analog
46	45	CPU I/O & Core; CPU PLL Digital
52	50	HTT I/O & Core

Table1: CPU and HTT Frequency Selection Table

Byte 0					CPUCLK (2:0) (MHz)	HTT (MHz)	Spread %	Overclock %
Bit4	Bit3	Bit2	Bit1	Bit0				
CPU SS_EN	CPU FS3	CPU FS2	CPU FS1	CPU FS0				
0	0	0	0	0	Hi-Z	Hi-Z	None	
0	0	0	0	1	X / 2	X / 3	None	
0	0	0	1	0	230.00	76.67	None	**15%**
0	0	0	1	1	240.00	80.00	None	**20%**
0	0	1	0	0	100.00	66.67	None	**0%**
0	0	1	0	1	133.33	66.67	None	
0	0	1	1	0	166.67	66.67	None	
0	0	1	1	1	200.00	66.67	None	
0	1	0	0	0	250.00	83.33	None	**25%**
0	1	0	0	1	260.00	86.67	None	**30%**
0	1	0	1	0	270.00	90.00	None	**35%**
0	1	0	1	1	280.00	93.33	None	**40%**
0	1	1	0	0	102.00	68.00	None	**2%**
0	1	1	0	1	136.00	68.00	None	
0	1	1	1	0	170.00	68.00	None	
0	1	1	1	1	204.00	68.00	None	
1	0	0	0	0	210.00	70.00	-0.5%	**5%**
1	0	0	0	1	220.00	73.33	-0.5%	**10%**
1	0	0	1	0	230.00	76.67	-0.5%	**15%**
1	0	0	1	1	240.00	80.00	-0.5%	**20%**
1	0	1	0	0	100.00	66.67	-0.5%	**0%**
1	0	1	0	1	133.33	66.67	-0.5%	
1	0	1	1	0	166.67	66.67	-0.5%	
1	0	1	1	1	200.00	66.67	-0.5%	
1	1	0	0	0	250.00	83.33	-0.5%	**25%**
1	1	0	0	1	260.00	86.67	-0.5%	**30%**
1	1	0	1	0	270.00	90.00	-0.5%	**35%**
1	1	0	1	1	280.00	93.33	-0.5%	**40%**
1	1	1	0	0	102.00	68.00	-0.5%	**2%**
1	1	1	0	1	136.00	68.00	-0.5%	
1	1	1	1	0	170.00	68.00	-0.5%	
1	1	1	1	1	204.00	68.00	-0.5%	

Table2: SRC Frequency Selection Table

Byte 0 Bit 5 SRC SS_EN	Byte 5 Bit3 SRC FS3	Byte 5 Bit2 SRC FS2	Byte 5 Bit1 SRC FS1	Byte 5 Bit0 SRC FS0	SRC (MHz)	Spread %	SRC OverClock %
0	0	0	0	0	100.00	0	0%
0	0	0	0	1	101.00	0	1%
0	0	0	1	0	102.00	0	2%
0	0	0	1	1	103.00	0	3%
0	0	1	0	0	104.00	0	4%
0	0	1	0	1	105.00	0	5%
0	0	1	1	0	106.00	0	6%
0	0	1	1	1	107.00	0	7%
0	1	0	0	0	100.00	0	0%
0	1	0	0	1	101.00	0	1%
0	1	0	1	0	102.00	0	2%
0	1	0	1	1	103.00	0	3%
0	1	1	0	0	104.00	0	4%
0	1	1	0	1	105.00	0	5%
0	1	1	1	0	106.00	0	6%
0	1	1	1	1	107.00	0	7%
1	0	0	0	0	100.00	-0.25%	0%
1	0	0	0	1	101.00	-0.25%	1%
1	0	0	1	0	102.00	-0.25%	2%
1	0	0	1	1	103.00	-0.25%	3%
1	0	1	0	0	104.00	-0.25%	4%
1	0	1	0	1	105.00	-0.25%	5%
1	0	1	1	0	106.00	-0.25%	6%
1	0	1	1	1	107.00	-0.25%	7%
1	1	0	0	0	100.00	-0.5%	0%
1	1	0	0	1	101.00	-0.5%	1%
1	1	0	1	0	102.00	-0.5%	2%
1	1	0	1	1	103.00	-0.5%	3%
1	1	1	0	0	104.00	-0.5%	4%
1	1	1	0	1	105.00	-0.5%	5%
1	1	1	1	0	106.00	-0.5%	6%
1	1	1	1	1	107.00	-0.5%	7%

Table3: ATIG Frequency Selection Table

Byte 0	Byte 9				ATIG (MHz)	Spread %	ATIG OverClock %
Bit 6	Bit4	Bit3	Bit1	Bit0			
ATIG SS_EN	ATIG FS3	ATIG FS2	ATIG FS1	ATIG FS0			
0	0	0	0	0	100.00	0	0%
0	0	0	0	1	105.00	0	5%
0	0	0	1	0	110.00	0	10%
0	0	0	1	1	115.00	0	15%
0	0	1	0	0	120.00	0	20%
0	0	1	0	1	125.00	0	25%
0	0	1	1	0	130.00	0	30%
0	0	1	1	1	135.00	0	35%
0	1	0	0	0	100.00	0	0%
0	1	0	0	1	105.00	0	5%
0	1	0	1	0	110.00	0	10%
0	1	0	1	1	115.00	0	15%
0	1	1	0	0	120.00	0	20%
0	1	1	0	1	125.00	0	25%
0	1	1	1	0	130.00	0	30%
0	1	1	1	1	135.00	0	35%
1	0	0	0	0	100.00	-0.25%	0%
1	0	0	0	1	105.00	-0.25%	5%
1	0	0	1	0	110.00	-0.25%	10%
1	0	0	1	1	115.00	-0.25%	15%
1	0	1	0	0	120.00	-0.25%	20%
1	0	1	0	1	125.00	-0.25%	25%
1	0	1	1	0	130.00	-0.25%	30%
1	0	1	1	1	135.00	-0.25%	35%
1	1	0	0	0	100.00	-0.5%	0%
1	1	0	0	1	105.00	-0.5%	5%
1	1	0	1	0	110.00	-0.5%	10%
1	1	0	1	1	115.00	-0.5%	15%
1	1	1	0	0	120.00	-0.5%	20%
1	1	1	0	1	125.00	-0.5%	25%
1	1	1	1	0	130.00	-0.5%	30%
1	1	1	1	1	135.00	-0.5%	35%

Table 4: CPU Divider Ratios

B19b(7:4)	Divider (3:2)								
Divider (1:0)	**Bit**	00		01		10		11	**MSB**
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	15	0111	30	1011	60	1111	120
	LSB	Address	Div	Address		Address	Div	Address	Div

Table 5: HTT Divider Ratios

B20b(3:0)	Divider (3:2)								
Divider (1:0)	**Bit**	00		01		10		11	**MSB**
	00	0000	4	0100	8	1000	16	1100	32
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	15	0111	30	1011	60	1111	120
	LSB	Address	Div	Address		Address	Div	Address	Div

Table 6: ATIG Divider Ratios

B19b(3:0)	Divider (3:2)								
Divider (1:0)	**Bit**	00		01		10		11	**MSB**
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	7	0111	14	1011	28	1111	56
	LSB	Address	Div	Address		Address	Div	Address	Div

General SMBus serial interface information for the ICS951464

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 $_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X$_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2$_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3$_{(H)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Spread Spectrum Enable and CPU Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Latched Input or SMBus Frequency Select	RW	Latched Inputs	SMBus	0
Bit 6	-	ATIG SS_EN	ATIG Spread Spectrum Enable	RW	Disable	Enable	0
Bit 5	-	SRC SS_EN	SRC Spread Spectrum Enable	RW	Disable	Enable	0
Bit 4	-	CPU SS_EN	CPU Spread Spectrum Enable	RW	Disable	Enable	0
Bit 3	-	CPU FS3	CPU Freq Select Bit 3	RW	See Table 1: CPU Frequency Selection Table		0
Bit 2	-	CPU FS2	CPU Freq Select Bit 2	RW			Latch
Bit 1	-	CPU FS1	CPU Freq Select Bit 1	RW			Latch
Bit 0	-	CPU FS0	CPU Freq Select Bit 0	RW			Latch

Note: Each Spread Spectrum Enable bit is independent from the other.
Bit(6:4) must all set to "1" in order to enable spread for CPU, SRC and ATIG clocks.

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	7	48MHz_1	48MHz_1 Output Enable	RW	Disable	Enable	1
Bit 6	6	48MHz_0	48MHz_0 Output Enable	RW	Disable	Enable	1
Bit 5	54	REF2	REF2 Output Enable	RW	Disable	Enable	1
Bit 4	55	REF1	REF1 Output Enable	RW	Disable	Enable	1
Bit 3	56	REF0	REF0 Output Enable	RW	Disable	Enable	1
Bit 2	51	HTTCLK0	HTTCLK0 Output Enable	RW	Disable	Enable	1
Bit 1	44,43	CPUCLK1	CPUCLK1 Output Enable	RW	Disable	Enable	1
Bit 0	48,47	CPUCLK0	CPUCLK0 Output Enable	RW	Disable	Enable	1

SMBus Table: ATIGCLK and CLKREQB# Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						1
Bit 6	Reserved						1
Bit 5	31,30	ATIGCLK1	ATIGCLK1 Output Enable	RW	Disable	Enable	1
Bit 4	35,34	ATIGCLK0	ATIGCLK0 Output Enable	RW	Disable	Enable	1
Bit 3	20,21	REQBSRC4	CLKREQB# Controls SRC4	RW	Does not control	Controls	0
Bit 2	Reserved						0
Bit 1	24,25	REQBSRC2	CLKREQB# Controls SRC2	RW	Does not control	Controls	0
Bit 0	Reserved						0

SMBus Table: SRCCLK Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	12,13	SRCCLK7	Master Output control. Enables or disables output, regardless of CLKREQ# inputs.	RW	Disable	Enable	1
Bit 6	16,17	SRCCLK6		RW	Disable	Enable	1
Bit 5	18,19	SRCCLK5		RW	Disable	Enable	1
Bit 4	20,21	SRCCLK4		RW	Disable	Enable	1
Bit 3	Reserved			Reserved			1
Bit 2	24,25	SRCCLK2		RW	Disable	Enable	1
Bit 1	Reserved			Reserved			1
Bit 0	39,38	SRCCLK0		RW	Disable	Enable	1

SMBus Table: CLKREQA# and CLKREQC# Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	12,13	REQASRC7	CLKREQA# Controls SRC7	RW	Does not control	Controls	0
Bit 6	16,17	REQASRC6	CLKREQA# Controls SRC6	RW	Does not control	Controls	0
Bit 5	18,19	REQASRC5	CLKREQA# Controls SRC5	RW	Does not control	Controls	0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	31,30	REQCATIG1	CLKREQC# Controls ATIG1	RW	Does not control	Controls	0
Bit 1	35,34	REQCATIG0	CLKREQC# Controls ATIG0	RW	Does not control	Controls	0
Bit 0	39,38	REQCSRC0	CLKREQC# Controls SRC0	RW	Does not control	Controls	0

SMBus Table: CPU Stop Control and SRC Frequency Select Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	SRC, ATIG	Differential Output Disable Mode	Hi-Z or Driven when disable	RW	Driven	Hi-Z	0
Bit 3	-	SRC FS3	SRC Freq Select Bit 3	RW	See Table 2: SRC Frequency Selection Table		0
Bit 2	-	SRC FS2	SRC Freq Select Bit 2	RW			0
Bit 1	-	SRC FS1	SRC Freq Select Bit 1	RW			0
Bit 0	-	SRC FS0	SRC Freq Select Bit 0	RW			0

SMBus Table: Device ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID7 (MSB)	DEVICE ID	R	-	-	0
Bit 6	-	Device ID6		R	-	-	1
Bit 5	-	Device ID5		R	-	-	1
Bit 4	-	Device ID4		R	-	-	0
Bit 3	-	Device ID3		R	-	-	0
Bit 2	-	Device ID2		R	-	-	0
Bit 1	-	Device ID1		R	-	-	1
Bit 0	-	Device ID0 (LSB)		R	-	-	0

SMBus Table: Revision and Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	x
Bit 6	-	RID2		R	-	-	x
Bit 5	-	RID1		R	-	-	x
Bit 4	-	RID0		R	-	-	x
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will congiure how many bytes will be read back, default is 9 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			1

SMBus Table: REF2, 48MHz Output Strength Control and ATIG Frequency Select Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	54	REF2Str	REF2 Strength Control	RW	1X	2X	1
Bit 6	7	48MHz_1Str	48MHz_1 Strength Control	RW	1X	2X	1
Bit 5	6	48MHz_0Str	48MHz_0 Strength Control	RW	1X	2X	1
Bit 4	Reserved						0
Bit 3	-	ATIG FS3	ATIG Freq Select Bit 3	RW	See Table 3: ATIG Frequency Selection Table		0
Bit 2	-	ATIG FS2	ATIG Freq Select Bit 2	RW			0
Bit 1	-	ATIG FS1	ATIG Freq Select Bit 1	RW			0
Bit 0	-	ATIG FS0	ATIG Freq Select Bit 0	RW			0

SMBus Table: PLLs M/N Programming Enable and REF1, REF0 Output Strength Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLLs M/N Programming Enable	RW	Disable	Enable	0
Bit 6	55	REF1Str	REF1 Strength Control	RW	1X	2X	1
Bit 5	56	REF0Str	REF0 Strength Control	RW	1X	2X	1
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div 9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: ATIG PLL VCO Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: ATIG PLL VCO Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: ATIG PLL Spread Spectrum Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: ATIG PLL Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: CPU and ATIG Divider Ratio Programming Bits Select Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPU_Div3	CPU_Divider Ratio Programming Bits	RW	See Table 4: CPU Divider Ratios		X
Bit 6	-	CPU_Div2		RW			X
Bit 5	-	CPU_Div1		RW			X
Bit 4	-	CPU_Div0		RW			X
Bit 3	-	ATIG_Div3	ATIG_Divider Ratio Programming Bits	RW	See Table 5: ATIG Divider Ratios		X
Bit 2	-	ATIG_Div2		RW			X
Bit 1	-	ATIG_Div1		RW			X
Bit 0	-	ATIG_Div0		RW			X

SMBus Table: HTT Divider Ratio Programming Bits Select Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	-	HTT_Div3	HTT_Divider Ratio Programming Bits	RW	See Table 6: HTT Divider Ratios		X
Bit 2	-	HTT_Div2		RW			X
Bit 1	-	HTT_Div1		RW			X
Bit 0	-	HTT_Div0		RW			X

Absolute Max

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDD_A	-			V_{DD} + 0.5V	V	1
3.3V Logic Input Supply Voltage	VDD_In	-	GND - 0.5		V_{DD} + 0.5V	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion			300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4			mA	1
SMBCLK/SMBDAT Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SMBCLK/SMBDAT Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - K8 Push Pull Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =AMD64 Processor Test Load

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Rate	$\delta V/\delta t$	Measured at the AMD64 processor's test load. 0 V +/- 400 mV (differential measurement)	2		10	V/ns	1
Falling Edge Rate	$\delta V/\delta t$		2		10	V/ns	1
Differential Voltage	V_{DIFF}	Measured at the AMD64 processor's test load. (single-ended measurement)	0.4	1.25	2.3	V	1
Change in V_{DIFF_DC} Magnitude	ΔV_{DIFF}		-150		150	mV	1
Common Mode Voltage	V_{CM}		1.05	1.25	1.45	V	1
Change in Common Mode Voltage	ΔV_{CM}		-200		200	mV	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom. Maximum difference of cycle time between 2 adjacent cycles.	0	50	85	ps	1
Jitter, Accumulated	t_{ja}	Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50 ps, Sample Duration = 10 µs	-1000		1000		1,2,3
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		53	%	1
Output Impedance	R_{ON}	Average value during switching transition. Used for determining series termination value.	15	35	55	Ω	1
Group Skew	$t_{src-skew}$	Measurement from differential wavefrom			50	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All accumulated jitter specifications are guaranteed assuming that REF is at 14.31818MHz

[3] Spread Spectrum is off

Electrical Characteristics - HTTCLK Clock

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
PCI33 Clock period	T_{period}	33.33MHz output nominal	29.9910		30.0090	ns	2
		33.33MHz output spread	29.9910		30.1598	ns	2
HTT66 Clock period	T_{period}	66.67MHz output nominal	14.9955		15.0045	ns	2
		66.67MHz output spread	14.9955		15.0799	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@ MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Edge Rate	$\delta V/\delta t$	Rising edge rate	1		4	V/ns	1
Edge Rate	$\delta V/\delta t$	Falling edge rate	1		4	V/ns	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V			180	ps	1

*T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 30 pF (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that REF is at 14.31818MHz

Electrical Characteristics - SRC/ATIG 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300			mV	1
Crossing Voltage (abs)	Vx(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabsmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V			125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V			125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		55	%	1
Skew	t_{sk3}	V_T = 50%			100	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom			85	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

Electrical Characteristics - USB - 48MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	48.00MHz output nominal	20.8229		20.8344	ns	2
Clock Low Time	T_{low}	Measure from < 0.6V	9.3750		11.4580	ns	2
Clock High Time	T_{high}	Measure from > 2.0V	9.3750		11.4580	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_{r_USB}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		1.5	ns	1
Fall Time	t_{f_USB}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		1.5	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45		55	%	1
Group Skew	t_{skew}	V_T = 1.5 V			100	ps	1
Jitter, Cycle to cycle	$t_{jcyc\text{-}cyc}$	V_T = 1.5 V			130	ps	1,2

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]ICS recommended and/or chipset vendor layout guidelines must be followed to meet this specification

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100		100	ppm	1,2
Clock period	T_{period}	14.318MHz output nominal	69.8270		69.8550	ns	2
Clock Low Time	T_{low}	Measure from < 0.6V	30.9290		37.9130	ns	2
Clock High Time	T_{high}	Measure from > 2.0V	30.9290		37.9130	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V, V_{OH}@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I_{OL}	V_{OL} @MIN = 1.95 V, V_{OL} @MAX = 0.4 V	29		27	mA	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			1.5	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			1.5	ns	1
Skew	t_{sk1}	V_T = 1.5 V			100	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	44	53	56	%	1
Jitter	$t_{jcyc\text{-}cyc}$	V_T = 1.5 V		200	300	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs = 22Ω (unless otherwise specified)

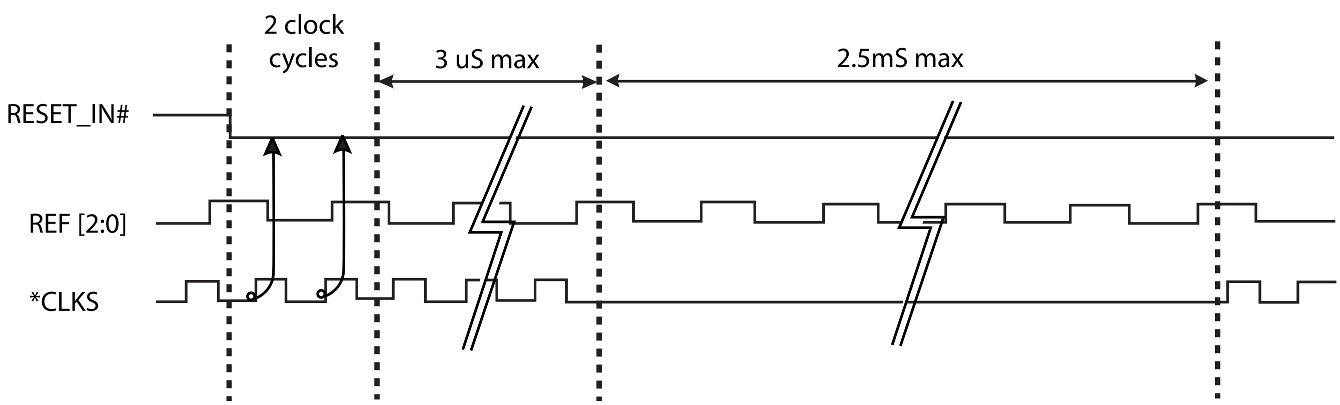
[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

RESET_IN# - Assertion (transition from '1' to '0')

Asserting RESET_IN pin stops all the outputs including CPU, SRC, ATIG, PCI and USB with the REF[2:0] running. The pin is a Schmitt trigger input with debouncing. After it is triggered, REF clocks will wait for two clock cycle to ensure the RESET_IN is asserted. Then, it will take 3uS for the clocks to stop without glitches. The clock chip will be power down and re-power up, and SMBus will be reloaded. It will take no more than 2.5mS for the clocks to come out with correct frequencies and no glitches.

**** Deassertion of RESET_IN# (transition from '0' to '1') has NO effect on the clocks.**



SRC Routing Information

SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch	2, 3
L2 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	2, 3
L3 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	2, 3
Rs	33	ohm	2, 3
Rt	49.9	ohm	2, 3

Down Device Differential Routing	Dimension or Value	Unit	Figure
L4 length, Route as coupled **microstrip** 100 ohm differential trace.	2 min to 16 max	inch	2
L4 length, Route as coupled **stripline** 100 ohm differential trace.	1.8 min to 14.4 max	inch	2

Differential Routing to PCI Express Connector	Dimension or Value	Unit	Figure
L4 length, Route as coupled **microstrip** 100 ohm differential trace.	0.25 to 14 max	inch	3
L4 length, Route as coupled **stripline** 100 ohm differential trace.	0.225 min to 12.6 max	inch	3

Fig.1

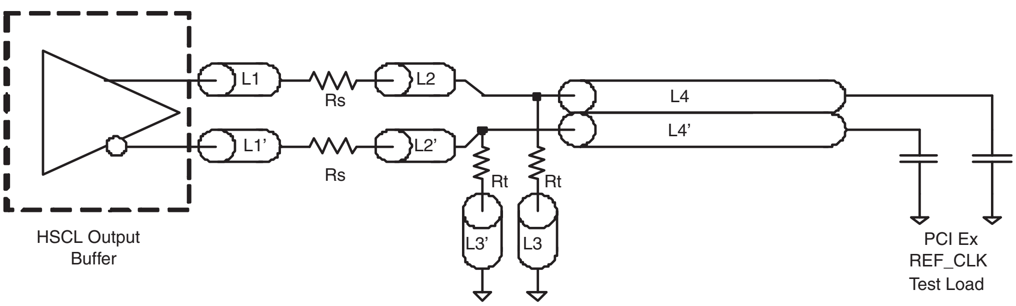


Fig.2

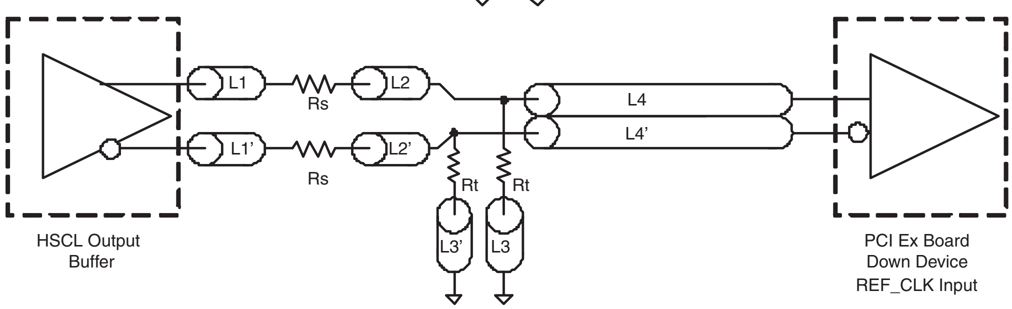
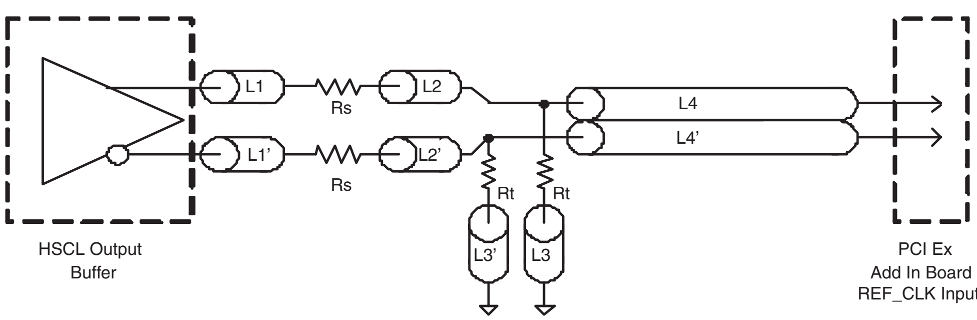


Fig.3



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS951464** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period. Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

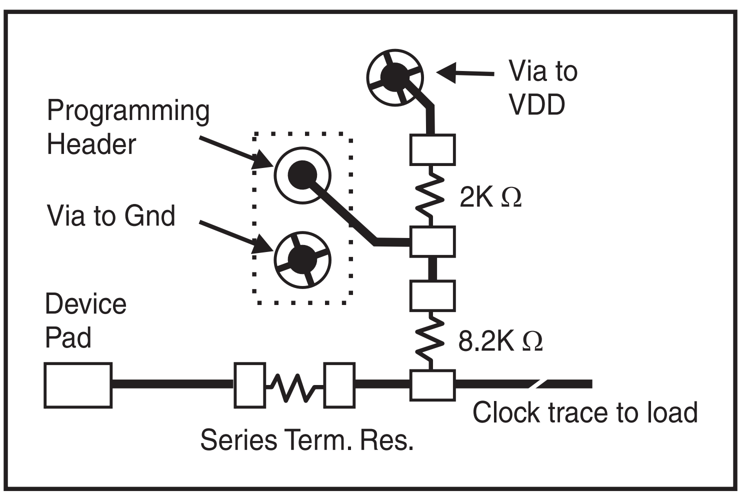
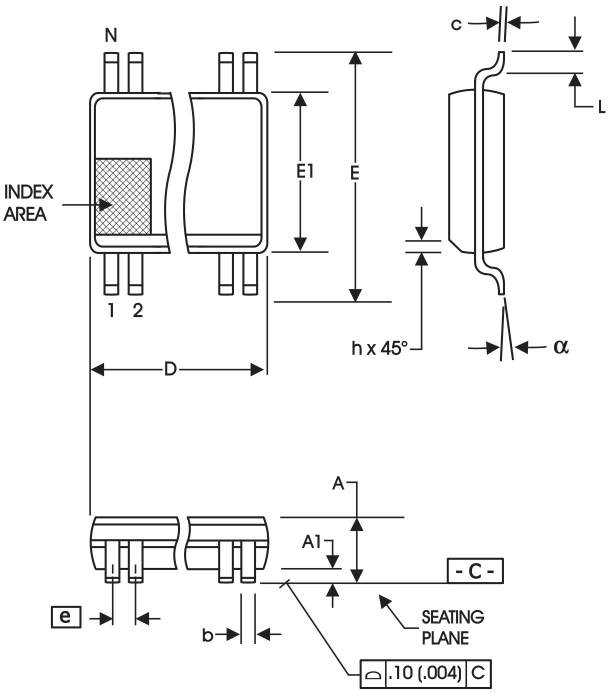


Fig. 1



56-Lead, 300 mil Body, 25 mil, SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

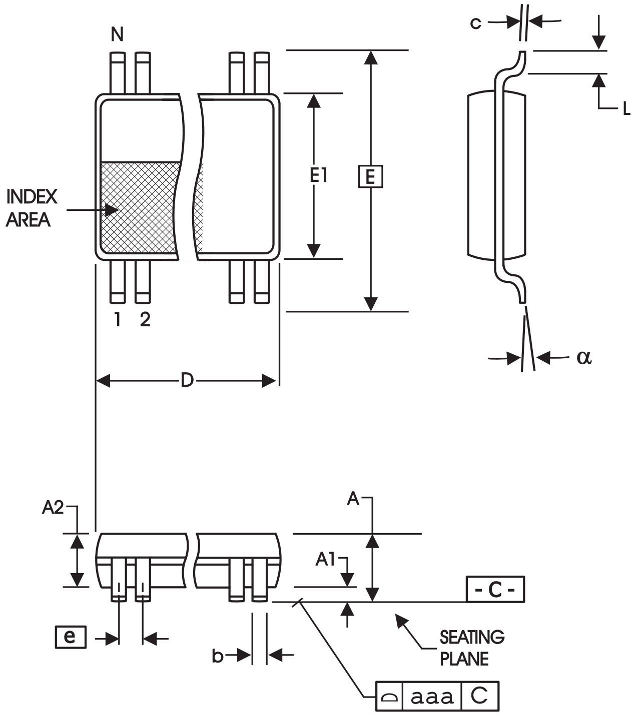
Ordering Information

951464yFLFT

Example:

XXXX y F LF T

- **T** — **Designation for tape and reel packaging**
- **LF** — **Lead Free, RoHS Compliant**
- **F** — **Package Type**
  F = SSOP
- **y** — **Revision Designator** (will not correlate with datasheet revision)
- **XXXX** — **Device Type (consists of 3 to 7 digit numbers)**



56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

951464yGLFT

Example:

XXXX y G LF T

- **T** — **Designation for tape and reel packaging**
- **LF** — **Lead Free, RoHS Compliant**
- **G** — **Package Type**
  G = TSSOP
- **y** — **Revision Designator** (will not correlate with datasheet revision)
- **XXXX** — **Device Type (consists of 3 to 7 digit numbers)**

Revision History

Rev.	Issue Date	Description	Page #
A	4/9/2008	Going to Release.	-
B	9/17/2009	Updated Power Group table.	4

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