Programmable Timing Control Hub™ for P4™ processor

Recommended Application:

SIS 645/650 style chipsets.

Output Features:

- 2 - Pairs of differential CPUCLKs (differential current mode)
- 1 - SDRAM @ 3.3V
- 8 - PCI @3.3V
- 2 - AGP @ 3.3V
- 2 - ZCLKs @ 3.3V
- 1- 48MHz, @3.3V fixed.
- 1- 24/48MHz, @3.3V selectable by I^2C (Default is 24MHz)
- 3- REF @3.3V, 14.318MHz.

Features/Benefits:

- Programmable output frequency, divider ratios, output rise/falltime, output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- For PC133 SDRAM system use the ICS9179-06 as the memory buffer.
- For DDR SDRAM system use the ICS93705 or ICS93722 as the memory buffer.
- Uses external 14.318MHz crystal.

Key Specifications:

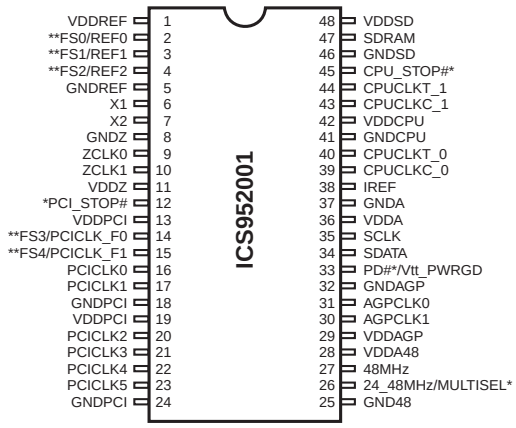
- PCI - PCI output skew: < 500ps
- CPU - SDRAM output skew: < 1ns
- AGP - AGP output skew: <150ps

Functionality

Bit 2	Bit 7	Bit 6	Bit 5	Bit 4	CPU	SDRAM	ZCLK	AGP
FS4	FS3	FS2	FS1	FS0	(MHz)	(MHz)	(MHz)	(MHz)
0	0	0	0	0	66.67	66.67	66.67	66.67
0	0	0	0	1	100.00	100.00	66.67	66.67
0	0	0	1	0	100.00	200.00	66.67	66.67
0	0	0	1	1	100.00	133.33	66.67	66.67
0	0	1	0	0	100.00	150.00	60.00	60.00
0	0	1	0	1	100.00	125.00	62.50	62.50
0	0	1	1	0	100.00	160.00	66.67	66.67
0	0	1	1	1	100.00	133.33	80.00	66.67
0	1	0	0	0	100.00	200.00	66.67	66.67
0	1	0	0	1	100.00	166.67	62.50	62.50
0	1	0	1	0	100.00	166.67	71.43	83.33
0	1	0	1	1	80.00	133.33	66.67	66.67
0	1	1	0	0	80.00	133.33	66.67	66.67
0	1	1	0	1	95.00	95.00	63.33	63.33
0	1	1	1	0	95.00	126.67	63.33	63.33
0	1	1	1	1	66.67	66.67	50.00	50.00

Note: For additional margin testing frequencies, refer to Byte 4

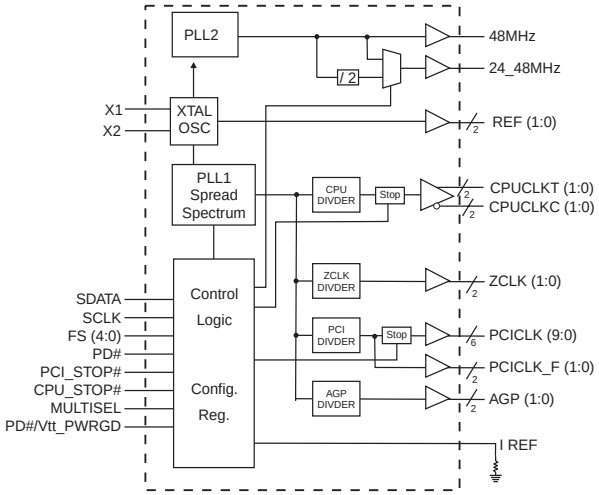
Pin Configuration



48-Pin 300-mil SSOP and TSSOP

* These inputs have a 120K pull up to VDD.
** These inputs have a 120K pull down to GND.

Block Diagram



Power Groups

VDDCPU = CPU
VDDPCI = PCICLK_F, PCICLK
VDDSD = SDRAM
AVDD48 = 48MHz, 24MHz, fixed PLL
AVDD = Analog Core PLL
VDDAGP= AGP
VDDREF = Xtal, REF
VDDZ = ZCLK

General Description

The **ICS952001** is a two chip clock solution for desktop designs using SIS 645/650 style chipsets. When used with a zero delay buffer such as the ICS9179-06 for PC133 or the ICS93705 for DDR applications it provides all the necessary clocks signals for such a system.

The **ICS952001** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology and a reset feature to provide a safe setting under unstable system conditions. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Pin Description

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 11, 13, 19, 29, 42, 48	VDD	PWR	Power supply for 3.3V
2	FS0	IN	Frequency select pin.
	REF0	OUT	14.318 MHz reference clock.
3	FS1	IN	Frequency select pin.
	REF1	OUT	14.318 MHz reference clock.
4	FS2	IN	Frequency select pin.
	REF2	OUT	14.318 MHz reference clock.
5, 8, 18, 24, 25, 32, 37, 41, 46	GND	PWR	Ground pin for 3V outputs.
6	X1	IN	Crystal input,nominally 14.318MHz.
7	X2	OUT	Crystal output, nominally 14.318MHz.
10, 9	ZCLK(1:0)	OUT	Hyperzip clock outputs.
12	PCI_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when MODE pin is in Mobile mode
14	FS3	IN	Frequency select pin.
	PCICLK_F0	OUT	PCI clock output, not affected by PCI_STOP#
15	FS4	IN	Frequency select pin.
	PCICLK_F1	OUT	PCI clock output, not affected by PCI_STOP#
23, 22, 21, 20, 17, 16	PCICLK (5:0)	OUT	PCI clock outputs.
26	MULTISEL	IN	3.3V LVTTL input for selecting the current multiplier for CPU outputs.
	24_48MHz	OUT	Clock output for super I/O/USB default is 24MHz
27	48MHz	OUT	48MHz output clock
28, 36	AVDD	PWR	Analog power supply 3.3V
30, 31	AGPCLK (1:0)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
33	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
	Vtt_PWRGD	IN	This pin acts as a dual function input pin for Vtt_PWRGD and PD# signal. When Vtt_PWRGD goes high the frequency select will be latched at power on thereafter the pin is an asynchronous active low power down pin.
34	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
35	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
38	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
43, 39	CPUCLKC (1:0)	OUT	"Complementary" clocks of differential pair CPU outputs. These clocks are 180° out of phase with SDRAM clocks. These open drain outputs need an external 1.5V pull-up.
44, 40	CPUCLKT (1:0)	OUT	"True" clocks of differential pair CPU outputs. These clocks are in phase with SDRAM clocks. These open drain outputs need an external 1.5V pull up.
45	CPU_STOP#	IN	Stops all CPUCLKs clocks at logic 0 level, when MODE pin is in Mobile mode
47	SDRAM	OUT	SDRAM clock output.

CPUCLK Swing Select Functions

MULTSEL0	Byte 23 Bit 7	Board Target Trace/Term Z	Reference R, Iref= Vdd/(3*Rr)	Output Current	Voh @ Z, Iref=2.32mA
0	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.71V @ 60
0	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
0	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
1	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.85V /2 60
1	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.71V @ 50
1	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.60 @ 20
0	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.5V @ 20
1	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.90V @ 30
1	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.75V @ 20
1	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	0.84V @ 20

General I²C serial interface information for the ICS952001

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	○		
	○		○
	○		○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			○
	○		○
	○		○
	○		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

*See notes on the following page.

Serial Configuration Command Bitmap

Bytes 0-3: Are reserved for external clock buffer.

Byte4: Functionality and Frequency Select Register (default = 0)

Bit	Description											PWD
Bit 2 Bit 7:4	Bit 2	Bit 7	Bit 6	Bit 5	Bit 4							00000 Note1
	FS4	FS3	FS2	FS1	FS0	CPU	SDRAM	ZCLK	AGP	PCI	Spread Precentage	
	0	0	0	0	0	66.67	66.67	66.67	66.67	33.33	0 to -0.5% Down Spread	
	0	0	0	0	1	100.00	100.00	66.67	66.67	33.33	0 to -0.5% Down Spread	
	0	0	0	1	0	100.00	200.00	66.67	66.67	33.33	0 to -0.5% Down Spread	
	0	0	0	1	1	100.00	133.33	66.67	66.67	33.33	0 to -0.5% Down Spread	
	0	0	1	0	0	100.00	150.00	60.00	60.00	30.00	+/- 0.25% Center Spread	
	0	0	1	0	1	100.00	125.00	62.50	62.50	31.25	+/- 0.25% Center Spread	
	0	0	1	1	0	100.00	160.00	66.67	66.67	33.33	+/- 0.25% Center Spread	
	0	0	1	1	1	100.00	133.33	80.00	66.67	33.33	0 to -0.5% Down Spread	
	0	1	0	0	0	100.00	200.00	66.67	66.67	33.33	+/- 0.25% Center Spread	
	0	1	0	0	1	100.00	166.67	62.50	62.50	31.25	0 to -0.5% Down Spread	
	0	1	0	1	0	100.00	166.67	71.43	83.33	41.67	+/- 0.25% Center Spread	
	0	1	0	1	1	80.00	133.33	66.67	66.67	33.33	+/- 0.25% Center Spread	
	0	1	1	0	0	80.00	133.33	66.67	66.67	33.33	+/- 0.25% Center Spread	
	0	1	1	0	1	95.00	95.00	63.33	63.33	31.67	+/- 0.25% Center Spread	
	0	1	1	1	0	95.00	126.67	63.33	63.33	31.67	+/- 0.25% Center Spread	
	0	1	1	1	1	66.67	66.67	50.00	50.00	25.00	+/- 0.25% Center Spread	
	1	0	0	0	0	105.00	140.00	70.00	70.00	35.00	+/- 0.25% Center Spread	
	1	0	0	0	1	100.90	100.90	67.27	67.27	33.63	+/- 0.25% Center Spread	
	1	0	0	1	0	108.00	144.00	72.00	72.00	36.00	+/- 0.25% Center Spread	
	1	0	0	1	1	100.90	134.53	67.27	67.27	33.63	+/- 0.25% Center Spread	
	1	0	1	0	0	112.00	149.33	74.67	74.67	37.33	+/- 0.25% Center Spread	
	1	0	1	0	1	133.33	100.00	66.67	66.67	33.33	0 to -0.5% Down Spread	
	1	0	1	1	0	133.33	133.33	66.67	66.67	33.33	+/- 0.25% Center Spread	
	1	0	1	1	1	133.33	166.67	66.67	66.67	33.33	+/- 0.25% Center Spread	
	1	1	0	0	0	100.00	133.00	80.00	66.67	33.33	+/- 0.25% Center Spread	
	1	1	0	0	1	100.00	100.00	80.00	66.67	33.33	+/- 0.25% Center Spread	
	1	1	0	1	0	100.00	166.67	83.33	62.50	31.25	+/- 0.25% Center Spread	
	1	1	0	1	1	133.33	160.00	80.00	66.67	33.33	+/- 0.25% Center Spread	
	1	1	1	0	0	100.00	133.00	100.00	66.67	33.33	+/- 0.25% Center Spread	
	1	1	1	0	1	100.00	100.00	100.00	66.67	33.33	+/- 0.25% Center Spread	
	1	1	1	1	0	100.00	166.67	100.00	62.50	31.25	+/- 0.25% Center Spread	
	1	1	1	1	1	133.33	160.00	100.00	66.67	33.33	+/- 0.25% Center Spread	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit , 2 7:4											0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled											0
Bit 0	0 - Running 1- Tristate all outputs											0

Note1:
Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Note: PWD = Power-Up Default

Byte 5: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	30	1	AGPCLK1
Bit 6	31	1	AGPCLK1
Bit 5	26	0	SEL24_48MHz (1=24MHz, 0=48MHz)
Bit 4	15	X	FS4 Read Back
Bit 3	14	X	FS3 Read Back
Bit 2	4	X	FS2 Read Back
Bit 1	3	X	FS1 Read Back
Bit 0	2	X	FS0 Read Back

Byte 6: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	10	1	ZCLK1
Bit 6	9	1	ZCLK0
Bit 5	14	0	PCICLK_F0 stop control 0 = Free Running; 1 = Stop
Bit 4	15	0	PCICLK_F1 stop control 0 = Free Running; 1 = Stop
Bit 3	40, 39	1	CPUCLKT/C0 stop control 0 = Free Running; 1 = Stop
Bit 2	44, 43	1	CPUCLKT/C1 stop control 0 = Free Running; 1 = Stop
Bit 1	39, 40	1	CPUCLKT/C0 output control
Bit 0	43, 44	1	CPUCLKT/C1 output control

Byte 7: Output Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	15	1	PCICLK_F1
Bit 6	14	1	PCICLK_F0
Bit 5	23	1	PCICLK5
Bit 4	22	1	PCICLK4
Bit 3	21	1	PCICLK3
Bit 2	20	1	PCICLK2
Bit 1	17	1	PCICLK1
Bit 0	16	1	PCICLK0

Byte 8: Byte Count Read Back Register

Bit	Name	PWD	Description
Bit 7	Byte7	0	Note: Writing to this register will configure byte count and how many bytes will be read back, default is $0F_H$ = 15 bytes.
Bit 6	Byte6	0	
Bit 5	Byte5	0	
Bit 4	Byte4	0	
Bit 3	Byte3	1	
Bit 2	Byte2	1	
Bit 1	Byte1	1	
Bit 0	Byte0	1	

Byte 9: Watchdog Timer Count Register

Bit	Name	PWD	Description
Bit 7	WD7	0	The decimal representation of these 8 bits correspond to X • 290ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16 • 290ms = 4.6 seconds.
Bit 6	WD6	0	
Bit 5	WD5	0	
Bit 4	WD4	1	
Bit 3	WD3	0	
Bit 2	WD2	0	
Bit 1	WD1	0	
Bit 0	WD0	0	

Byte 10: Programming Enable bit 8 Watchdog Control Register

Bit	Name	PWD	Description
Bit 7	Program Enable	0	Programming Enable bit 0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all I^2C programing.
Bit 6	WD Enable	0	Watchdog Enable bit
Bit 5	WD Alarm	0	Watchdog Alarm Status 0 = normal 1= alarm status
Bit 4	SF4	0	Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corrsponding to Byte 0 Bit 2, 7:4 table
Bit 3	SF3	0	
Bit 2	SF2	0	
Bit 1	SF1	0	
Bit 0	SF0	1	

Byte 11: VCO Frequency M Divider (Reference divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 8	X	N divider bit 8
Bit 6	Mdiv 6	X	The decimal respresentation of Mdiv (6:0) corresposd to the reference divider value. Default at power up is equal to the latched inputs selection.
Bit 5	Mdiv 5	X	
Bit 4	Mdiv 4	X	
Bit 3	Mdiv 3	X	
Bit 2	Mdiv 2	X	
Bit 1	Mdiv 1	X	
Bit 0	Mdiv 0	X	

Byte 12: VCO Frequency N Divider (VCO divider) Control Register

Bit	Name	PWD	Description
Bit 7	Ndiv 7	X	The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selecton. Notice Ndiv 8 is located in Byte 11.
Bit 6	Ndiv 6	X	
Bit 5	Ndiv 5	X	
Bit 4	Ndiv 4	X	
Bit 3	Ndiv 3	X	
Bit 2	Ndiv 2	X	
Bit 1	Ndiv 1	X	
Bit 0	Ndiv 0	X	

Byte 13: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	SS 7	X	The Spread Spectrum (12:0) bit will program the spread precentage. Spread precent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use ICS software for spread programming. Default power on is latched FS divider.
Bit 6	SS 6	X	
Bit 5	SS 5	X	
Bit 4	SS 4	X	
Bit 3	SS 3	X	
Bit 2	SS 2	X	
Bit 1	SS 1	X	
Bit 0	SS 0	X	

Byte 14: Spread Spectrum Control Register

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	Reserved
Bit 5	Reserved	X	Reserved
Bit 4	SS 12	X	Spread Spectrum Bit 12
Bit 3	SS 11	X	Spread Spectrum Bit 11
Bit 2	SS 10	X	Spread Spectrum Bit 10
Bit 1	SS 9	X	Spread Spectrum Bit 9
Bit 0	SS 8	X	Spread Spectrum Bit 8

Byte 15: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	SD Div 3	X	SDRAM clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	SD Div 2	X	
Bit 5	SD Div 1	X	
Bit 4	SD Div 0	X	
Bit 3	CPU Div 3	X	CPUCLKT/C clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	CPU Div 2	X	
Bit 1	CPU Div 1	X	
Bit 0	CPU Div 0	X	

Byte 16: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	AGP Div 3	X	AGP clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	AGP Div 2	X	
Bit 5	AGP Div 1	X	
Bit 4	AGP Div 0	X	
Bit 3	ZCLK Div 3	X	ZCLK clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	ZCLK Div 2	X	
Bit 1	ZCLK Div 1	X	
Bit 0	ZCLK Div 0	X	

Byte 17: Output Divider Control Register

Bit	Name	PWD	Description
Bit 7	AGP_INV	0	AGP Phase Inversion bit
Bit 6	ZCLK_INV	0	ZCLK Phase Inversion bit
Bit 5	SD_INV	0	SDRAM Phase Inversion bit
Bit 4	CPU_INV	0	CPUCLK Phase Inversion bit
Bit 3	PCI Div 3	X	PCI clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to table 2. Default at power up is latched FS divider.
Bit 2	PCI Div 2	X	
Bit 1	PCI Div 1	X	
Bit 0	PCI Div 0	X	

Table 1

Div (3:2) / Div (1:0)	00	01	10	11
00	/2	/4	/8	/16
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

Table 2

Div (3:2) / Div (1:0)	00	01	10	11
00	/4	/8	/16	/32
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

Byte 18: Group Skew Control Register

Bit	Name	PWD	Description
Bit 7	CPU_Skew 1	1	These 2 bits delay the CPUCLKT/C (1:0) clocks with respect to all other clocks. 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps
Bit 6	CPU_Skew 0	0	
Bit 5	SD_Skew 1	0	These 2 bits delay the SDRAM with respect to CPUCLK 00 = 0ps 01 = 250ps 10 = 500ps 11 =750ps
Bit 4	SD_Skew 0	1	
Bit 3	(Reserved)	1	(Reserved)
Bit 2	(Reserved)	1	
Bit 1	(Reserved)	1	
Bit 0	(Reserved)	1	

Byte 19: Group Skew Control Register

Bit	Name	PWD	Programmable Delay Stop									
Bit 7	These 4bits control CPU-ZCLK(1:0)	1	0	0	0	0	1.85ns	1	0	0	0	3.05ns
Bit 6		0	0	0	0	1	2.00ns	1	0	0	1	3.20ns
Bit 5		0	0	0	1	0	2.15ns	1	0	1	0	3.35ns
Bit 4		0	0	0	1	1	2.30ns	1	0	1	1	3.50ns
Bit 3	These 4 bits control CPU-AGP(1:0)	1	0	1	0	0	2.45ns	1	1	0	0	3.65ns
Bit 2		0	0	1	0	1	2.60ns	1	1	0	1	3.80ns
Bit 1		0	0	1	1	0	2.75ns	1	1	1	0	3.95ns
Bit 0		0	0	1	1	1	2.90ns	1	1	1	1	4.10ns

Byte 20: Group Skew Control Register

Bit	Name	PWD	Programmable Delay Stop									
Bit 7	These 4bits control CPU-PCICLK_F(1:0)	0	0	0	0	0	1.85ns	1	0	0	0	3.05ns
Bit 6		1	0	0	0	1	2.00ns	1	0	0	1	3.20ns
Bit 5		0	0	0	1	0	2.15ns	1	0	1	0	3.35ns
Bit 4		0	0	0	1	1	2.30ns	1	0	1	1	3.50ns
Bit 3	These 4 bits control CPU-PCICLK(5:0)	0	0	1	0	0	2.45ns	1	1	0	0	3.65ns
Bit 2		1	0	1	0	1	2.60ns	1	1	0	1	3.80ns
Bit 1		0	0	1	1	0	2.75ns	1	1	1	0	3.95ns
Bit 0		0	0	1	1	1	2.90ns	1	1	1	1	4.10ns

Byte 21: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	24/48_Slew	0	24/48 MHz clock slew rate control bits. 01 = strong; 00, 11 = normal; 10 = weak
Bit 6		0	
Bit 5	AGP_Slew	0	AGP clock slew rate control bits. 01 = strong; 00, 11 = normal; 10 = weak
Bit 4		0	
Bit 3	ZCLK_Slew	0	ZCLK clock slew rate control bits. 01 = strong; 00, 11 = normal; 10 = weak
Bit 2		0	
Bit 1	REF_Slew	0	REF clock slew rate control bits. 01 = strong; 00, 11 = normal; 10 = weak
Bit 0		0	

Byte 22: Slew Rate Control Register

Bit	Name	PWD	Description
Bit 7	SDRAM Slew	0	SDRAM clock slew rate control bits. 01 = strong; 00, 11 = normal;10 = weak
Bit 6		0	
Bit 5	(Reserved)	X	(Reserved)
Bit 4		X	
Bit 3	PCICLK_F Slew	0	PCICLK_F clock slew rate control bits. 01 = strong; 00, 11 = normal;10 = weak
Bit 2		0	
Bit 1	PCICLK Slew	0	PCICLK clock slew rate control bits. 01 = strong; 00, 11 = normal;10 = weak
Bit 0		0	

Byte 23: Output Control Register

Bit	Pin#	PWD	Description
Bit 7	-	0	Iref Output Control
Bit 6	-	1	MULITSEL Readback
Bit 5	47	1	SDRAM
Bit 4	27	1	48MHz
Bit 3	26	1	24_48MHz
Bit 2	4	1	REF2
Bit 1	3	1	REF1
Bit 0	2	1	REF0

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C
Case Temperature . . . . . 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%, VDDL=2.5 V± 5%(unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 30 pF; CPU @ 133 MHz			280	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF			25	mA
Input frequency	F_i	V_{DD} = 3.3 V		14.32		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH\ @MIN}$= 1.0V , $V_{OH@\ MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL\ @MIN}$= 1.2V , $V_{OL@\ MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	ns
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25			mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2.0	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2.0	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45.0		55.0	%
Skew Window	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	t_{j1s1}[1]	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24M, 48M, REF

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	V_O = V_{DD}*(0.5)	20		60	Ω
Output Impedance	R_{DSN5}[1]	V_O = V_{DD}*(0.5)	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -14 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 6.0 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	10			mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4.0	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4.0	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45.0		55.0	%
Jitter	t_{j1s5}[1]	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} =V_{DDL} 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}[1]	V_O = V_{DD}*(0.5)	10		20	Ω
Output Impedance	R_{DSN2A}[1]	V_O = V_{DD}*(0.5)	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL2A}	I_{OL} = 19 mA			0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V			-42	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33			mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2.0	ns
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	45		55	%
Jitter[1]	$t_{cyc-cyc}$	V_T = 1.5 V			250.0	ps

[1]Guarenteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period. Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

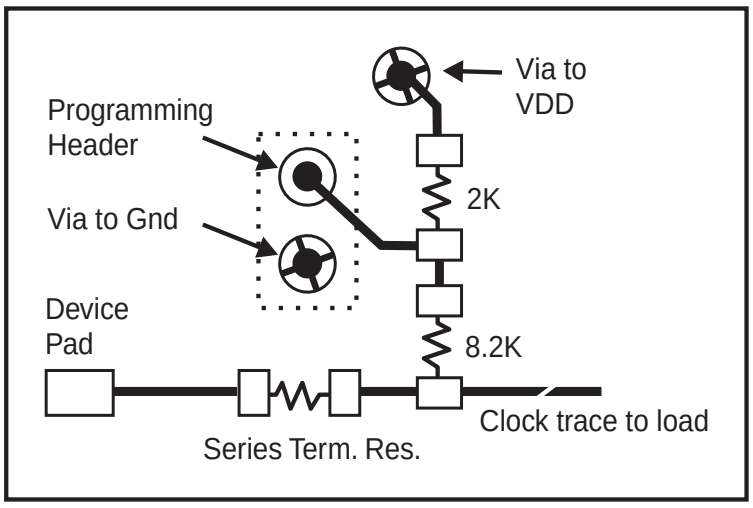
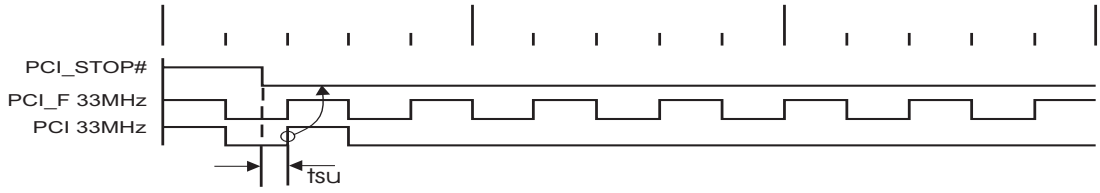


Fig. 1

PCI_STOP# - Assertion (transition from logic "1" to logic "0")

The impact of asserting the PCI_STOP# signal will be the following. All PCI and stoppable PCI_F clocks will latch low in their next high to low transition. The PCI_STOP# setup time tsu is 10 ns, for transitions to be recognized by the next rising edge.

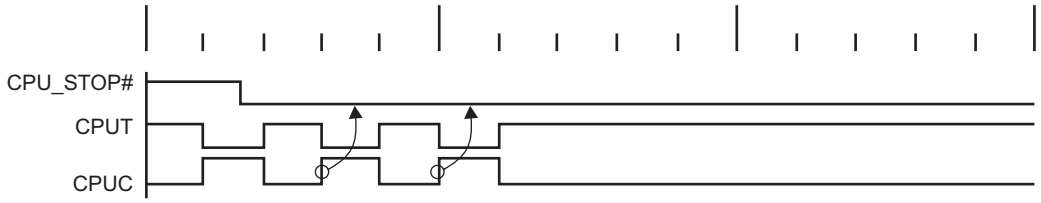
Assertion of PCI_STOP# Waveforms



CPU_STOP# - Assertion (transition from logic "1" to logic "0")

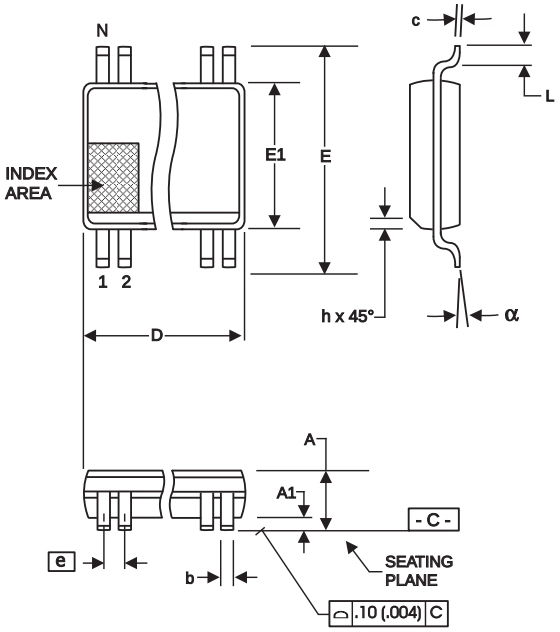
The impact of asserting the CPU_STOP# pin is all CPU outputs that are set in the I^2C configuration to be stoppable via assertion of CPU_STOP# are to be stopped after their next transition following the two CPU clock edge sampling as shown. The final state of the stopped CPU signals is CPUT=High and CPUC=Low. There is to be no change to the output drive current values. The CPUT will be driven high with a current value equal to (MULTSEL0) X (I REF), the CPUC signal will not be driven.

Assertion of CPU_STOP# Waveforms



CPU_STOP# Functionality

CPU_STOP#	CPUT	CPUC
1	Normal	Normal
0	iref * Mult	Float



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

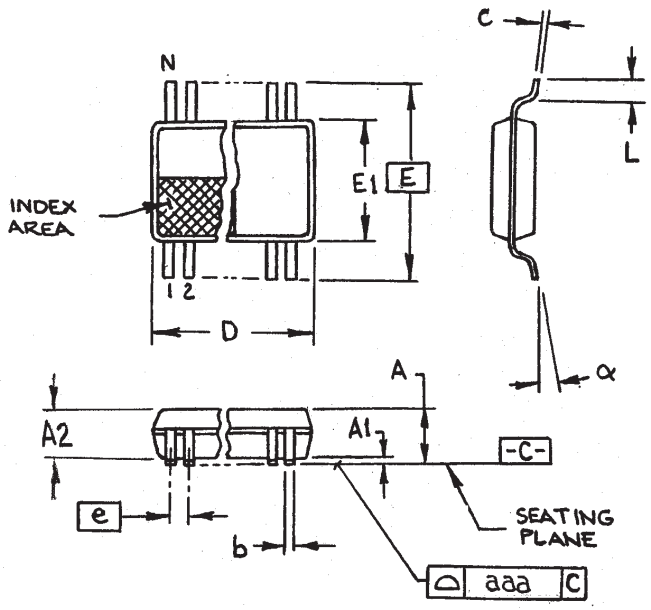
Ordering Information

ICS952001yFT

Example:

ICS XXXX y F - T

- **Designation for tape and reel packaging**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.30
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

MO-153 JEDEC 7/6/00 Rev B
Doc.# 10-0039

Ordering Information

ICS952001yFT

Example:

ICS XXXX y G - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
G=TSSOP

Revision Designator

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device

Registered Company

9001

For more information on Integrated Circuit Systems Inc. or any of our products please visit our web site at:
http://www.icst.com