## General Description

The ICS854104I is a low skew, high performance 1-to-4 Differential-to-LVDS Clock Fanout Buffer. Utilizing Low Voltage Differential Signaling (LVDS), the ICS854104I provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS854104I accepts a differential input level and translates it to LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the ICS854104I ideal for those applications demanding well defined performance and repeatability.

## Features

- Four differential LVDS output pairs
- One differential clock input pair
- CLK/nCLK can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Each output has an individual OE control
- Maximum output frequency: 700MHz
- Translates differential input signals to LVDS levels
- Additive phase jitter, RMS: 0.232ps (typical)
- Output skew: 50ps (maximum)
- Part-to-part skew: 350ps (maximum)
- Propagation delay: 1.3ns (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

## Block Diagram
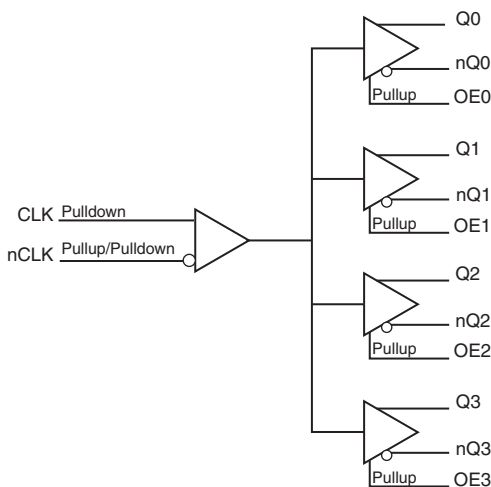


## Pin Assignment



**ICS854104**

**16-Lead TSSOP**
**4.4mm x 5.0mm x 0.925mm package body**
**G Package**
**Top View**

# Pin Descriptions and Characteristics

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | OE0 | Input | Pullup | Output enable pin for Q0, nQ0 outputs. See Table 3. LVCMOS/LVTTL interface levels. |
| 2 | OE1 | Input | Pullup | Output enable pin for Q1, nQ1 outputs. See Table 3. LVCMOS/LVTTL interface levels. |
| 3 | OE2 | Input | Pullup | Output enable pin for Q2, nQ2 outputs. See Table 3. LVCMOS/LVTTL interface levels. |
| 4 | $V_{DD}$ | Power | | Positive supply pin. |
| 5 | GND | Power | | Power supply ground. |
| 6 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 7 | nCLK | Input | Pullup/Pulldown | Inverting differential clock input. $V_{DD}/2$ default when left floating. |
| 8 | OE3 | Input | Pullup | Output enable pin for Q3, nQ3 outputs. See Table 3. LVCMOS/LVTTL interface levels. |
| 9, 10 | nQ3, Q3 | Output | | Differential output pair. LVDS interface levels. |
| 11, 12 | nQ2, Q2 | Output | | Differential output pair. LVDS interface levels. |
| 13, 14 | nQ1, Q1 | Output | | Differential output pair. LVDS interface levels. |
| 15, 16 | nQ0, Q0 | Output | | Differential output pair. LVDS interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | k$\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | k$\Omega$ |

# Function Table

## Table 3. Output Enable Function Table

| Inputs | Outputs |
|---|---|
| OE[3:0] | Q[0:3], nQ[0:3] |
| 0 | High-Impedance |
| 1 | Active (default) |

# Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of he product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5V |
| Outputs, $I_O$ (LVDS)<br>    Continuous Current<br>    Surge Current | <br>10mA<br>15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 100.3°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

**Table 4A. LVDS Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | | | | 75 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |

**Table 4C. Differential DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK, nCLK | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nCLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 0.5 | | $V_{DD}$ − 0.85 | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as $V_{IH}$.

## Table 4D. LVDS DC Characteristics, $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{OD}$ | Differential Output Voltage | | 250 | 350 | 450 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change | | | | 50 | mV |
| $V_{OS}$ | Offset Voltage | | 1.2 | 1.3 | 1.45 | V |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change | | | | 50 | mV |

## Table 5. AC Characteristics, $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $f_{MAX}$ | Output Frequency | | | | 700 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | | 0.9 | | 1.3 | ns |
| $f_{jit}$ | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.232 | 0.245 | ps |
| | | 100MHz, Integration Range: 12kHz – 20MHz | | 0.235 | 0.250 | ps |
| $tsk$(o) | Output Skew; NOTE 2, 4 | | | | 50 | ps |
| $tsk$(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 350 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 180 | | 660 | ps |
| odc | Output Duty Cycle | | 45 | | 55 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f_{MAX}$ unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crossing point of the input to the differential output crossing point.
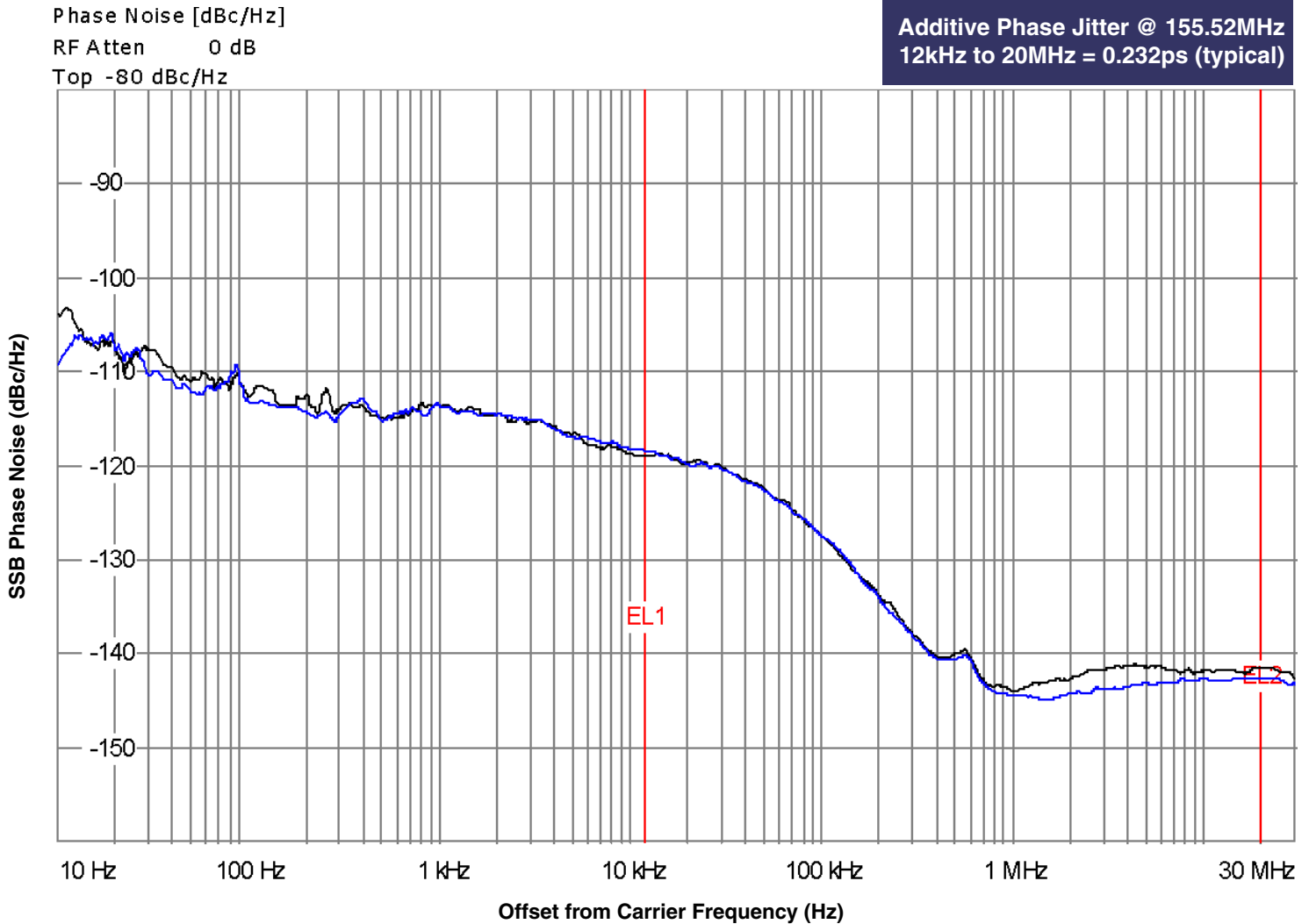NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

# Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

```
Phase Noise [dBc/Hz]
RF Atten      0 dB
Top -80 dBc/Hz
```

**Additive Phase Jitter @ 155.52MHz
12kHz to 20MHz = 0.232ps (typical)**



Axis labels — Y: SSB Phase Noise (dBc/Hz), values -90, -100, -110, -120, -130, -140, -150. X: Offset from Carrier Frequency (Hz), values 10 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz, 1 MHz, 30 MHz. Markers EL1, EL2.

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator is the Rhode & Schwarz SMA 100A Signal Generator 9kHz – 6GHz. Phase noise is measured with the Agilent E5052A Signal source Analyzer.
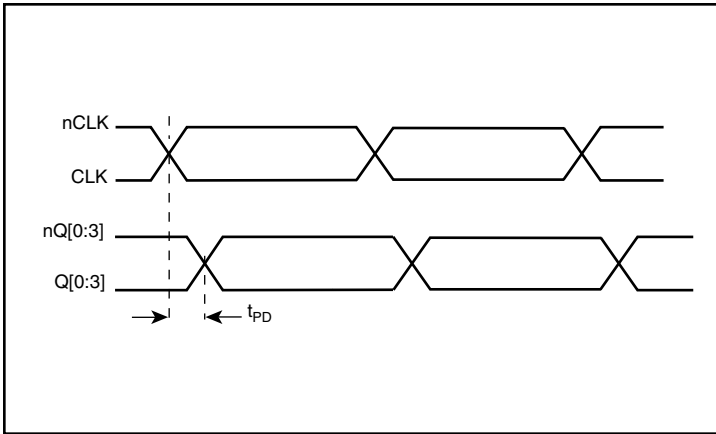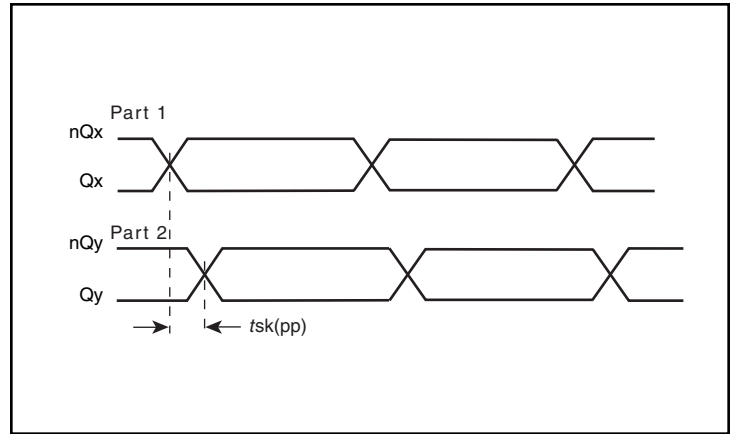
# Parameter Measurement Information
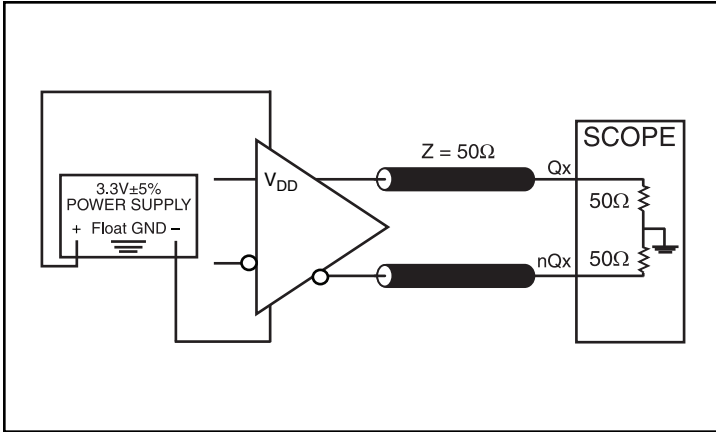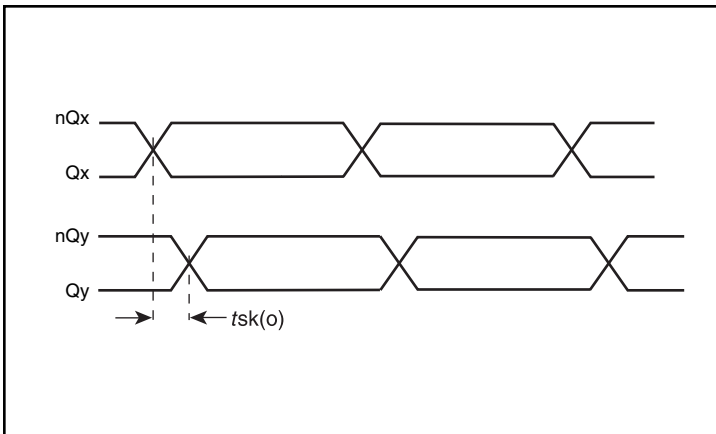


**3.3V LVDS Output Load AC Test Circuit**
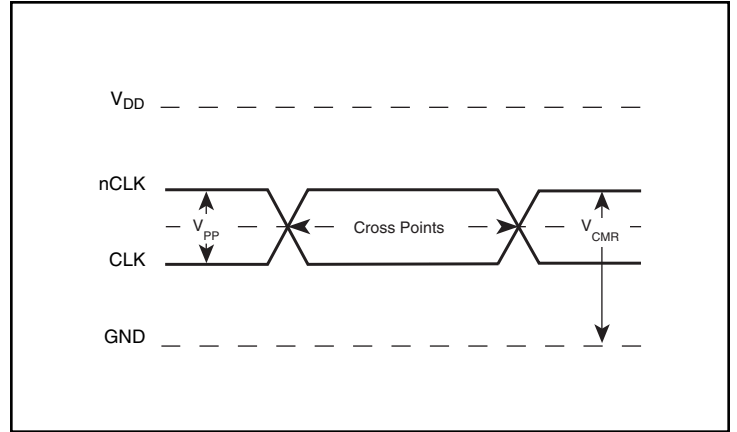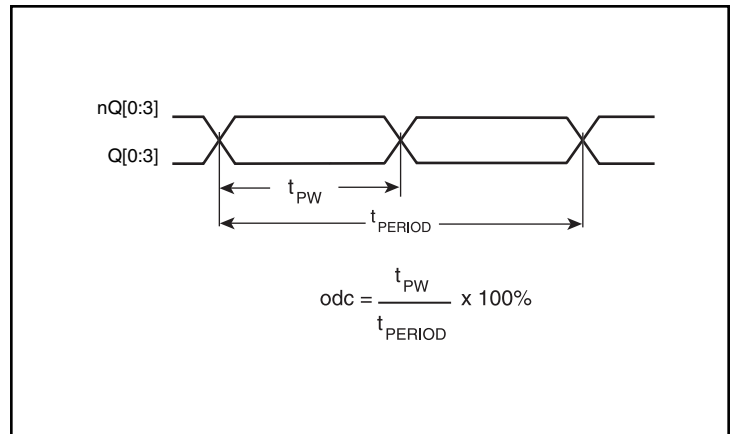


**Differential Input Level**



**Propagation Delay**



**Part-to-Part Skew**



**Output Skew**



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$
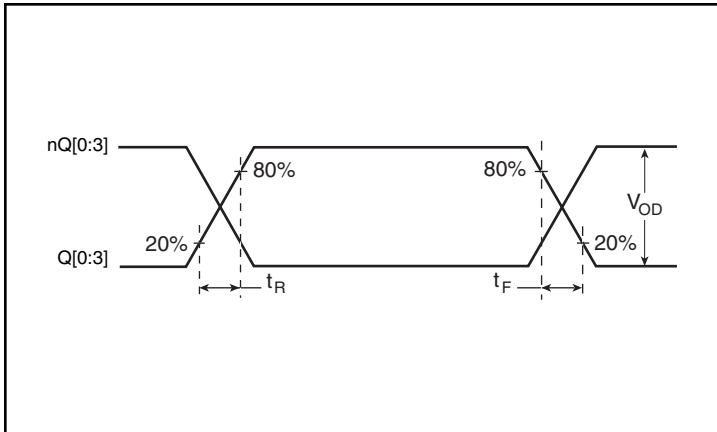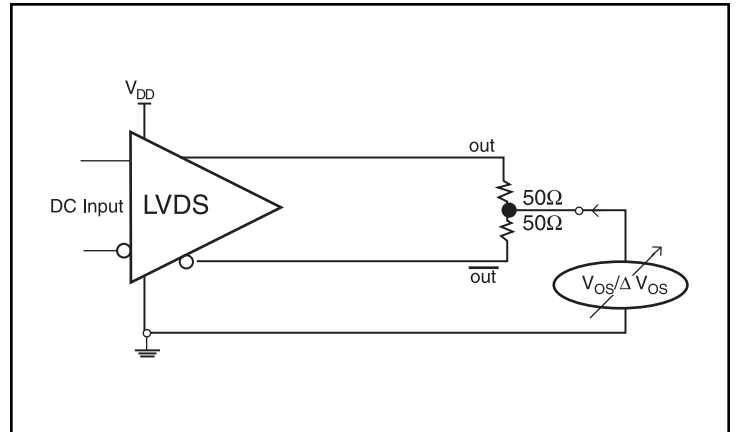
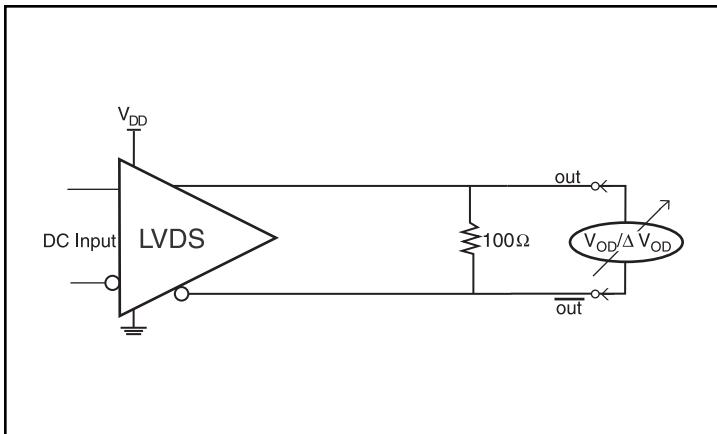**Output Duty Cycle/Pulse Width/Period**

## Parameter Measurement Information, continued



**Output Rise/Fall Time**



**Offset Voltage Setup**



**Differential Output Voltage Setup**

# Applications Information

## Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_{REF}$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{DD}$ = 3.3V, R1 and R2 value should be adjusted to set $V_{REF}$ at 1.25V. The values below are for when both the single ended swing and $V_{DD}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{DD}$ + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.
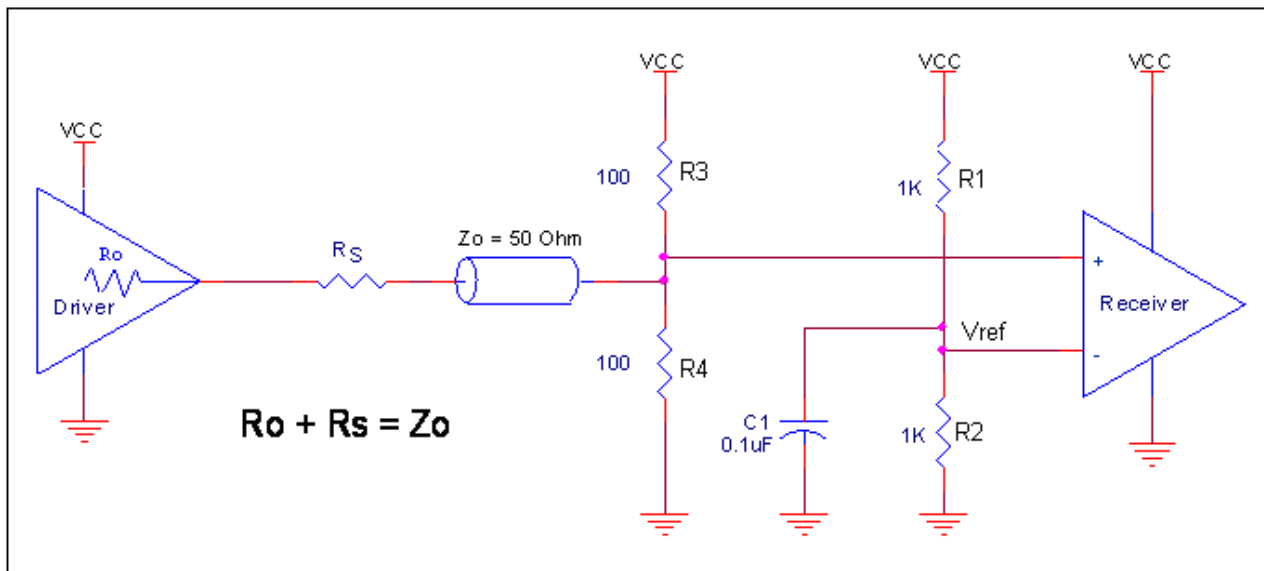


**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A* to *2F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.
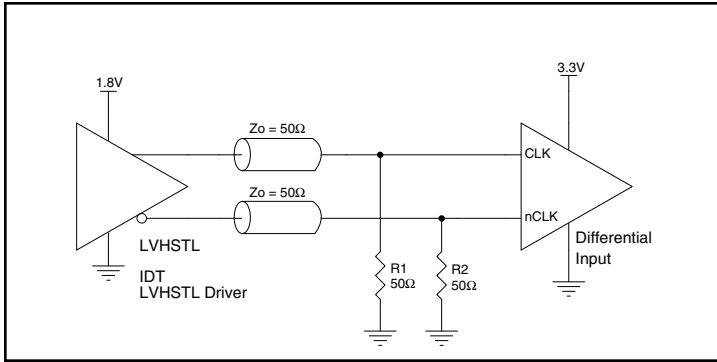


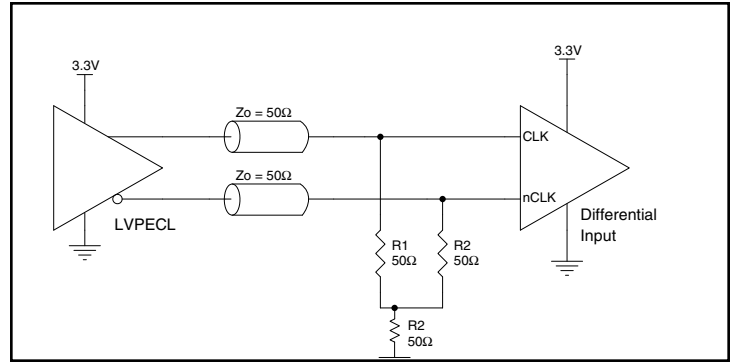**2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**



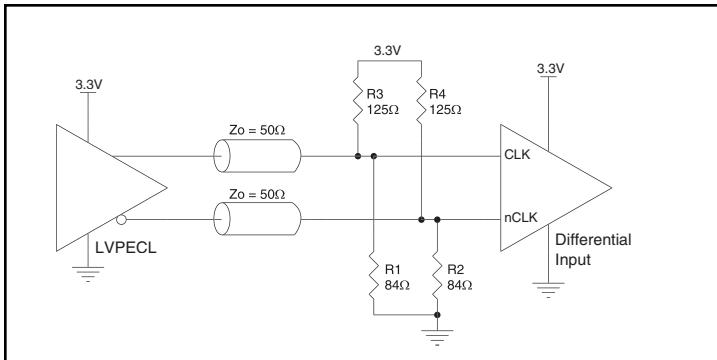**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



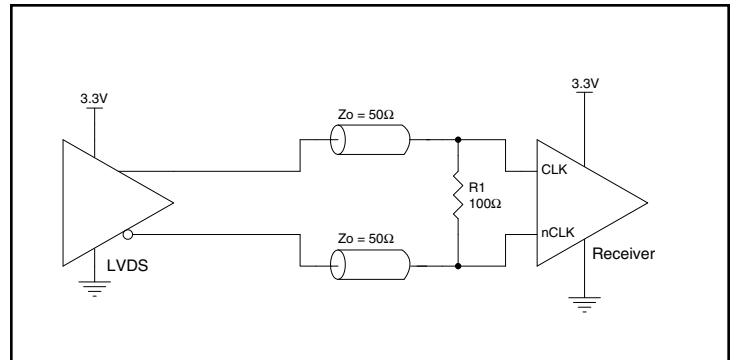**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**
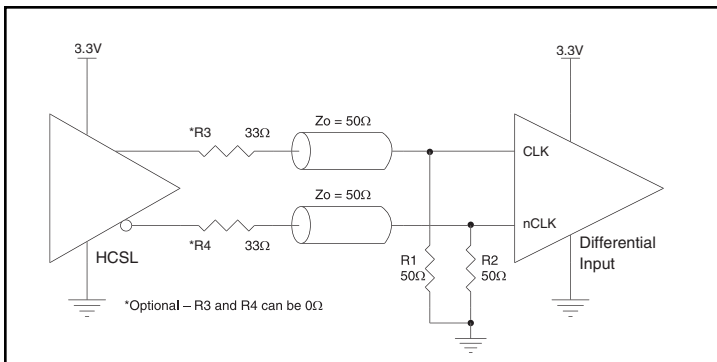


**Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**



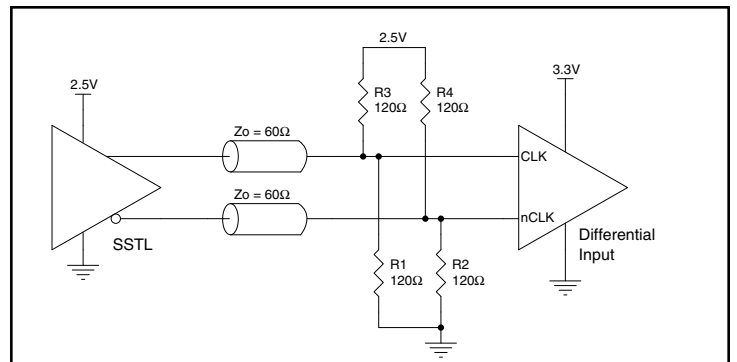**Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 2F. CLK/nCLK Input Driven by a 2.5V SSTL Driver**

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ($Z_T$) is between 90$\Omega$ and 132$\Omega$. The actual value should be selected to match the differential impedance ($Z_0$) of your transmission line. A typical point-to-point LVDS design uses a 100$\Omega$ parallel resistor at the receiver and a 100$\Omega$ differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

**Figure 3A. Standard Termination**

**Figure 3B. Optional Termination**
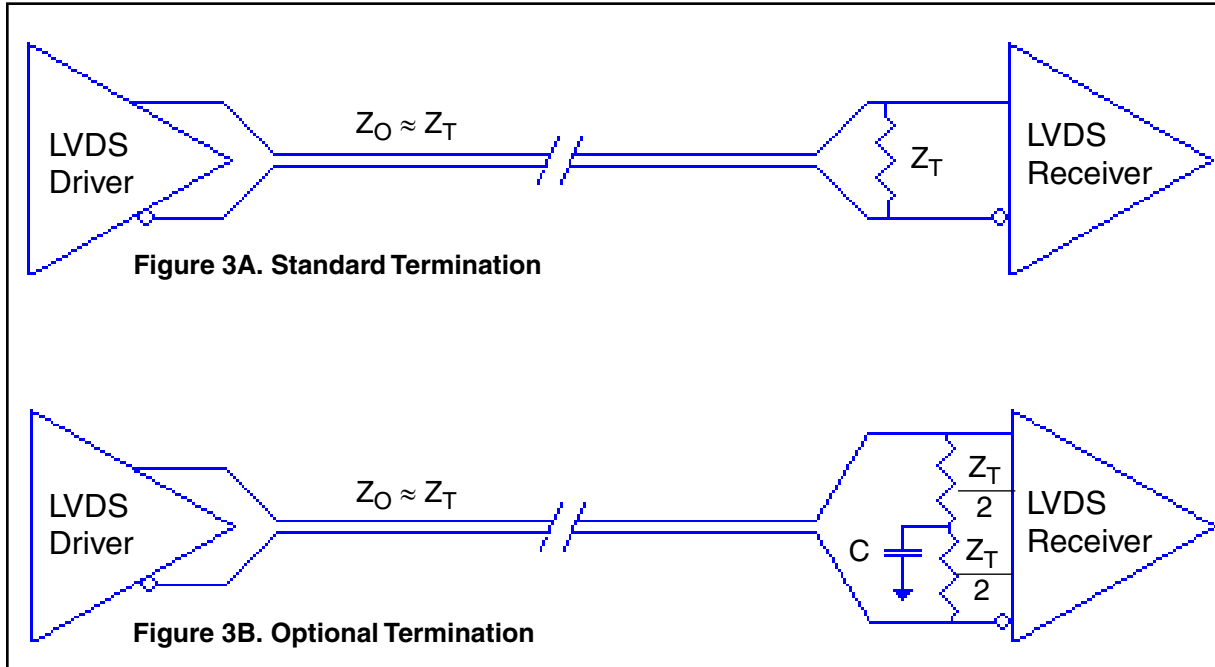
**LVDS Termination**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854104I.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS854104I is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = $V_{DD\_MAX}$ * $I_{DD\_MAX}$ = 3.465V * 75mA = **259.875mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.260W * 100.3°C/W = 111.1°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

### Table 6. Thermal Resistance $\theta_{JA}$ for 16-Lead TSSOP, Forced Convection

| $\theta_{JA}$ **by Velocity** | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 100.3°C/W | 96.0°C/W | 93.9°C/W |

# Reliability Information

**Table 7. $\theta_{JA}$ vs. Air Flow Table for a 16-Lead TSSOP**

| | $\theta_{JA}$ **by Velocity** | | |
|---|---|---|---|
| **Meters per Second** | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 100.3°C/W | 96.0°C/W | 93.9°C/W |

# Transistor Count

The transistor count for ICS854104I is: 286

# Package Outline and Package Dimensions
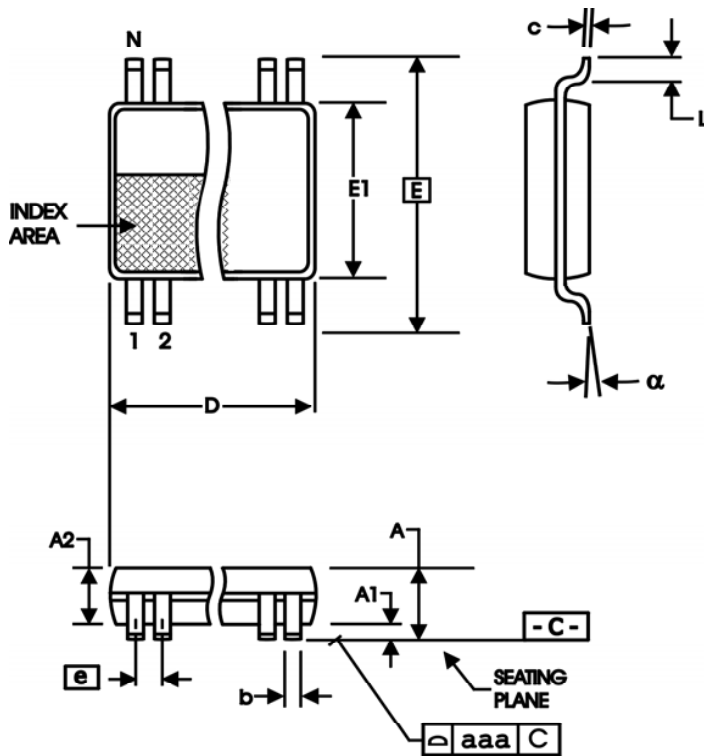
**Package Outline - G Suffix for 16-Lead TSSOP**



**Table 8. Package Dimensions**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 16 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 4.90 | 5.10 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| **α** | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 854104AGILF | 54104AIL | "Lead-Free" 16-Lead TSSOP | Tube | -40°C to 85°C |
| 854104AGILFT | 54104AIL | "Lead-Free" 16-Lead TSSOP | Tape & Reel | -40°C to 85°C |

## Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | T5 | 4 | AC Characteristics - deleted "Bank A" test conditions from part-to-part skew row. | 8/13/09 |
| B | T5 | 4 | AC Characteristics - Additive Phase Jitter, added maximum spec for 155.52MHz and added 100MHz specs. | 9/10/10 |
| | | 8 | Updated *Wiring the Differential Input to Accept Single-ended Levels.* | |
| | | 10 | Updated *LVDS Driver Termination.* | |
| B | T4B | 3 | Corrected typo error; $I_{IH}$ = 5µA Max, $I_{IL}$ = -150µA Min. | 1/30/14 |
| | T9 | 13 | Deleted quantity from Tape & Reel | |

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TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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