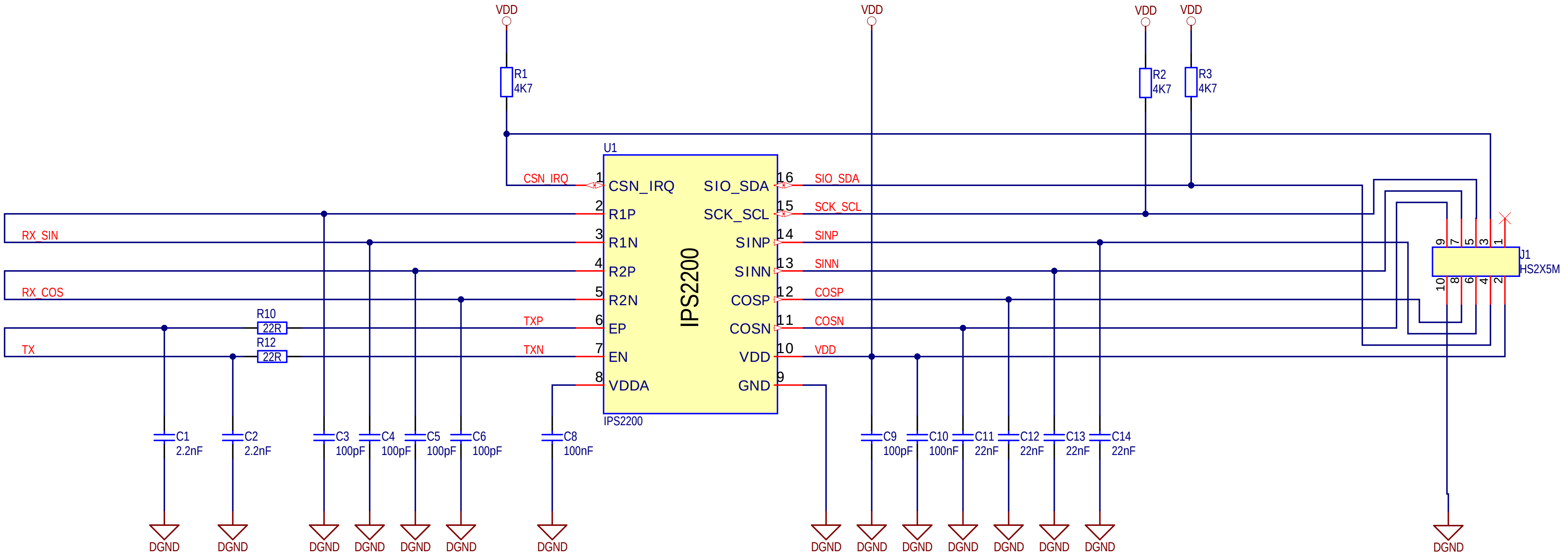
IDT Europe GmbH
A Renesas Company

R_59_IPS2200_8X45_OD32_ID18

Date: 11.09.2019
Project: R_59_V10_IPS2200_8X45_OD32_ID18.PrjPCB
Version 1.0
Content: Schematic
Coil PCB Layout
Coil PCB 3D Model
Bill of Materials
PCB Manifacture Requirements
Coil Layer Stack
Target PCB Layout
Target PCB 3D Model



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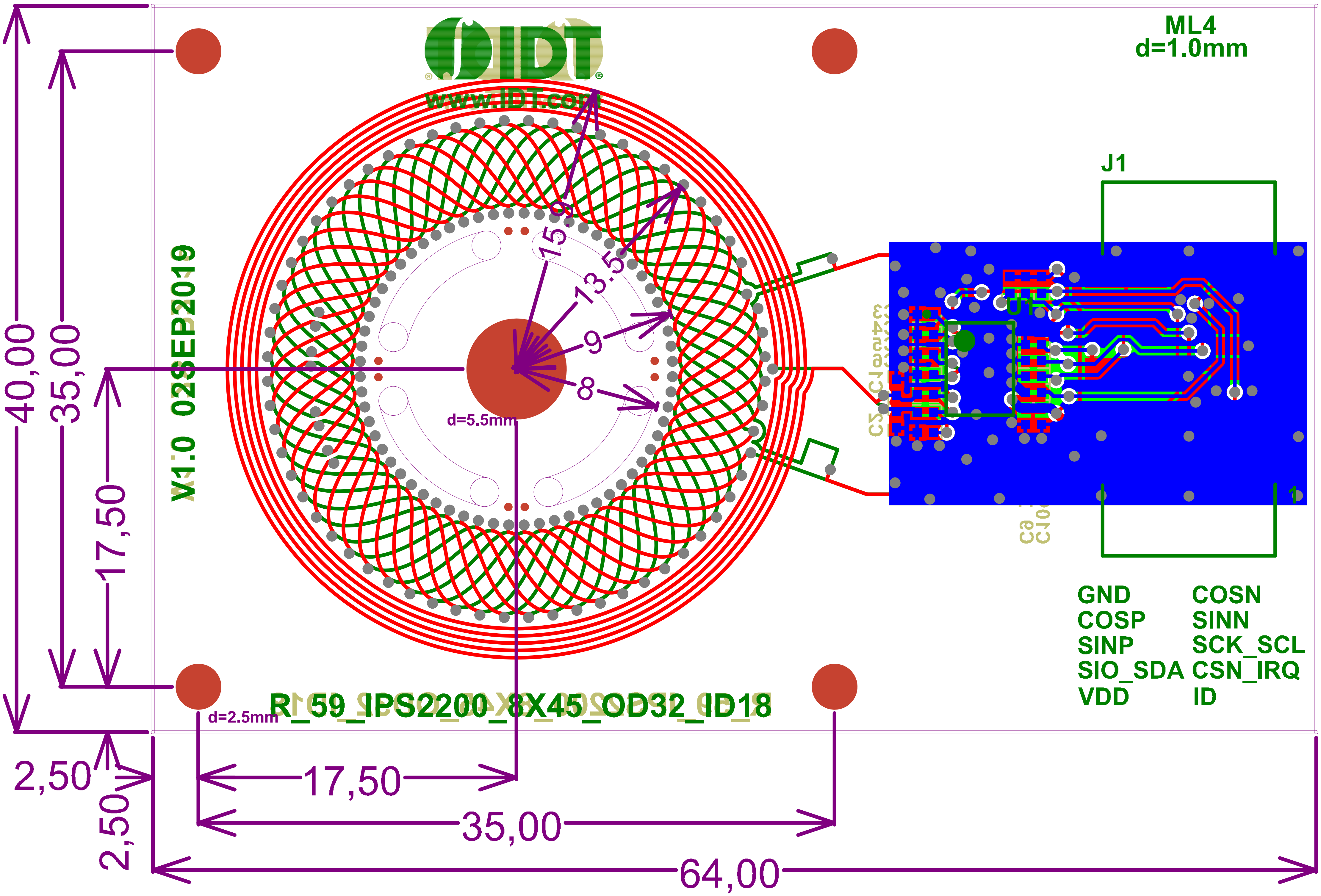
Sheet title	R_59_V10_IPS2200_8X45_OD32_ID18		Size	A4	
File name	R_59_V10_IPS2200_8X45_OD32_ID18.SCHDOC				
Date	11.09.2019	*System Engineering Team*	Drawn by	B.GOMBOR	Sheet 1 of 1

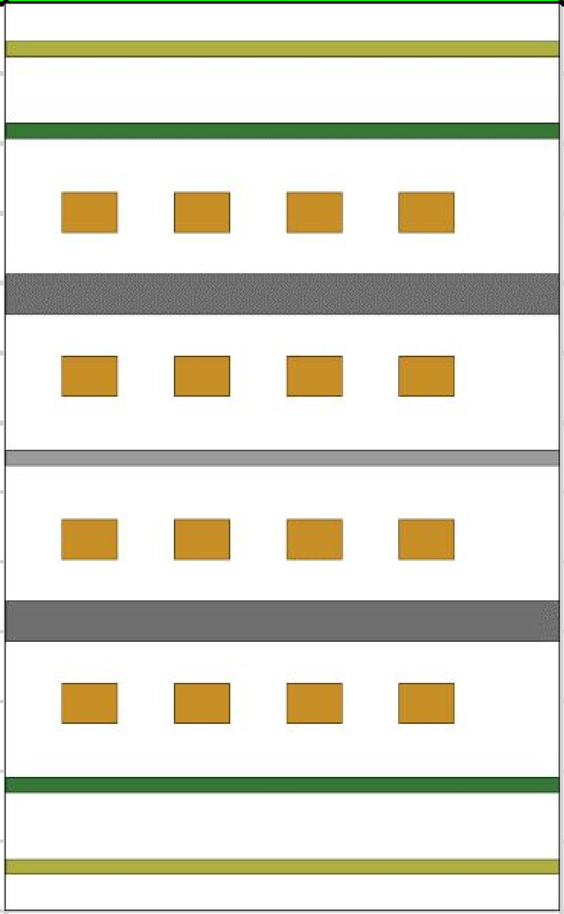

ML4
d=1.0mm
www.IDT.com
J1
U1
1
V1.0 02SEP2019
15.9
13.5
9
8
d=5.5mm
d=2.5mm
R_59_IPS2200_8X45_OD32_ID18
GND
COSP
SINP
SIO_SDA
VDD
COSN
SINN
SCK_SCL
CSN_IRQ
ID
40,00
35,00
17,50
2,50
2,50
17,50
35,00
64,00

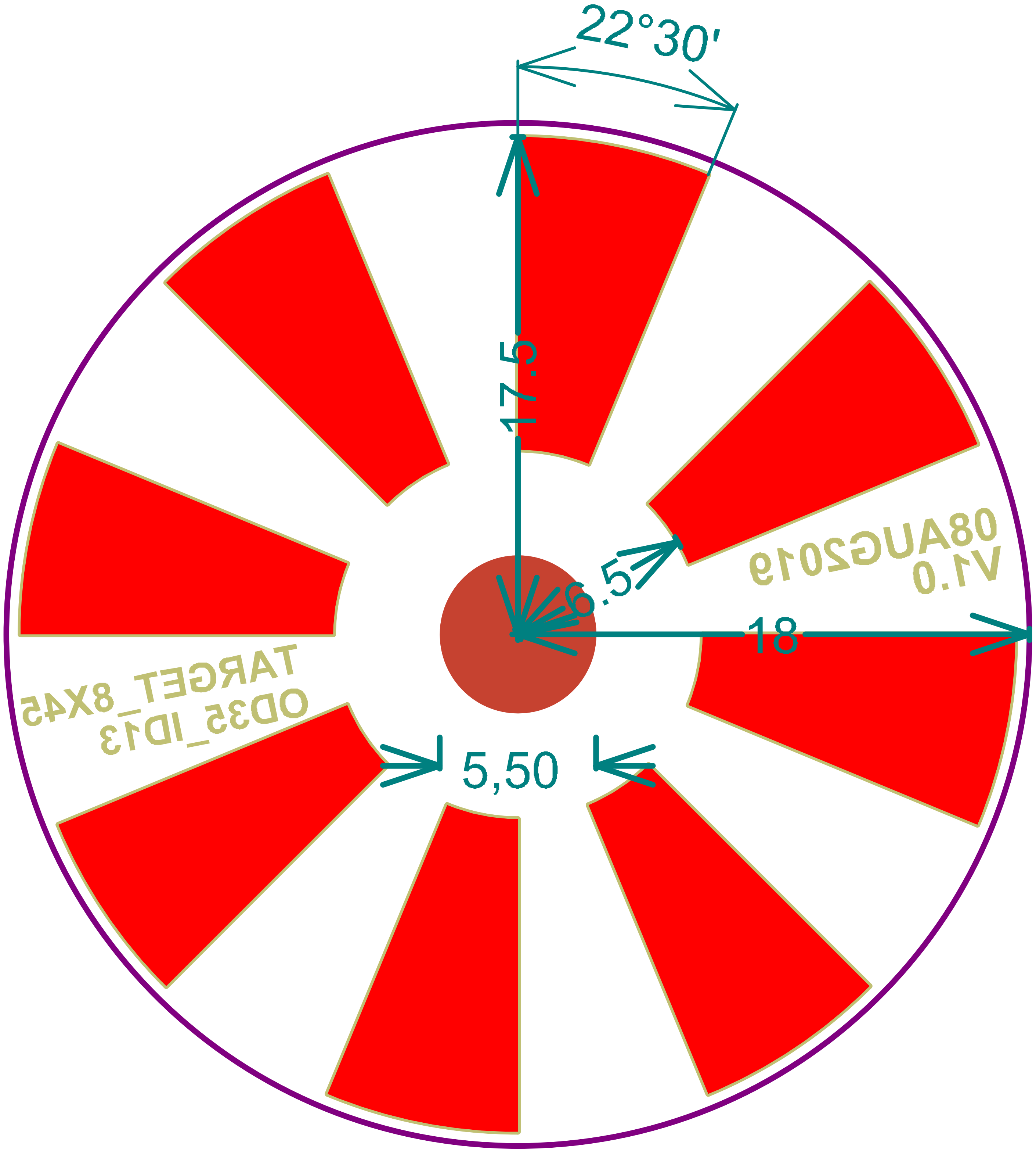
Designator	Value	Quantity	Footprint
C1, C2	2.2nF	2	C0402 3D
R1, R2, R3	4K7	3	R0402 3D
C11, C12, C13, C14	22nF	4	C0402 3D
R10, R12	22R	2	R0402 3D
C8, C10	100nF	2	C0402 3D
C3, C4, C5, C6, C9	100pF	5	C0402 3D
J1	HS2X5M	1	T821M110A1S100CEU-B
U1	IPS2200	1	TSSOP16_NVT02006

Manufacturing requirements

Name	R_59_V10_IPS2200_8X45_OD32_ID18
Number of layers	4
Base material	FR-4
Thickness	1.0 mm +/- 10%
Thickness of copper coating	35 µm
Final cover	ENIG
Minimal copper width	0.2 mm
Minimal copper to copper distance	0.15 mm
Via hole/pad diameter	0.3/0.6 mm
Slotted holes	no
Panel dimensions	64 x 40 mm
Silk screen color	white on both sides
Solder mask color	green

Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	Solder Resist	0,030mm	3,5
4		Top Layer	Copper	0,035mm	
5		Dielectric 1	FR-4	0,175mm	4,29
6		Inner Layer 1	Copper	0,035mm	
7		Dielectric 3	FR-4	0,530mm	3,96
8		InnerLayer 2	Copper	0,035mm	
9		Dielectric 2	FR-4	0,175mm	4,29
10		Bottom Layer	Copper	0,035mm	
11		Bottom Solder	Solder Resist	0,030mm	3,5
12		Bottom Overlay			
13		Bottom Paste			
	Height : 1,080mm				


22°30'
17.5
6.5
18
5,50
TARGET_8X45
OD35_ID13
08AUG2019
V1.0