Separate Sheet

Product Specifications of the RL78/L1A

Group name		RL78/L1A	
		80-pin LQFP 0.5mm Pitch	100-pin LQFP 0.5mm Pitch
Code Flash Memory (KB)		48 - 96	64 - 128
RAM (KB)		5.5	5.5
Data Flash Memory (KB)		8	8
I/O port		59	79
CPU		RL78 CPU core	
Main System Clock	High-speed system clock	1 - 20MHz : Vdd=2.7 - 3.6V 1 - 8MHz : Vdd=1.8 - 2.7V	
	High-speed on-chip oscillator clock	HS (high-speed main) operation mode : 1 – 24 MHz (Vdd=2.7 - 3.6V) HS (high-speed main) operaion mode : 1 - 16MHz (Vdd=2.4 - 3.6V) LS (low-speed main) operation mode : 1～8MHz (Vdd=1.8 - 3.6V)	
Subsystem Clock		32.768 kHz : Vdd=1.8 - 3.6V	
Low-speed on-chip oscillator clock		15 kHz (TYP) : Vdd=1.8V - 3.6V	
Timer	16-bit timer TAU	8 channels（Timer outputs: 8, PWM outputs: 7 (Note 1)	
	8-bit or 16-bitinterval timer	2 channels (8 bits)/ 1 channel (16 bit)	
	Watchdog timer	1 channel	
	12-bit interval timer	1 channel	
	Real-time clock 2	1 channel	
	RTC output	1 channel 1 Hz (subsystem clock : f_{SUB} = 32.768 kHz)	
Clock output/buzzer output		2	
12-bit resolution A/D converter		10 channels	14 channels
12-bit resolution D/A converter		2 channels	
Voltage reference		2.5 V / 2.048 V / 1.8 V / 1.5 V	

Operational amplifier	Total	3 channels	
	OpAMP with analog switches	2 channels (2 in-out/channel)	2 channels (4 in-out/channel)
Comparator		1 channel	
Serial interface		CSI(SPIsupported): 1 channel/UART: 1channel/Simplified I^2C: 1 channel CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channelCSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel	
I^2Cbus		1channel	
LCD controller /driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
	Segment signal output	32 (28) (Note 2)	45 (41) (Note 2)
	Common signal output	4 (8) (Note 2)	
Data transfer controller (DTC)		30 sources	
Event link controller (ELC)		Event input: 22, Event trigger output: 8	
Vectored interrupt sources	Internal	31	
	External	9	
Key interrupt		8	
Power-on-reset circuit		Power-on-reset：1.51±0.04 V Power-down-reset：1.50±0.04 V	
Voltage detector		Rising edge: 1.88 V - 3.13 V(10 stages) Falling edge: 1.84 V - 3.06 V(10 stages)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.8V - 3.6V	
Operating ambient temperature		T_A = -40 - +85℃	

(Note 1) The number of outputs varies, depending on the setting of channels in use and the number of the master.
(Note 2) The number in parentheses indicates the number of signal outputs when 8 coms are used

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