RENESAS Tool News

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Notes on Using the Following Tools
CS+ Code Generator for RL78 (CS+ for CC)
CS+ Code Generator for RL78 (CS+ for CA and CX)
e2 studio (Code Generator Plug-in)
Applilet3 Coding Assistance Tool for RL78

When using the CS+ Code Generator for RL78 (CS+ for CC), the CS+ Code Generator for RL78 (CS+ for CA and CX), the e2 studio (Code Generator Plug-in), and the Applilet3 coding assistance tool for RL78, take note of the problems on the following points that are described in this note.

1. Indication of Channels of Serial Interface IICA
Applicable MCUs: RL78/G14 group
R5F104MK, R5F104PK, R5F104ML, and R5F104PL

2. Procedure for Setting the PLL Clock
Applicable MCUs: RL78/F13, RL78/F14, and RL78/F15 groups

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1. Indication of Channels of Serial Interface IICA

1.1 Products Concerned

- V2.03.00 and later versions of the CS+ Code Generator for RL78 (CS+ for CC)
- V2.03.00 and later versions of the CS+ Code Generator for RL78 (CS+ for CA and CX)
- V2.1.0.21 and later versions of the e2 studio (V1.0.0 and later versions of the Code Generator Plug-in)
- V1.07.00 and later versions of the Applilet3 coding assistance tool for RL78

1.2 Applicable MCUs

RL78/G14 group

R5F104MK, R5F104PK, R5F104ML, and R5F104PL

1.3 Description

Since the GUI does not indicate the channel 1 IICA serial interface for the above products, graphically setting up its operation is impossible. Accordingly, code for channel 1 cannot be generated.

1.4 Workaround

Create a project for an MCU of the RL78/G14 group which has at least 80 pins and also has 256 KB of ROM. Set up the IICA1 serial interface then generate the code. Use the generated code for channel 1.

1.5 Schedule for Fixing the Problem

This problem will be fixed in the versions of the products to be released in April 2016.

2. Procedure for Setting the PLL Clock

2.1 Products Concerned

- V2.01.00 and later versions of the CS+ Code Generator for RL78 (CS+ for CC)
- V2.01.00 and later versions of the CS+ Code Generator for RL78 (CS+ for CA and CX)
- V2.1.0.21 and later versions of the e2 studio (V1.0.0 and later versions of the Code Generator Plug-in)
- V1.07.00 and later versions of the Applilet3 coding assistance tool for RL78

2.2 Applicable MCUs

RL78/F13, RL78/F14, and RL78/F15 groups

2.3 Descriptions

The generated code for setting the PLL clock in the clock generation circuit differs from the example of PLL settings in User's Manual: Hardware for the MCUs and is thus incorrect.

2.4 Workaround

Modify the generated code so that it is in accord with the example of PLL settings in User's Manual: Hardware.
This modification is required every time code is generated.

Example: RL78/F13, F14 User's Manual: Hardware R01UH0368EJ0200 Document Search

Modify the code described in process 8 to 10 of "(1) Example of procedure for setting oscillation of PLL clock" in section 5.6.4,

Examples of Setting Circuit, in that user's manual.

Before modification:

```
-----------------------------------------------------------------------
void R_CGC_Create(void)
{
.............
   /* Set fMP to PLL clock select mode */     /* <- Step 9 */
   SELPLL = 1U;                              /* <- Step 9 */
   /* Set fSUB */
   XTSTOP = 1U;
   /* Set fSL */
   SELLOSC = 1U;
   /* Set fCLK */
   CSS = 0U;
   MDIV = _00_CGC_FMP_DIV_DEFAULT;           /* <- Step 8 */
   /* Set fIH */
   HIOSTOP = 0U;
.............
}
-----------------------------------------------------------------------
```

After modification:

```
-----------------------------------------------------------------------
void R_CGC_Create(void)
{
.............
   MDIV = _00_CGC_FMP_DIV_DEFAULT;   /* <- Step 8 (moved) */
   /* Set fMP to PLL clock select mode */     /* <- Step 9 (moved) */
   SELPLL = 1U;                              /* <- Step 9 (moved) */
   while ((PLLSTS & 0x88) != 0x88U ) {       /* <- Step 10 (added) */
    ; }                                  /* <- Step 10 (added) */
   /* Set fSUB */
   XTSTOP = 1U;
   /* Set fSL */
   SELLOSC = 1U;
   /* Set fCLK */
   CSS = 0U;
   /* Set fIH */
   HIOSTOP = 0U;
.............
}
-----------------------------------------------------------------------
```

2.5 Schedule for Fixing the Problem

This problem will be fixed in the versions of the products to be released in April 2016.
