RENESAS

AN-1079 High Speed Level Shifting with Dual Supply GreenPAK

Author: Luke Thomas, Gino Castillo Date: August 6, 2015

Level Shifting Applications

Designs are growing in complexity, including different ICs in the same design which operate in different voltage domains. SOCs continue to lower their power supply voltage, while sensors tend to stay at higher voltages. Logic levels compatible 5V at are incompatible with their 3.3V counterparts. Multiple power rails increase the need to have interface chips that translate voltages from one level to another with sufficient speed.

Level Shifting with LVDI

There are many ways to interface with different voltages levels in PAK. See AN-1063 to see a level shifting technique external coupling using circuitry not discussed here. One way to detect low level logic levels is by using the Low Voltage Digital Input (LVDI) PIN option available in PAK. Setting a pin to LVDI lowers the VIH to ~1.2V, even with high Vdd voltage. Thus, low level inputs can be detected while outputs maintain a high voltage swing. However, throughput is limited when using the LVDI because the asymmetry of the LVDI circuitry causes propagation delay skew of ~700ns.

Dual Supply GreenPAK

The Dual Supply GreenPAK, SLG46621V, includes two voltage rails with integrated level shifters to make interfacing two levels easy while maintaining high speed. Vdd (PIN1) powers the main circuitry and the I/O for PINs 2-10. Vdd2 (PIN14) powers the I/O circuitry for PINs 12-20.

The secondary Vdd is labeled Vdd2 and automatically translates between the PINs powered by Vdd2 and the rest of the chip.

For I/O connected to Vdd2, the LVDI settings do not need to be used when interfacing different voltage domains. Thus, the Vdd2 is powered by the lower voltage rail to match the threshold specs while avoiding the propagation delay from the LVDI.

Throughput Comparisons

A comparison is shown graphically in Figure 1 visualizing the increase in throughput by using the Dual Supply GreenPAK's internal level shifters as compared to an LVDI configuration. The constraint to determine the maximum throughput is determined using two rules: the output duty cycle must stay between 40%-60% and the output voltage must be greater than 90% of typical VOH.

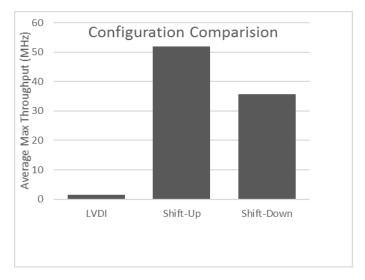


Figure 1. Input PIN Comparison



The LVDI, Shift-up, and Shift-down configurations are explained below.

LVDI: Both Vdd and Vdd2 are set to 5V, while the input signal ranges from 0V to 1.8V. The input pin is configured as below, shown in Figure 2.

Properties				
PIN 3				
I/O selection:	Digital input			
Input mode: OE = 0	Low voltage digital i			
Output mode: OE = 1	None			
Resistor:	Floating			
Resistor value:	Floating \$			

Figure 2. LVDI Configuration Settings

Shift-Up: To shift an input signal up in the Dual Supply GreenPAK, configure the input supplied on Vdd2 as a Digital Input with/without Schmitt Trigger. Match Vdd2 to the level of the lower voltage input signal. For these tests, Vdd is set to 5V and Vdd2 along with the input signal is at 1.8V. The input configuration is shown in Figure 3.

Properties	×				
PIN 20					
I/O selection:	Digital input 🔷				
Input mode: OE = 0	Digital in without Sd 🗢				
Output mode: OE = 1	None				
Resistor:	Floating				
Resistor value:	Floating 🔷				

Figure 3. Shift-up Configuration Settings

Shift-Down: Conversely, shifting down is just as easy. Choose input PINs 2-10 with the higher Vdd while the shifted-down output on PINs 12-20.

CH1 (Yellow/Top line) – PIN#03 5V Input CH2 (Green/ 2nd line) – PIN#20 1.8V Output

Vdd1 = 5V, Vdd2 = 1.8V



Figure 4. Level-Shift Response at 15MHz

Test Data

These quick tests were done using two independent power supplies, a frequency generator and the SLG46621V programed in socket. The input signal was connected via a shielded SMA cable to the GreenPAK socket. Table 1 shows the input configurations and Table 2 shows the results used in this application note.



Test	Input P-P	Input PIN	Output Config	Vdd1	Vdd2
		Low Voltage			
LVDI	1.8V	Digital Input	Push Pull 1x	5V	5V
		DI without			
Shift-up	1.8V	Schmitt Trig	Push Pull 1x	5V	1.8V
		DI without			
Shift-down	5V	Schmitt Trig	Push Pull 1x	5V	1.8V

Table 1. Test Configurations

			Measured Throughput
Test	In (PIN)	Out (PIN)	(MHz)
	2	20	1.4
	3	19	1.7
LVDI	4	18	1.1
	20	3	43
	19	4	54
Shift-up	18	5	59
	3	20	30
	4	19	31
Shift-down	5	18	46

Table 2. Test Results

Conclusion

The throughput for a LVDI configuration is much lower in all cases due to the propagation delay through the LVDI circuitry, thus a Dual Supply GreenPAK is better equipped to handle high speed signals between different voltages.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit <u>www.renesas.com/contact-us/</u>.