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Introduction

This app note describes how to build a current monitor system using a programmable mixed-signal ASIC (SLG46620), a precision current shunt monitor (INA199A2), an LDO (LP2951), and two 7-segment LED displays.

Design Goal

The design started with a need to build a simple, small, and low-cost current monitor to measure real time current in a USB charging environment.

While voltage on the V_{BUS} line ranges from 5V to 20V, the charge current ranges from 100mA to 3A. Recently, Dialog Semiconductor designed a 2-digit display voltmeter (AN-1075*); the current monitor design incorporated the 2-digit voltmeter and added a wide input voltage LDO to power the system as well as a current shunt monitor IC to precisely measure the current flow through the V_{BUS} line. Since the current is displayed through a two-digit display, its resolution is 0.1A.

System Level Design Approach

Figure 1 shows the current monitor's circuit schematic.

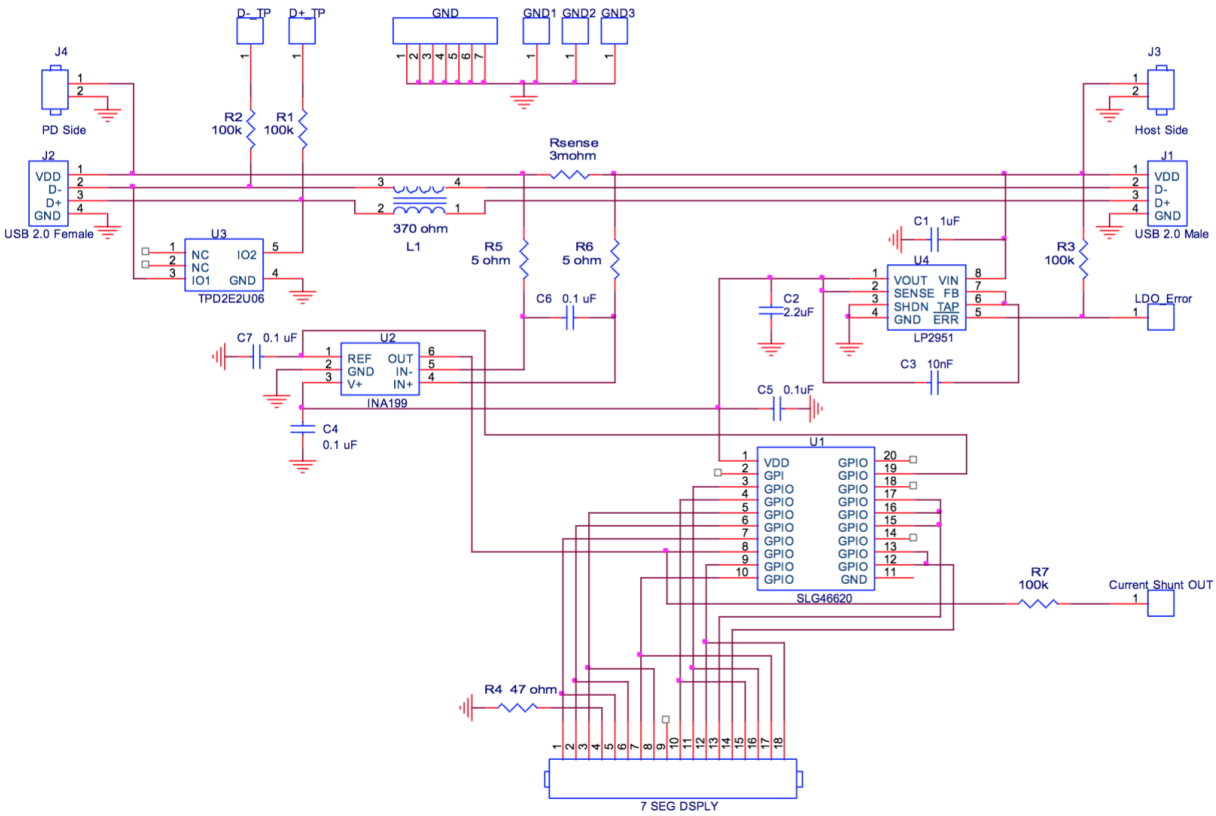

Figure 1. Current Monitor Schematic

* **AN-1075 – GreenPAK Voltmeter with 2 Digit LED Display**

It can be inserted in the middle of any USB charging path via its male and female USB Type A connectors. There are common mode chokes on the data lines; D+ and D- test points can be used to observe USB handshaking. The circuit is powered from USB host side (J1), where V_{BUS} (labeled as VDD in figure 1) can range between 5V to 20V. LP2951 is the LDO and regulates system power to 3.3V and powers the INA199A2 and SLG46620. INA199A2 amplifies the voltage difference across the 3mΩ sense resistor 100 fold, and feeds it to the SLG46620's ADC input. The SLG46620 then converts the ADC's output code into a two digit decimal number between 00 and 30, which corresponds to 0.0A and 3.0A respectively. Finally, the SLG46620 displays these 2 digits by time multiplexing them onto two 7-segment displays. To account for the ADC's inherent offset voltage, SLG46620 also outputs a reference voltage for the INA199A2 reference.

SLG46620 Design Approach

The current monitor front end is comprised of the Programmable Gain Amplifier (PGA), Analog to Digital Converter (ADC) and Finite State Machine (FSM0). The ADC digitizes the input voltage value and loads it into FSM0, which is used as a counter with its output period directly proportional to the loaded data. When the input voltage is ~30mV (ADC offset voltage), ADC output will be digital 0, which provides the shortest FSM0 period. When the input voltage is 1.03 volts, ADC output will be 255, which provides the longest counter period.

For example, when ADC's input is at 0.53V, its output will be 128. FSM0's output will be a periodic waveform with a period of 128*[FSM0 clock] and a pulse width of 1 FSM0 clock. The ADC offset is eliminated by using the 30mV reference voltage generated by SLG46620's DAC0 macro-cell. Figure 2 shows the relationship between ADC output value and the FSM0 counter period. At the end of its period, FSM0's output will go high for 1 count.

The next circuit utilizes two 4-bit decimal counters (DC) to count up to the current readings that will be shown on the LED. The tenths digit (0.1A) DC is called First Decimal Counter (FDC) and includes DFF0, DFF1, DFF2, and PIPE DELAY0. The ones digit (1.0A) DC is called Second Decimal Counter (SDC) and includes DFF6, DFF7, DFF8, and PIPE DELAY1. FDC counts up the tenths digit at a rate of 23ms per digit. It counts 10 times from 1111_2 to 0110_2 as shown in figure 3, which shows FDC's timing diagram with respect to the decimal value it represents as well as FSM0 out.

SDC is used to count the ones digit at a rate of 230ms (23ms x 10). It counts 4 times from 1111_2 to 1100_2. The FDC increments the current display every 100mA and the SDC increments the current display every 1A with a maximum value of 3A. The example in figure 3's current reading is 1.6A. The FDC counts through an entire 0 through 9 cycle, then after it resets to 0, SDC increments from 0 to 1. FDC then counts to 6, which is when the FSM0 has finished its count period and the DCs have captured the 1.6A reading.

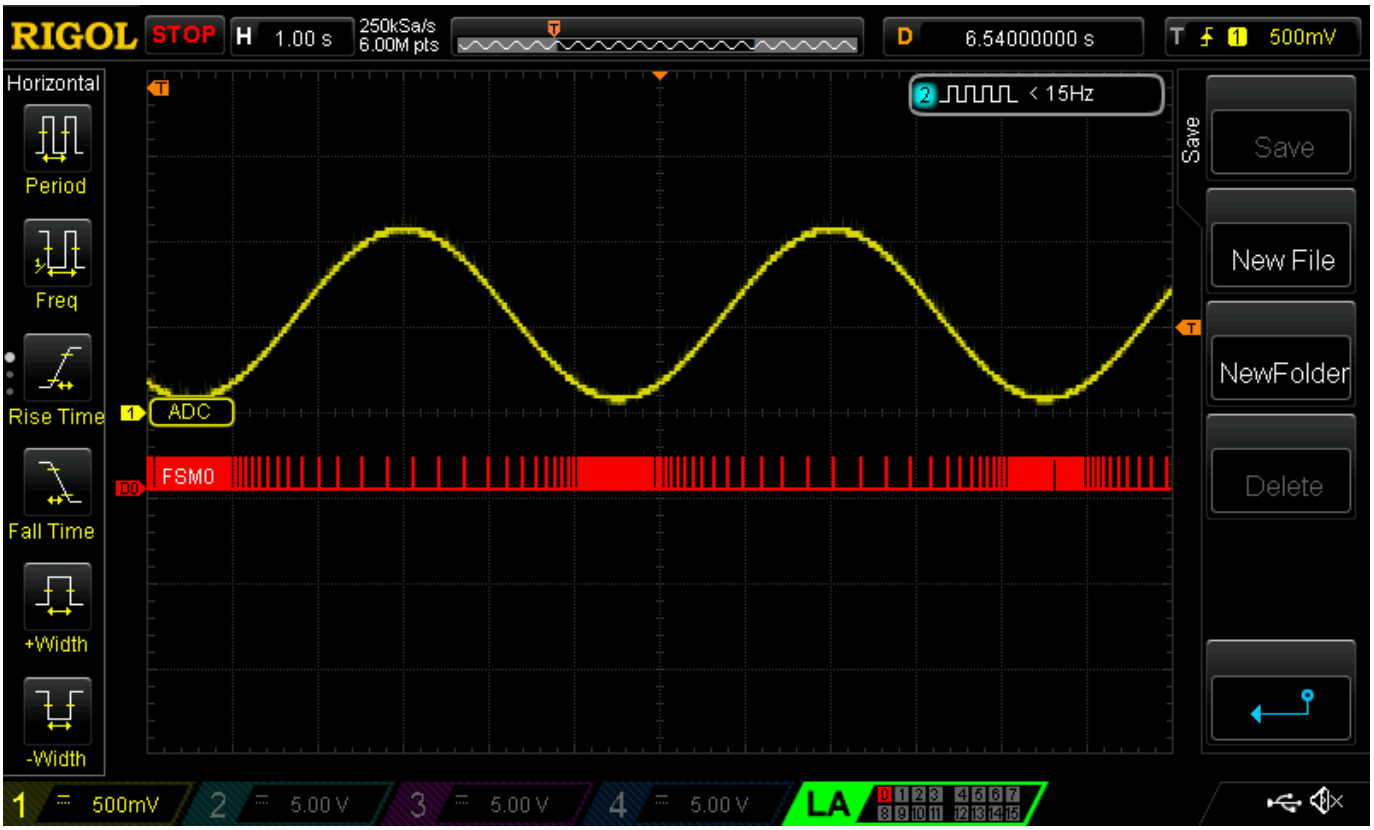

Figure 2. ADC value vs. FSM0 count period

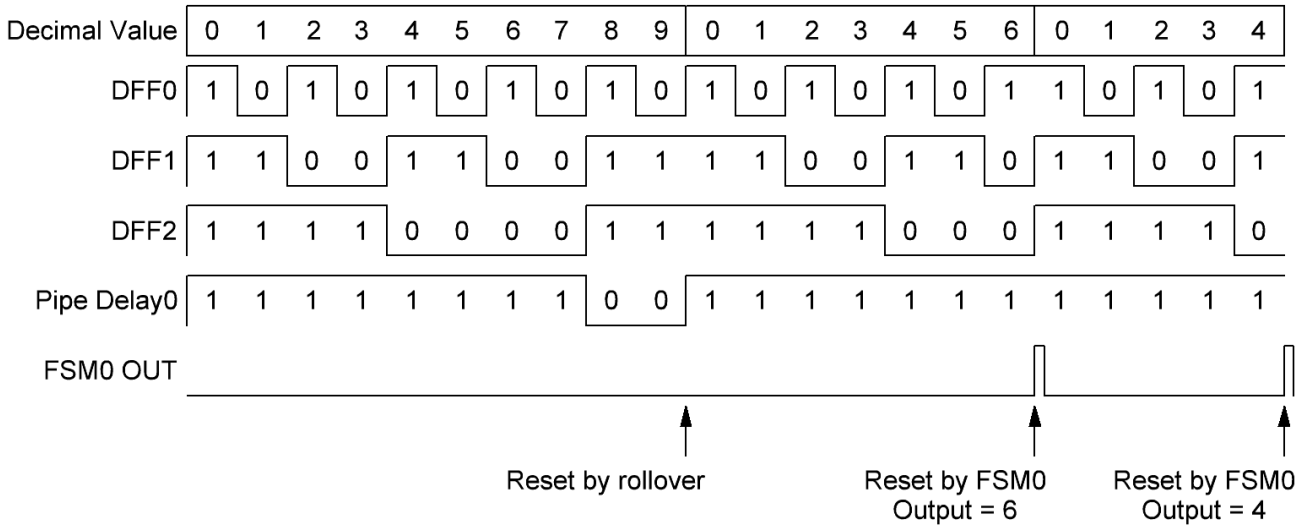

Figure 3. FDC Timing Diagram

After reaching the last value, FSM0 output's rising edge resets both DCs. FDC will be reset by 2-bit LUT1 and 3-bit LUT2, while SDC will be reset by 3-bit LUT8. At this point, the appropriate binary code is captured and decoded onto the 7-segment displays. In order for the numerical values of the measured current and decimal counters contents to match, the decimal counters and FSM0 counter have to match in their respective periods. The design ignores ADC input voltage higher than 900mV because max current to be measured is 3A (3mΩ x 100 gain x 3A = 900mV). 900mV ADC input corresponds to 230 ADC output. In other words, FSM0 clock times max FSM0 counter data (230) should be equal to DC clock times max DC data (30). In this design, FSM0 clock is sourced from CNT1 (3ms) and DC clock is sourced from CNT0 (23ms); therefore, 3*230=23*30=690ms.

Table 1 below shows a few examples.

At different current readings, table 1 shows that Total Count Time = FSM0 data * FSM0 clock period = DC data * DC clock period. The ADC converts the analog voltage into 8 bits of data and loads them into FSM0. Since the FSM0 and DC total count time is the same, the DC will stop counting at a value that corresponds to the current reading. In row 1, the DC stops counting at 5, which corresponds to 0.5A current reading.

Since the DCs are always counting, they are not suitable for outputting signals directly to the display. So when CNT6 resets the DCs, their values are latched; LATCH3, LATCH4, LATCH5 and 3-bit LUT4 latch the FDC value and LATCH10, LATCH11, 3-bit LUT13, 3-bit LUT14 latch the SDC value. The circuit behaves as follows: CNT6 resets FSM0 through P DLY0 every 823ms (this is set to be longer than SDC total count time of 690ms). P DLY0's inverted signal stores DC values into the latches.

Current (A)	ADC Input (mV)	ADC output/FSM0 data	FSM0 clock period (ms)	DC data	DC clock period (ms)	Total Count Time (ms)
0.5	150	38	3	5	23	115
1	300	77	3	10	23	230
1.5	450	115	3	15	23	345
2	600	153	3	20	23	460
3	900	230	3	30	23	690

Table 1. FSM0 and DC Total Count Time

After this operation is finished, the second rising-edge detector (P DLY1) resets the DCs. After that, the data from the latches are ready to be displayed.

Display

7-segment displays require 4-bit binary code decoding as shown in figure 4. The seven segments are named "a" through "g"; each segment is controlled by one SLG46620 output pin.

Figure 4 shows, for example, that in order to display a "1", segments "b" and "c" need to be switched on. Figure 5 shows the decoder design portion of the SLG46620 design.

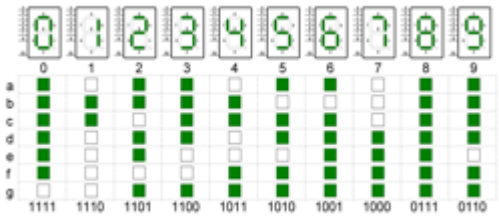

Figure 4. Display configuration table

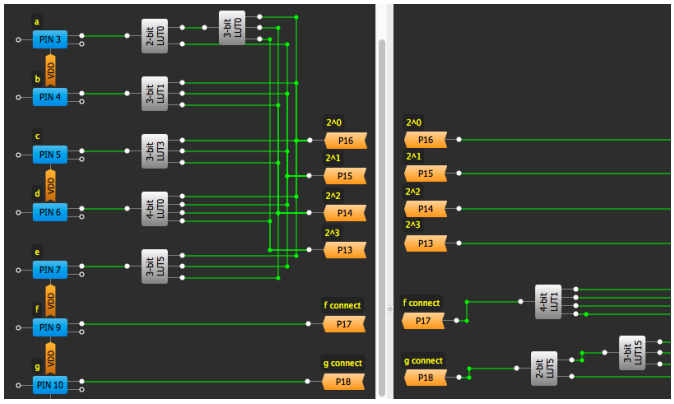

Figure 5. Decoder part review

Two Digits Display

The SLG46620 contains sufficient macro-cells to include the time-multiplex of two 4-bit latches' values to the 2 respective 7-segment displays.

3-bit LUTs 9, 10, 11, and 12 make up the mux for the 4-bit decoder. The mux select signal is a clock generated by DFF9. While the displays' cathodes are multiplexed with the decoder outputs, their anodes are multiplexed as well so current can alternatively flow through the tenths and unit digit displays. Since human eye response is magnitudes slower than 10kHz, both digits will appear to be constantly lit when in reality they are alternatively lit. The clock's 50% duty cycle ensures even light intensity across the two displays. Pins 12 and 13 are used to source the one's digit display anode; pins 15, 16, and 17 are used to source the tenths digit display anode.

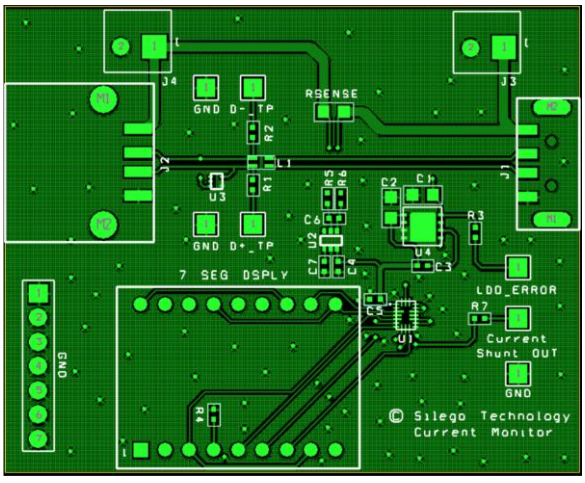

Figure 6. Current Monitor PCB layout top side

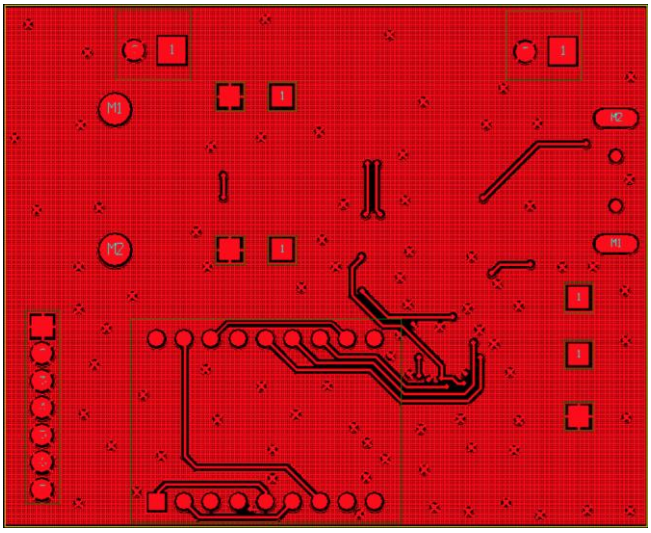

Figure 7. Current Monitor PCB layout bottom side

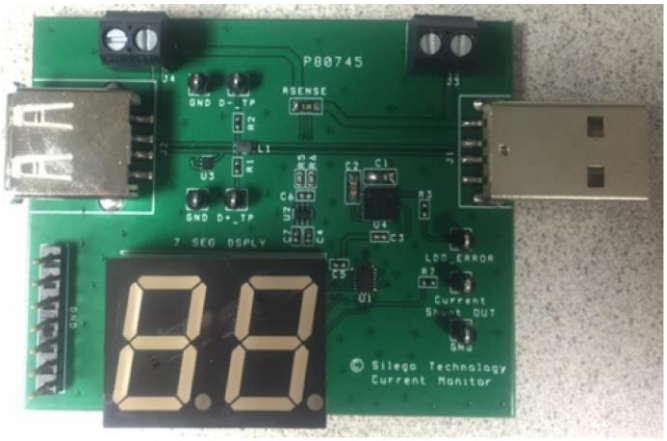

Figure 8. Current Monitor Board

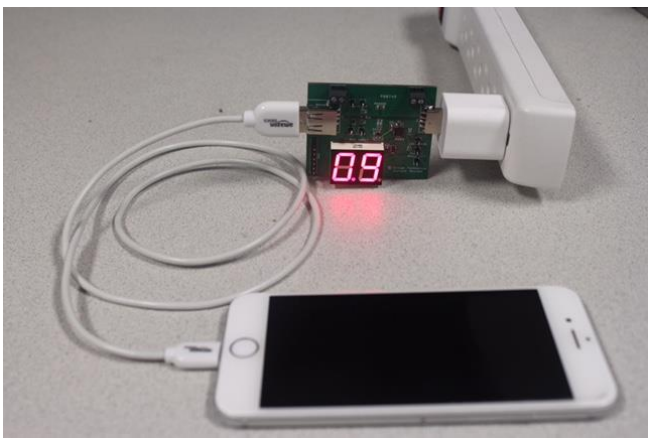

Figure 9. Current Monitor Board Measuring Phone Charge Current

Conclusion

This application note described how to implement a 2-digit current monitor with a pair of 7-segment displays using SLG46620 as the mixed-signal control element. Figure 6 and 7 shows the PCB top and bottom layer routing respectively. Figure 8 and 9 shows the physical current monitor board. This design can be used for current measurement from 0 to 3A with 100mA resolution. This design can be used to measure USB charge current up to 3A of any portable device. It is a variant of the Dialog 2-Digit Voltmeter and suggests that other ingenious designs can be spun from it as well.

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