

Introduction

In this app note we will create a cycle stealing control unit for AC line-powered loads using a GreenPAK IC device. Cycle stealing is also known as cycle skipping, pulse skipping, integral cycle control, and burst fire.

Cycle stealing works by turning a power control switch on and off when the load current and voltage are zero. This technique is also known as soft-switching. Soft switching practically eliminates electromagnetic interference generated by the switching action, eliminates the power losses caused by hard switching, and reduces electrical stress on the power switches, thereby increasing reliability. A disadvantage of cycle stealing is that it may produce low frequency pulsating currents in the electrical mains that supply the power to the system, which may result in visible flicker.

Cycle stealing is the preferred method of control for high-power electrical loads where the load response is slow compared to the AC line frequency. A device that would fit this example is a thermal heater.

Cycle Stealing Method

When using the cycle stealing method, the average power delivered to the load is adjusted by selectively switching in and out mains cycles. e.g. for a 50% power level, over a set period of time (called "control period" or "switching cycle"), half of the cycles will be "on" and half will be "off". Figure 1 (a) shows three different output power levels for 8 full control period cycles. If the control period is 8 cycles long and a 50% power level is desired, 4 cycles will be on and 4 cycles off. Obviously, it is better to arrange them in an alternating fashion (on-off-on-off...) rather than grouping the "on" cycles at the beginning of the control period, because alternating the cycles will reduce flicker. This approach of distributing the "on" and "off" cycles evenly over the control period is valid for any power level and shown in Figure 1 (b).

Increasing the skip percentage (the percentage of skipped to total cycles, SP) reduces average output power level, average output RMS voltage, and current. This is shown in table 1.

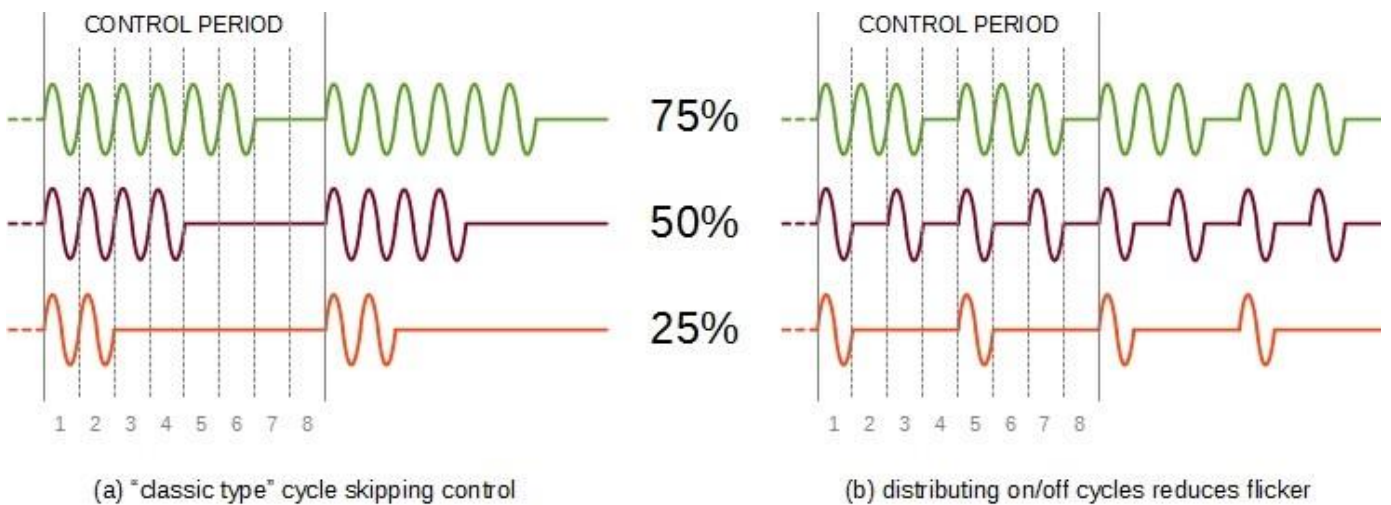


Figure 1. Cycle stealing method

	Formula	SP=0	SP=25%	SP=50%	SP=75%
Output power	$P = P_0 (1-SP)$	100%	75%	50%	25%
Output RMS voltage	$V = V_0 \sqrt{1 - SP}$	$V_0 = V_{input}$	86% V_0	71% V_0	50% V_0
Output RMS current	$I = I_0 \sqrt{1 - SP}$	$I_0 = V_0/R$	86% I_0	71% I_0	50% I_0

Table 1. Output power, RMS voltage, and RMS current

Flicker problems worsen as finer control resolution is required. Classic cycle stealing methods rely on skipping a certain percentage of cycles in a given control period. Hence, as power control resolution is increased, a greater number of cycles is needed in the control period, and as the control period extends, visible flicker worsens.

Cycle stealing can be done using half-cycles instead of full cycles, because mains voltage is zero in the middle of the mains cycle. Half-cycle control provides increased resolution and reduced flicker.

However, using a half-cycle stealing method may introduce a DC voltage to the output by switching on an unequal number of positive and negative half-cycles. The DC voltage may be irrelevant for some applications and unacceptable for others. Control circuitry may be designed so that an equal number of positive and negative half cycles is assured. Figure 2 (a) illustrates half-cycle stealing method on an 8-cycle (16 half-cycle) control period, while Figure 2 (b) illustrates the same method with balance control. Sometimes to achieve positive/negative balance cycle distribution over the control period has to be imperfect.

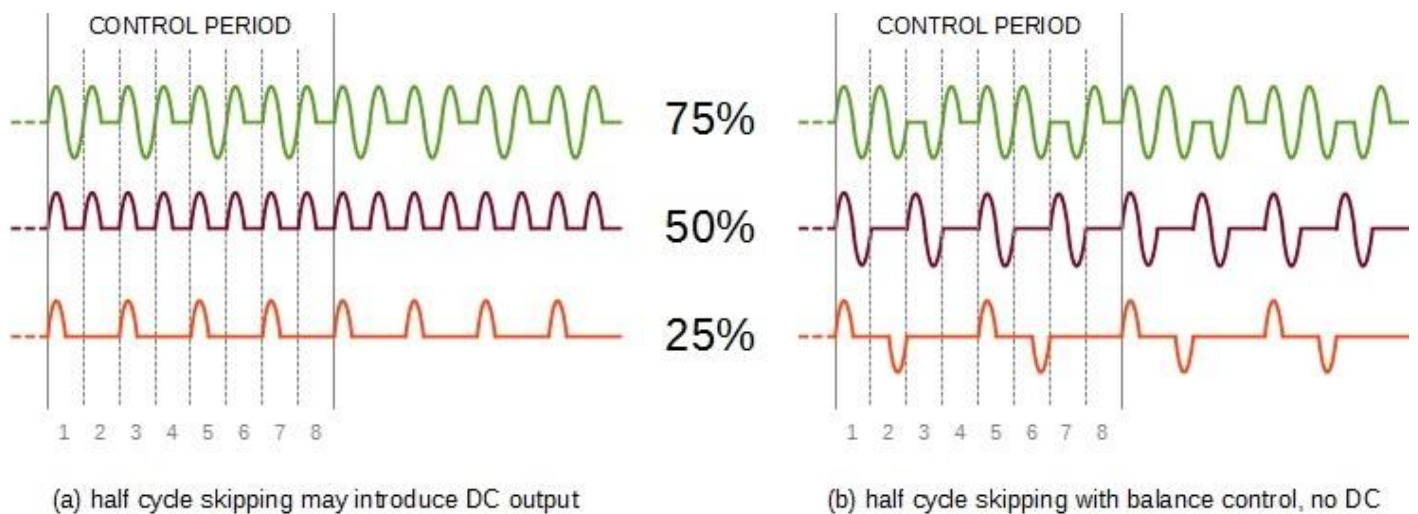


Figure 2. Half cycle skipping method

Cycle stealing is suitable for resistive loads, because the current is directly proportional to voltage. For inductive, capacitive, and non-linear load types, cycle stealing might not be suitable. For example, a classic diode rectifier will keep the same power level with almost any skip percentage – the more cycles are skipped, the higher the current will be while bridge diodes are conducting, so there is no sense applying cycle stealing control to such non-linear load.

Cycle stealing vs phase-angle control

A popular method for AC power control is phase-angle control. In this control method, the output is turned on each half-cycle after a delay period. By varying the delay, the power level is adjusted. The two methods are presented side by side for comparison in Figure 3, showing the output voltage waveform at three different power levels and full power. Phase angle control method has no flicker problem, but it does have the drawback of inherently generating radio frequency interference and presenting a non-linear load to the AC line.

Adding components to solve EMI issues also adds cost, mass and bulk to the circuit.

In the phase-angle control method, the waveform is the same in every cycle, so only higher frequencies (the harmonics of the mains frequency) are introduced by the power control process. Since lower frequencies are not introduced, there is no flicker.

However, hard switching at non-zero voltage introduces parasitic ringing in LC circuits at very high frequencies (RF), because both the parasitic inductance and capacitance involved are very small. Figure 4 shows the current waveform for three different power levels to illustrate the ringing introduced by hard switching. Note that the ringing is bigger when voltage is higher at the switching moment (red waveform), because more energy is stored in the parasitic LC circuit at the beginning of the ringing transient. Since the cycle stealing method switches when voltage and current are zero, there is no energy stored within parasitic LC elements to start ringing and produce RF.

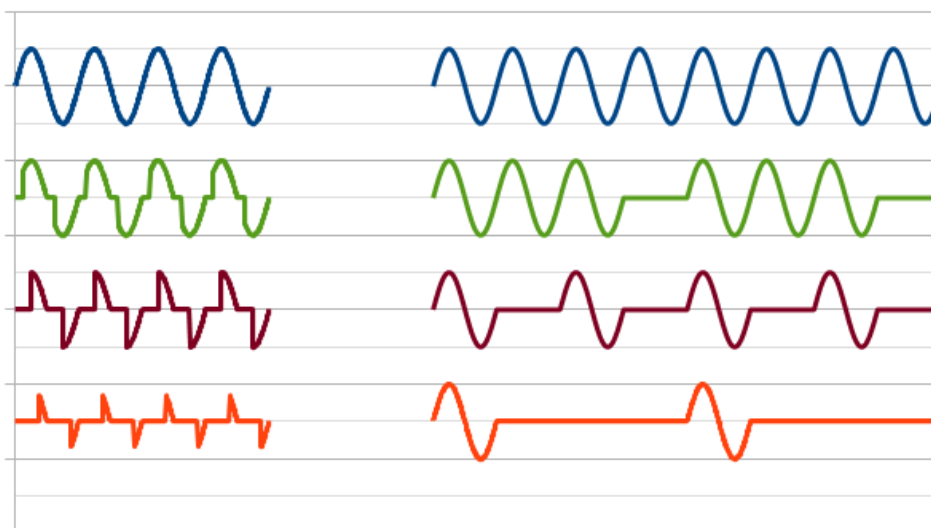


Figure 3. Cycle skipping vs Phase-angle control

The phase angle control circuit is considered easier and cheaper since cycle stealing requires a more complex control circuit. While that is generally true, GreenPAK ICs enable implementing a complete control circuit in a single device, thus negating that argument.

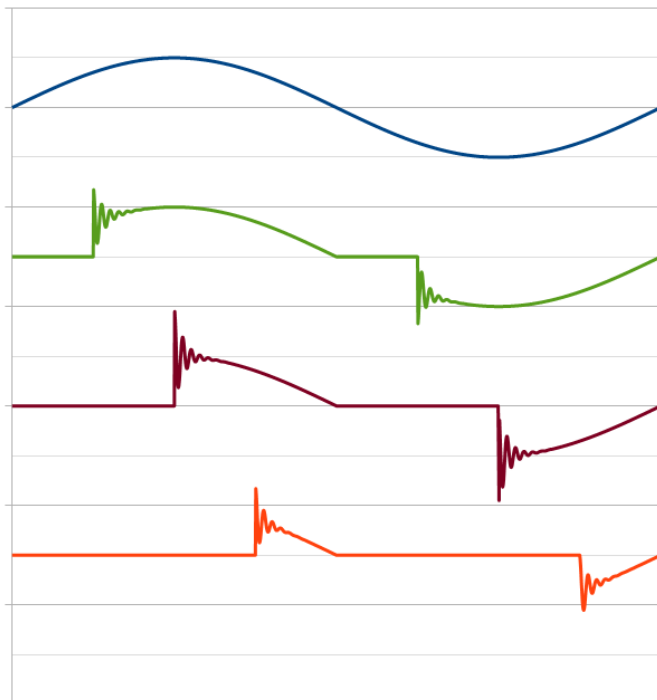


Figure 4. Phase-angle EMI issues

Power circuit

Since the focus of this application note is on the cycle stealing control circuit, the configuration of the power circuit is based on the MOC3063 IC that integrates a zero crossing circuit and a triac driver. An alternative solution for a power circuit with separate zero crossing circuits and triac drivers is presented in the Application Note [AN-1124 AC Phase Control Light Dimmer](#). We selected the MOC3063 for its simplicity and integration. Note that the snubber circuit composed of C1 and R3 is not necessary for cycle stealing.

The purpose of the snubber circuit is to choke the ringing resulting from hard switching, but with soft switching it can be omitted. Without the snubber circuit, the component count is down to the MOC3063, a power triac, and 2 resistors. The component values are calculated for controlling a 4kW load at 230VAC mains with power triac BTA41-600B. Triac-based AC power circuits are popular because they are simple, cost effective, and robust. At high load currents, triac forward-voltage drop creates considerable losses, so a heatsink is required. For improved efficiency, one could create a power circuit based on MOSFETs/IGBTs rather than triacs. However, high efficiency has its own disadvantages: higher component costs, circuit complexity, and reduced robustness.

The operation of the power circuit in Figure 5 is fairly simple. While the control signal is LOW, the load is off. While the control signal is HIGH, the MOC3063 will turn on the power triac T1 at each zero-crossing point, and the triac will stay on (latched) until the next zero-crossing. At the end of the half-cycle, just before zero-crossing, T1 will turn itself off, but if the control signal is HIGH at the zero-crossing moment, T1 will be immediately turned on again.

Control circuit within GreenPAK

When the PWM control signal with duty cycle D is applied to the control input of the power circuit, the half-cycle skip percentage will be exactly 1-D, provided that the PWM frequency is not synchronous with the mains frequency. It is easy to generate a PWM signal thanks to GreenPAK's integrated RC oscillator. There are several options to set the duty cycle of the PWM signal:

- analog by control voltage (e.g. from analog sensor)
- digital by serial communication (SPI or I2C)

- selectable from a set of predefined values by digital input signals (e.g. rotary switch)
- preset in register at startup

Note that if the PWM frequency is synchronized (phase locked) with the mains frequency, the skip percentage may only take integer values of fractions of the two frequencies and the resolution is finite. However, if the two frequencies are asynchronous, the resolution is not limited.

To make the PWM control signal asynchronous to the mains frequency, we will set the GreenPAK's RC oscillator to free-running mode. If the classic style of cycle stealing is desired (like the one presented in Figure 1(a)), the RC oscillator should be set to the mains frequency as the external clock source.

Timing diagrams for half-cycle control are shown in Figure 6. GreenPAK generates the PWM signal and applies it directly to the CTRL output.

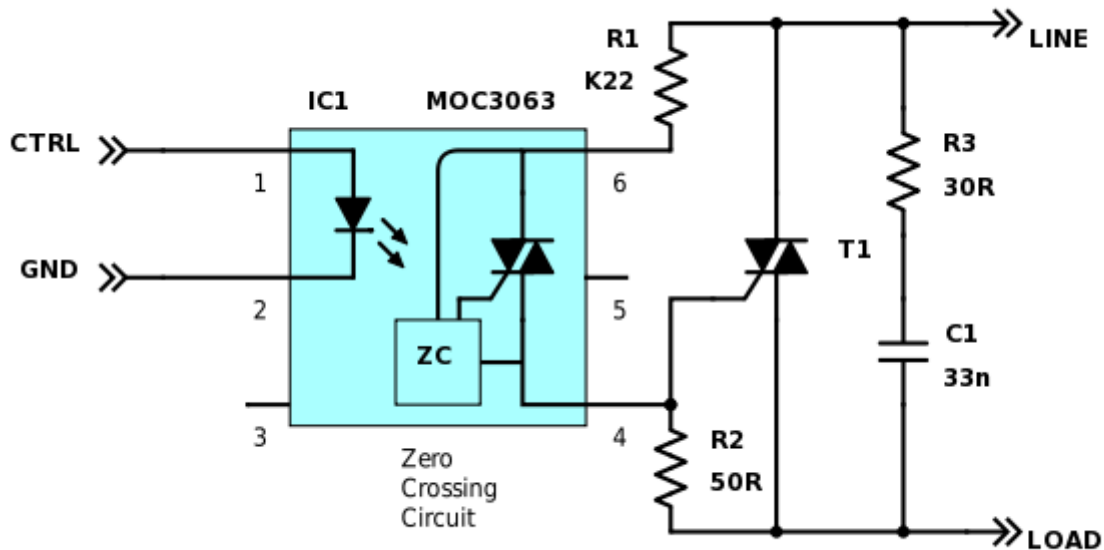


Figure 5. Power circuit

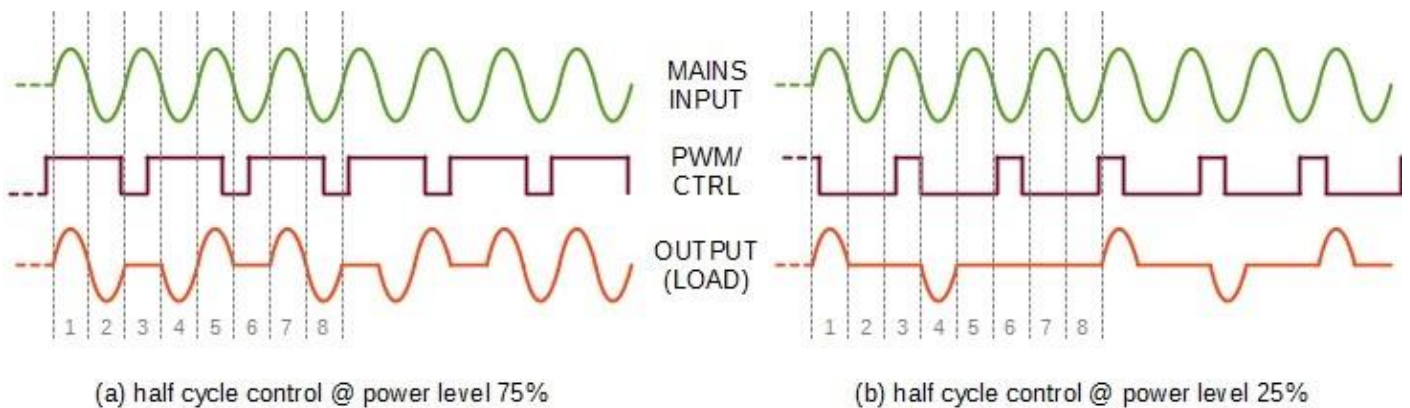


Figure 6. GreenPAK Half Cycle Control Waveforms

If CTRL is high at the zero-crossing moment (rising or falling), the MOC3063 will turn-on the triac switch for the following half-cycle.

We selected the SLG46220V for this project because it provides various options for setting the duty cycle. We chose to use an analog input, which is connected to Pin8. We used the PGA, ADC, and CNT2/DLY2 blocks to set up a PWM signal. The OSC block is set to 25kHz and its CLK/4 output drives CNT9/DLY9 which sets the PWM period to 28.16 msec. CNT2/DLY2 controls the duty cycle based on the ADC's output.

Other GreenPAK ICs may also be used to implement cycle stealing, although the design would be a bit different and some additional external components might be needed.

The control circuit we used is very simple, and GreenPAK is primarily used as a stand-alone PWM generator. Even though this design only covers unbalanced half-cycle control, it is applicable for certain loads, like thermal heaters. For full-cycle control, additional circuitry is needed to ensure that second half-cycle of the full cycle will not be skipped even if the PWM control signal is inactive at mid-cycle.

For a full-cycle control option, we can start from the same PWM control signal used for half-cycle control, and inhibit its application to rising (or falling) zero-crossings. The probability of the PWM signal being high or low at zero-crossing points is the same for both rising zero-crossings and falling zero crossings.

The skip percentage will be the same controlling full cycles at only rising (or only falling) zero-crossings or half-cycles at each zero-crossing. Note that this approach guarantees equal number of positive and negative half-cycles because they always go in pairs in one full cycle, thus no DC component will be introduced at the output.

Since rising and falling zero-crossings are the same for the MOC3063, we need to add a selector circuit. To select falling zero-crossings we can scale the mains voltage using the resistor divider and activate the Schmitt trigger option for the digital input pin. A schottky diode must be added to protect the input pin during the negative half-cycle. This additional external circuit is shown in Figure 7. After the Schmitt trigger action within GreenPAK, we get a signal STRIG that will go high shortly after rising zero crossing and go back low shortly before falling zero crossing.

When calculating the resistor values, voltage divider's ratio must be higher than V_{mhp}/V_{CC} , while lower than V_{mlp}/V_{sth} . V_{mhp} and V_{mlp} being the mains voltage peak values at high and low mains, V_{CC} being the GreenPAK power supply and V_{sth} being the HIGH-Level Input Voltage for Logic Input with Schmitt Trigger.

For $V_{mhp}=374V_p$ ($264V_{ac}$), $V_{mlp}=265V_p$ ($187V_{ac}$), $V_{CC}=5V_{dc}$ and $V_{sth}=3.333V_{dc}$ we get the divider ratio should be between 75 and 79, so 768K and 10K resistors are selected.

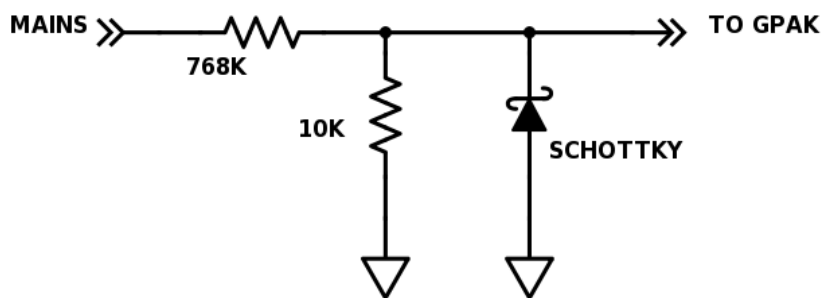


Figure 7. Zero Crossing Selector Circuit

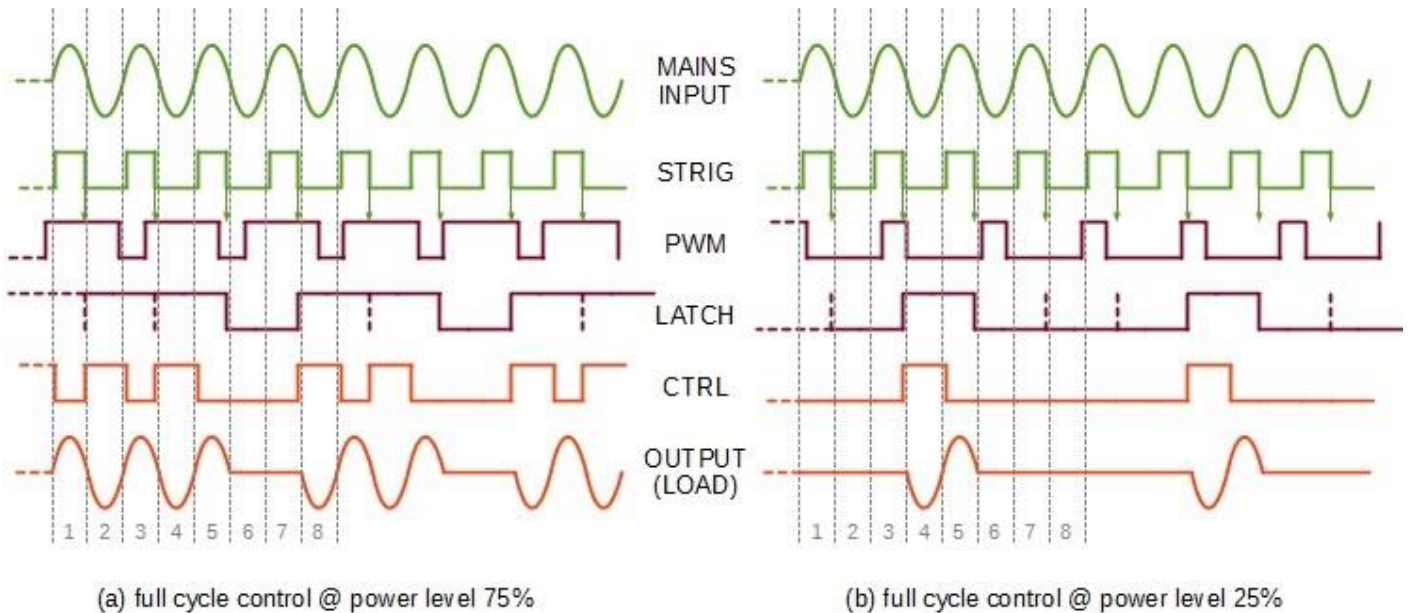


Figure 8. GreenPAK Full Cycle Control Waveforms

A falling edge of STRIG is used to latch the control signal for a full cycle, while a rising edge of STRIG is used to clear the control signal. Timing diagrams are presented in Figure 8 for two power levels: 75% and 25%.

Note that in the timing diagrams above, PWM period (“control period”) is set to 28msec, between one and two full cycles. That’s far away from 8 full cycles presented in Figures 1 and 2 in the introductory part of this app note. Selecting short PWM periods reduces flicker because the probability of sequential “off” cycles is lower than for longer PWM periods. Additionally, when using the internal GreenPAK oscillator to generate the PWM period, the oscillator frequency has both initial tolerance and drift. The longer the nominal PWM period, the bigger it’s total absolute deviation. At long PWM periods, the total deviation of the PWM period may approach the duration of the mains half-cycle and shift the PWM frequency to be synchronous with the mains frequency, so the skip percentage may only take integer values of fractions of the two frequencies thus making the control resolution finite.

Implementation of full-cycle control within GreenPAK adds just a couple of gates to the half-cycle design, as shown in Figure 9.

Half-cycle control signal is wired to Pin4, while the full-cycle control signal is wired to Pin8.

DFF0 latches the state of PWM signal at the falling edge of STRIG signal, just before the falling zero-crossing. INVO and 2-L0 resets CTRL at the rising zero-crossing.

Note that inverter INVO in the circuit above may be avoided by reconfiguring the external zero crossing selector circuit presented in Figure 7.

The design shown in Figure 9 sets the duty cycle of the PWM signal with an analog control voltage (e.g. from an external potentiometer).

Testing GreenPAK Design

We tested the design in two phases:

- 1) Design testing using GreenPAK Universal Development Board

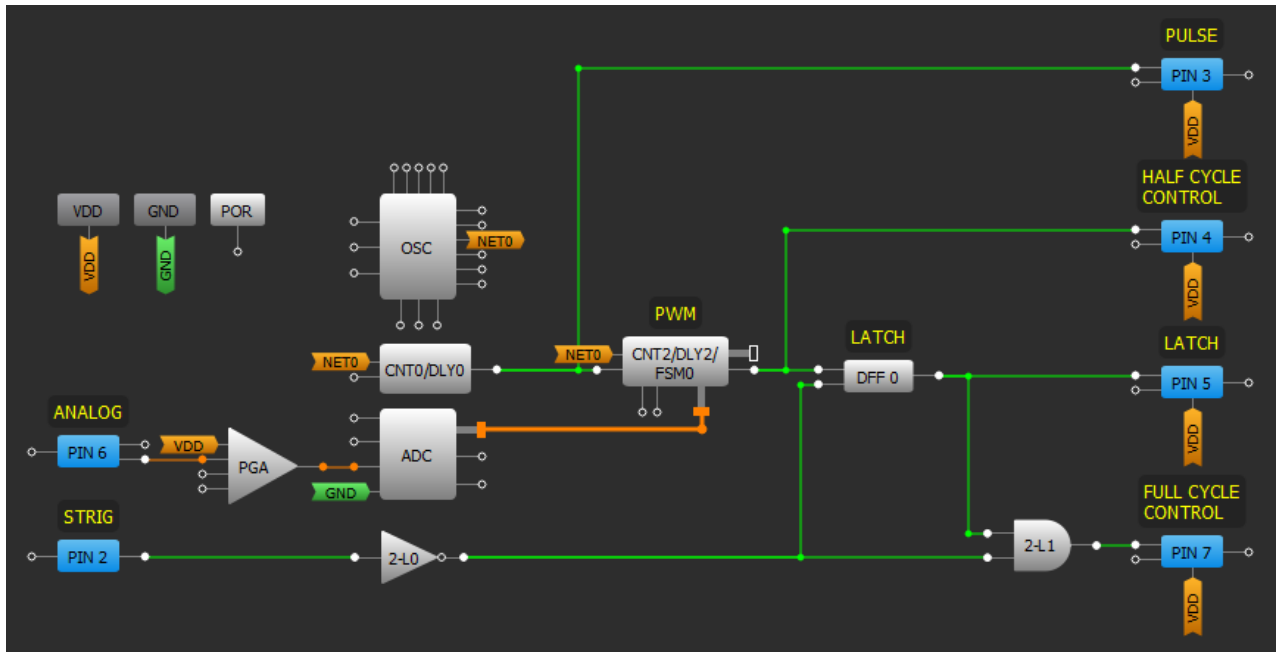


Figure 9. GreenPAK Design

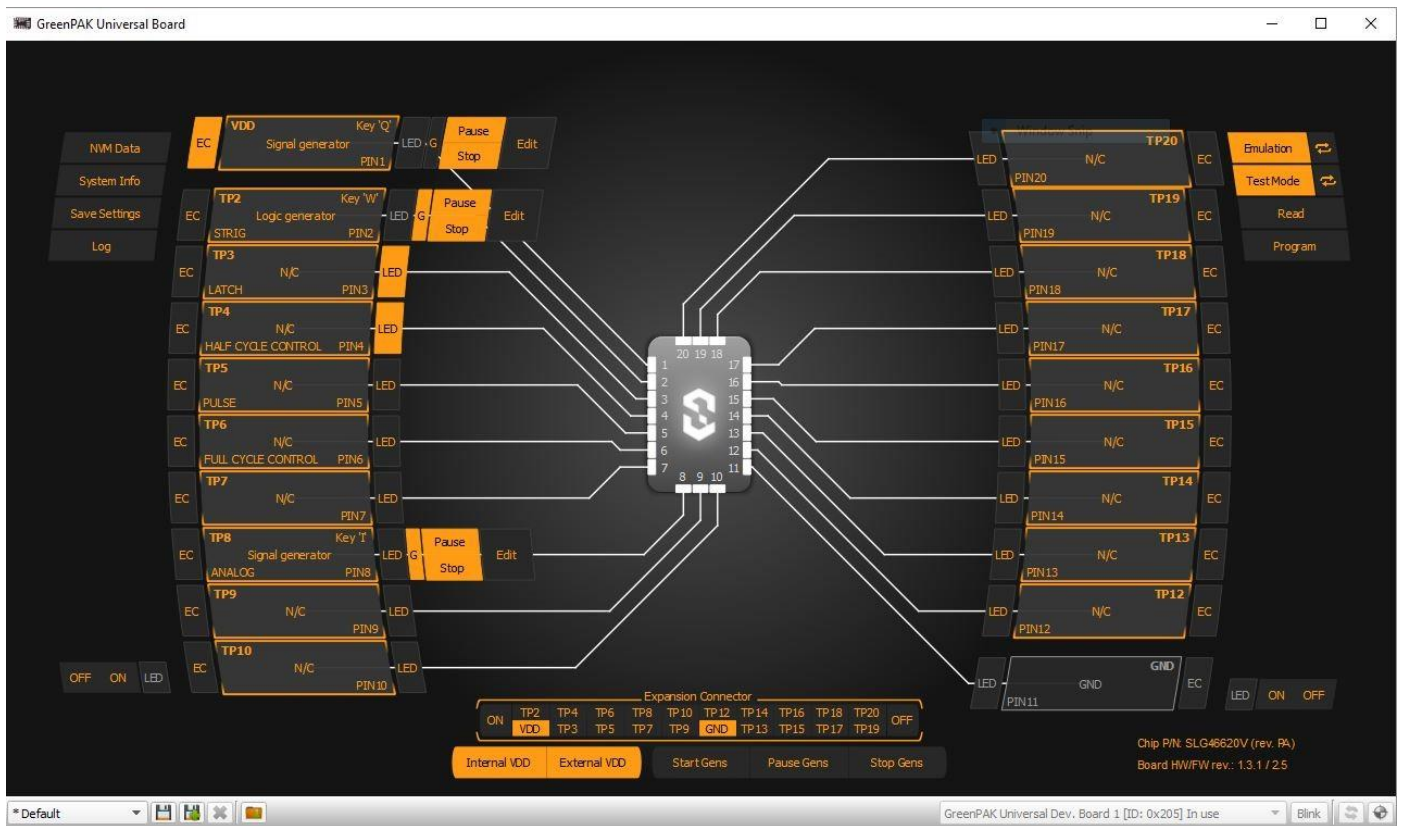


Figure 10. Emulator Setup

2) Final testing integrated with power circuit

We used the GreenPAK Emulation Tool included in GreenPAK Designer Development Suite to test the GreenPAK IC design. We created an Analog signal generator on Pin8 to simulate the analog input control signal. A logic generator was used to simulate STRIG input.

Internal signals are temporarily wired to free pins to make them accessible during testing, as shown in GreenPAK schematic presented in Figure 9. Pulse signal marking the beginning of the PWM period is wired to pin 5. Latch signal is wired to pin 3.

Control signals generated by the GreenPAK circuit are accessible on test pins of the GreenPAK Universal Development Board. All signals were inspected using external oscilloscopes and multimeters.

Final testing

For in-circuit testing, we assembled the power circuit on a breadboard and connected it to the GreenPAK Universal Development Board using jumper wires. A 4 kW resistive heater was used as the load.

Configuration for final testing is presented in Figure 12.

The first part of testing involved controlling the power delivered to the load using the control signal (either the GreenPAK Designer Signal Generator or an external potentiometer). Output power was monitored by measuring the RMS voltage at the load and the temperature of load. While RMS voltage reflected the changes in input control level instantly, temperature needed time to stabilize at the set level, as expected due to the thermal inertia of the heater.

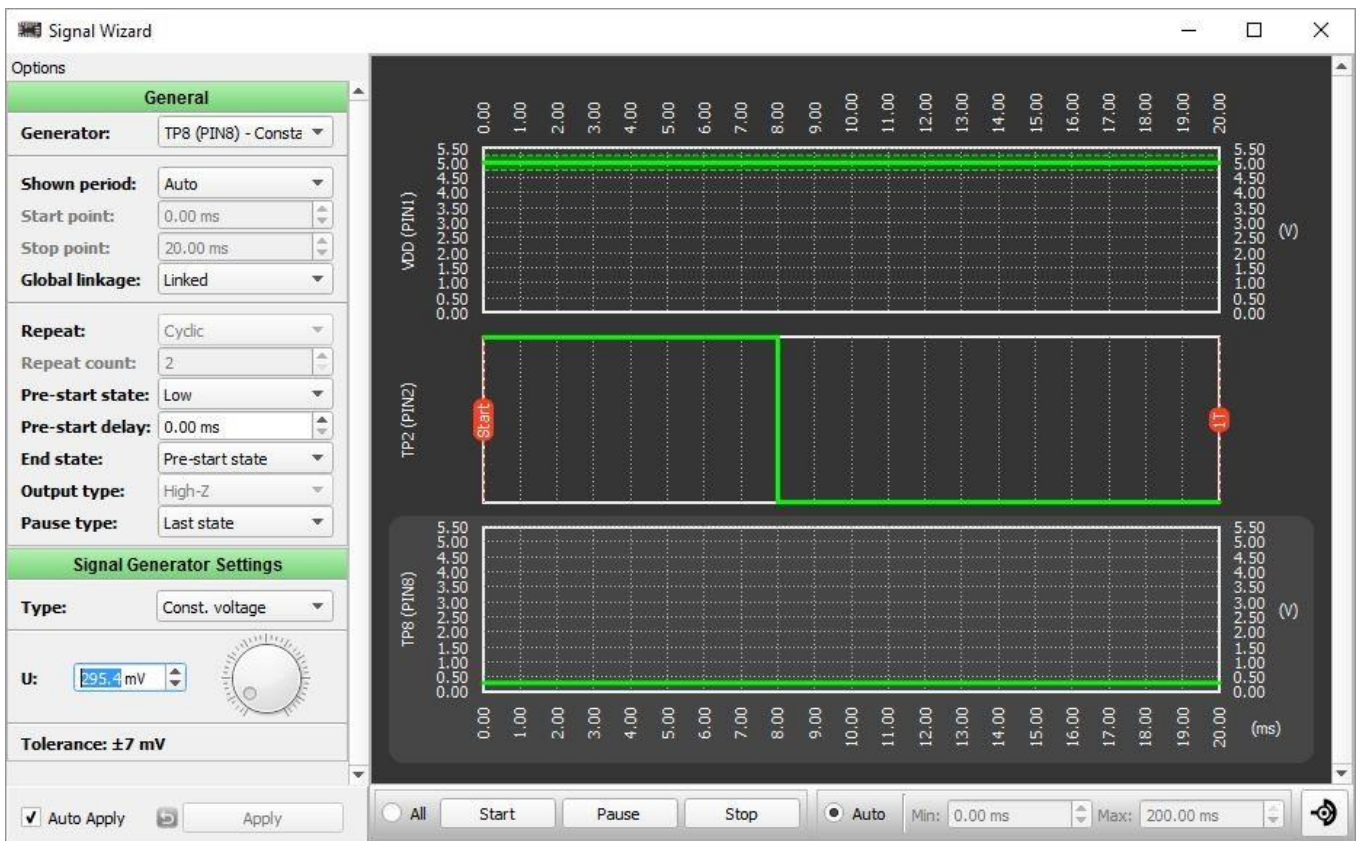


Figure 11. Generators Setup

The second part of testing included adding the temperature sensor to the circuit and closing the feedback loop to make the temperature regulator. A variac (variable autotransformer) was used to vary the input AC voltage. We monitored the output temperature to verify that the circuit was regulating the temperature within the full range of varying input voltage by skipping the right percentage of cycles.

At very low output power, the skip percentage would be very high and the load would get switched off for relatively long time periods, thus making the flicker problem hard to solve. At the same time, at very low output power, EMI issues with phase-angle method are minimized because the conducting angle is small and hard switching occurs at low voltage.

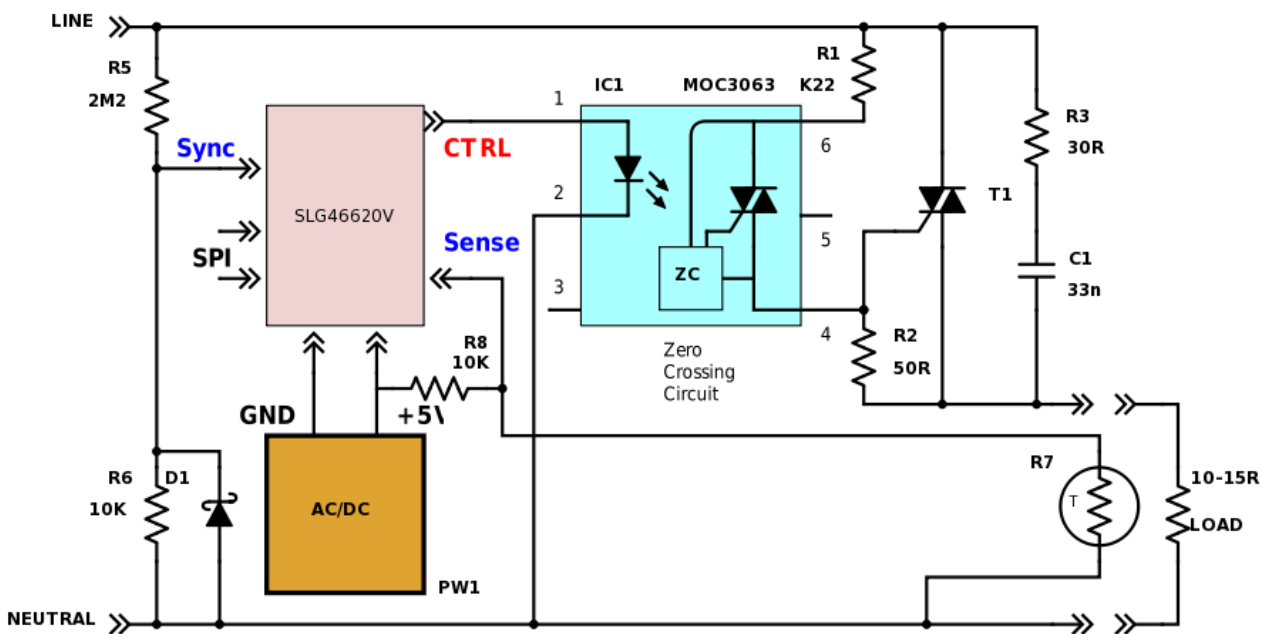


Figure 12. Final Testing Configuration

Extensions

Optional features may be added using surplus logic available in GreenPAK:

- 1) A soft start/soft stop circuit that increases gradually the output power at turn-on and/or decreases the output power at turn-off (fade-in/fade-out effect)
- 2) For some applications it might be interesting to set the minimum duty cycle (limit maximum skip percentage), below which output power goes to zero.

With the GreenPAK IC, there is a possibility to combine cycle stealing and phase-angle control methods in a combined method that unites the best features of both methods, reducing the EMI problems by cycle stealing at high power while avoiding flickering by phase-angle control at low power light dimming application.

Conclusion

We implemented a cycle stealing control system in a GreenPAK IC. The duty cycle of the GreenPAK's PWM output signal determines the fraction of the maximum load power. The control signal generated by the GreenPAK IC is used to turn on and off a power triac switch that is coupled to the AC line source such that the desired fraction of full load power is provided to the load.

This cycle stealing control scheme provides fine power control resolution without requiring a long control period. Furthermore, by shortening the control period, flicker due to pulsating AC line current is reduced.

The surplus circuitry in the GreenPAK can be utilized to implement additional features and functions in specific applications.

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