Application Note

Coulomb Counter

AN-1171

Abstract

This application note shows how to create a coulomb counter using a GreenPAK™ SLG46867V to measure the current drawn by a load.
This application note comes complete with design files which can be found in the References section.

Contents

Figures

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1 Terms and Definitions

GUI	Graphical user interface
P-FET	P-channel field-effect transistor
RS Latch	Set-reset latch

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/products/greenpak.

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-1171 Coulomb Counter.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

3 Introduction

This application note describes the creation of a coulomb counter to measure the current drawn by a load, where the measured current is represented in the time domain. To accomplish this, a GreenPAK™ SLG46867V with two internal 44 mΩ P-FET power switches are used.

4 Circuit Diagram and Timing Diagram

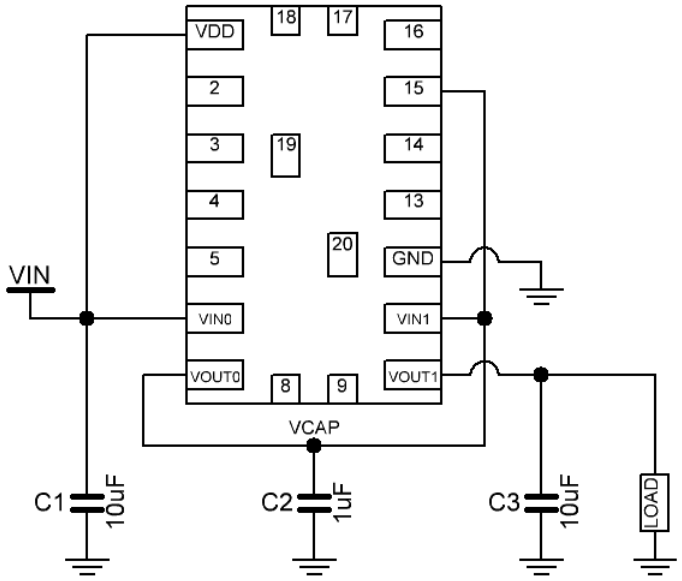

Figure 1: Circuit Diagram

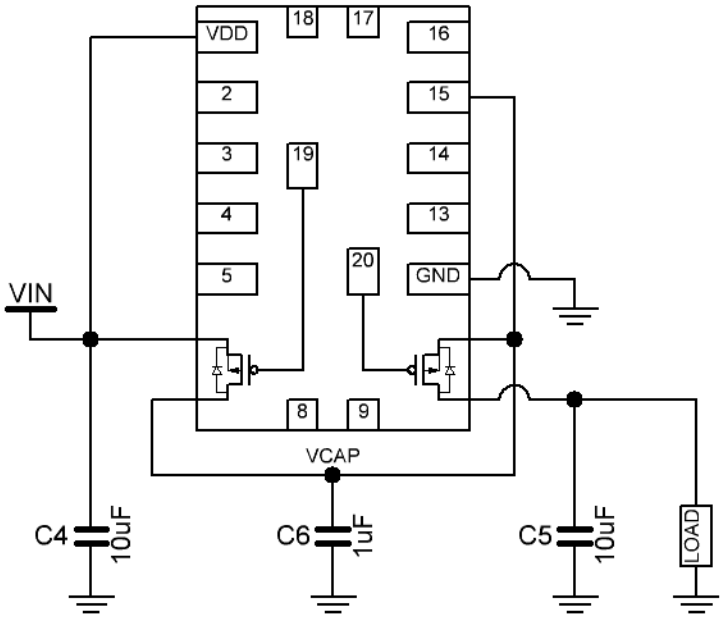

Figure 2: Circuit Diagram with Internal Connections

The switching capacitor, C2, see Figure 1 and Figure 2, charges and discharges. The length of time it takes for C2 to discharge is proportional to the load current. C1 is a decoupling capacitor for the GreenPAK SLG46867V power supply, and C3 is a decoupling capacitor for the output rail. This design is essentially a modified buck design that regulates its output rail to between 1824 mV and 2016 mV.

Figure 1 shows the pinout of the circuit with the power switch inputs and outputs labeled. Figure 2 shows how the power switches are connected inside the GreenPAK SLG46867V.

The timing signals for this design are shown in Figure 3.

Unlike some of GreenFET™ power switches, the SLG46867V's two internal 44 mΩ P-FETs are asserted active LOW, meaning that the P-FET will conduct when its gate is driven LOW. Likewise, when the gate is driven HIGH, the P-FET will not conduct.

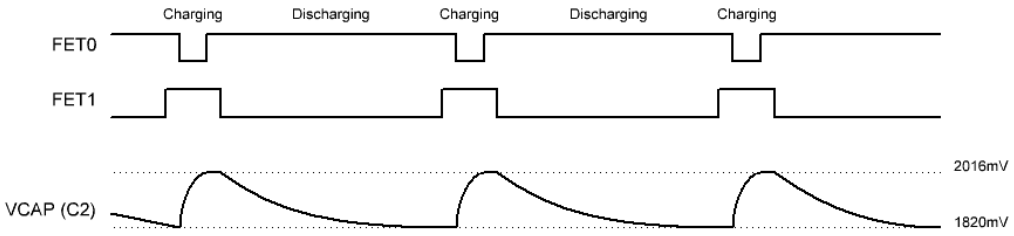

Figure 3: Timing Diagram

In order to prevent shoot-through timing protections are inserted into the GreenPAK SLG46867V design to ensure that both FETs will never be on at the same time. The technique used to prevent shoot-through is discussed further in Section 5.

5 GreenPAK Design

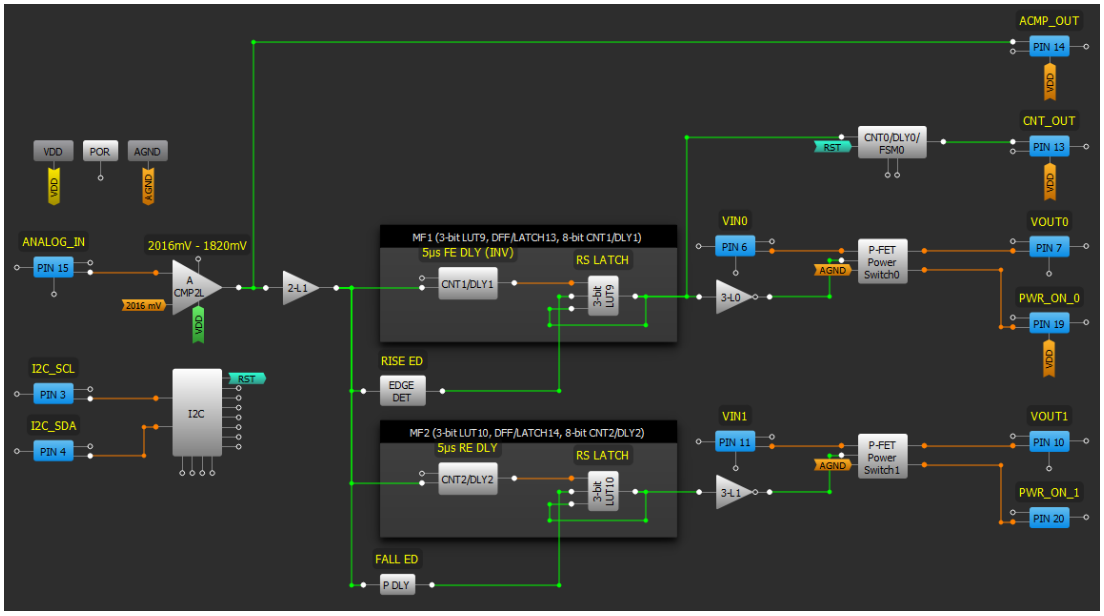

Figure 4: GreenPAK Design

Pin 15 (VCAP) of the GreenPAK SLG46867V is used to monitor the voltage at the top of C2, see Figure 4.

GreenPAK Designer software can be downloaded on the company website. Using the GUI of GreenPAK Designer set ACMP2L as shown in Figure 5:

1. Set ACMP2L V_IH threshold to 2016 mV.

2. Set Hysteresis to 196 mV to give a V_IL threshold of 1824 mV.

ACMP2L will output HIGH when the voltage at pin 15 raises above 2016 mV, and will stay HIGH until the voltage drops below 1824 mV. 2-bit LUT0 is used as a short buffer to give ACMP2L time to settle before affecting either of the switches.

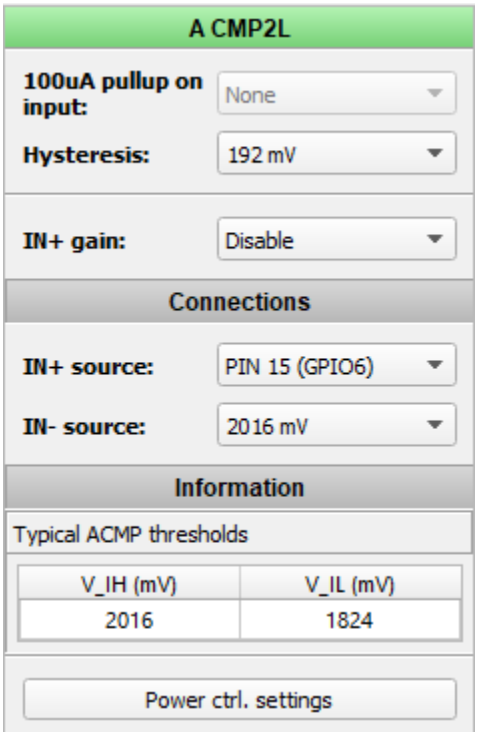

Figure 5: ACMP2L Settings

The timing protections to prevent shoot-through are created with two edge detectors and two multifunction blocks configured as a delay connected to a 3-bit LUT, see Figure 5.

If ACMP2L goes LOW, falling edge detector P DLY will output a short active HIGH pulse, which resets the RS latch in multi-function block 2 to LOW. Since the output of RS-Latch 3-bit LUT10 is inverted by 2-bit LUT2, it will drive the gate of P-FET1 HIGH, which will turn it off.

After 5 µs, CNT1/DLY1 will go HIGH, since it is configured as an inverted falling edge delay. This will set the RS-Latch 3-bit LUT9, causing it to go HIGH, see Figure 6. This signal is inverted by 3-bit LUT0, which drives the gate of P-FET0 LOW, which will allow it to conduct.

At this point FET0 is on and FET1 is off, so C2 is connected to VDD through FET0. It will charge up until ACMP2L registers that the voltage at the top of C2 has reached 2016 mV. When ACMP2L goes HIGH, the rising edge detector will reset the 3-bit LUT9 RS-Latch, turning off P-FET0. After 5 µs, CNT2/DLY2 will set the 3-bit LUT10 RS-Latch, causing P-FET1 to turn on. At this point FET0 is off and FET1 is on, so C2 is connected to the LOAD through FET1 and will begin to discharge.

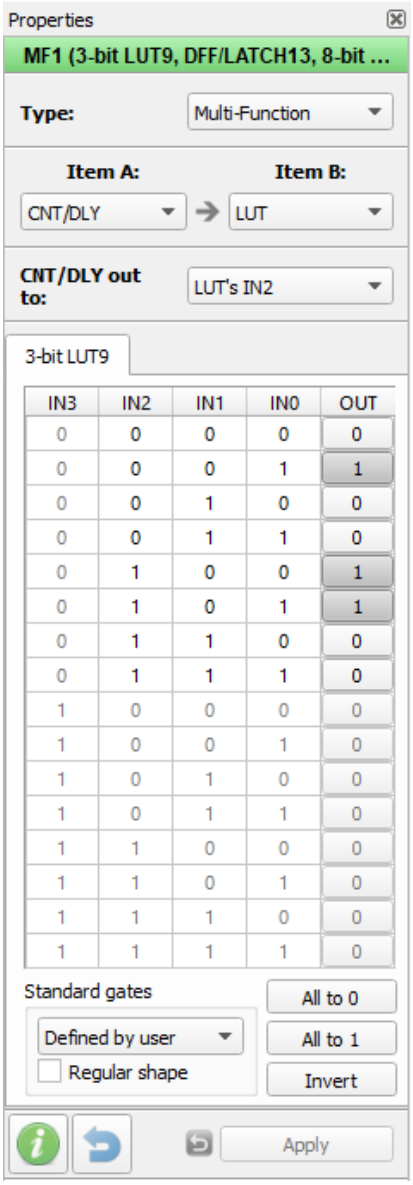

Figure 6: RS Latch Configuration

The coulomb counter information can be retrieved in a few different ways:

● Look at the raw output, the frequency of the FET switching, by watching pin 19 and pin 20.

● Receive a notification on pin 13 when CNT0 goes HIGH. Every time the system switches, the user-defined value inside CNT0 will be decremented. When CNT0 reaches 0, it will output HIGH for one clock cycle.

● Use an I2C read command to retrieve the count in CNT0 dynamically, then reset the counter with a pair of I2C write commands. In the commands below, [indicates a START bit, and] indicates a STOP bit.

- Read CNT0 MSBs: `[0x00 0xA6 [0x01 r`
- Read CNT0 LSBs: `[0x00 0xA5 [0x01 r`
- Reset CNT0: `[0x00 0xF4 0x01] [0x00 0xF4 0x00]`

6 Results

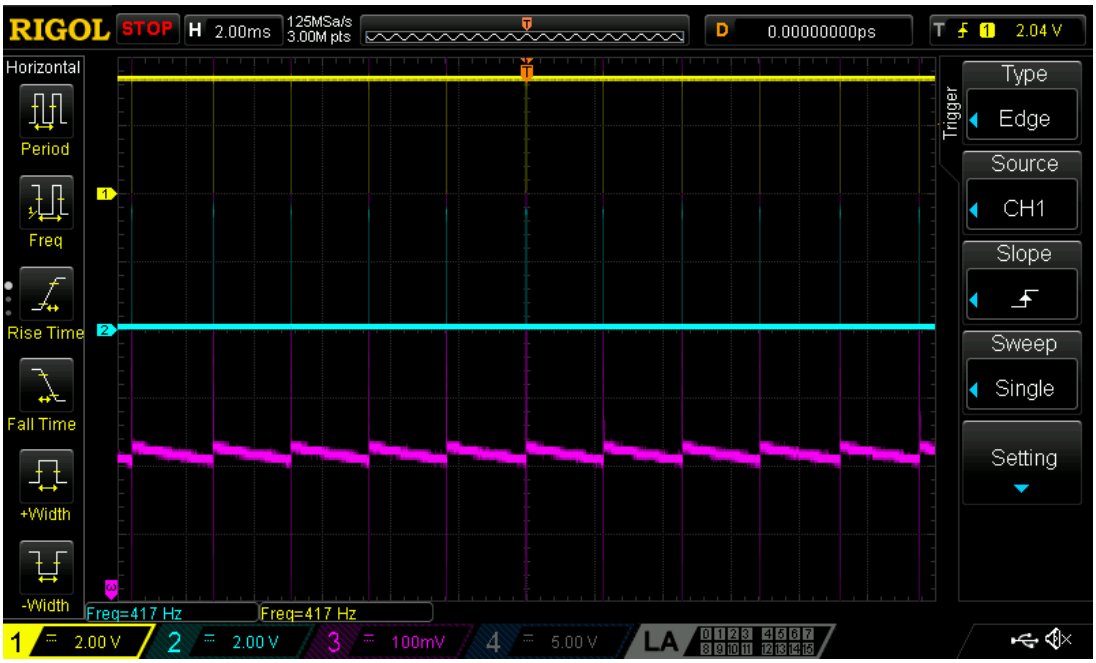

Figure 7: Operation at I_LOAD = 50 µA

Figure 7 shows operation when the load current is 50 µA. The oscilloscope channels are probing:

- Channel 1 (Yellow) – gate of FET0
- Channel 2 (Blue) – gate of FET1
- Channel 3 (Pink) – voltage at the top of C2

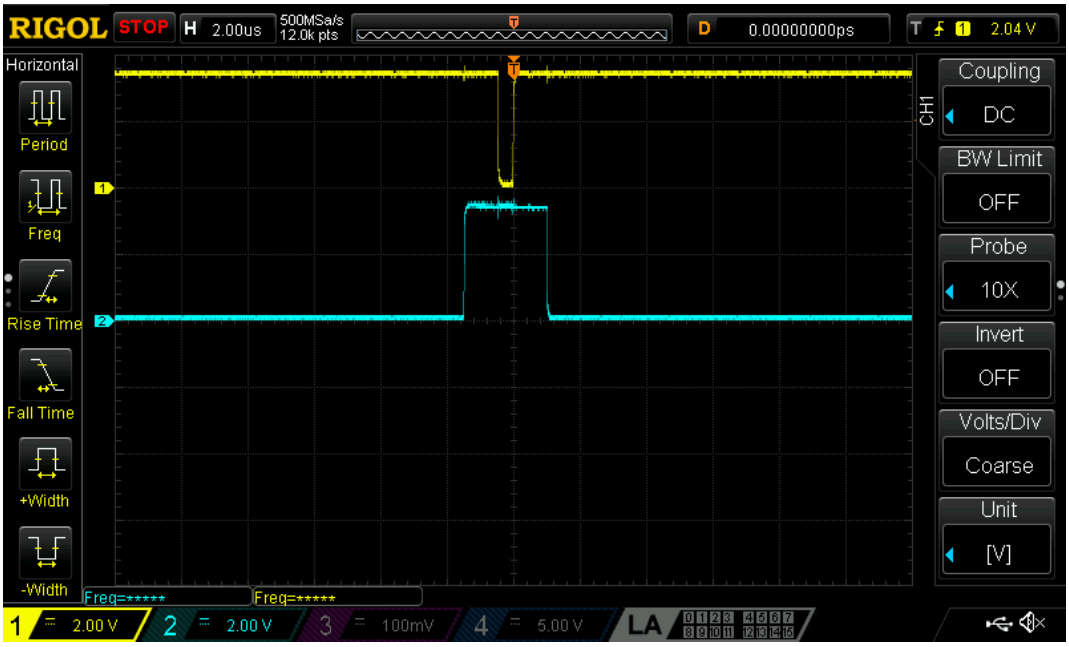

Figure 8: Gate Signals (Magnified)

Figure 8 shows a magnified view of the gate signals, both FETs will not be enabled at the same time due to the non-overlapping circuitry built into the GreenPAK design.

The raw output switching frequency was measured with various load currents, from 10 µA to 75 mA, see Table 1

Table 1: Load Current vs Switching Frequency

Load Current (µA)	Switching Frequency (Hz)
10	0.8
50	4.5
100	9
500	45
1000	90
5000	454
10000	909
20000	1800
30000	2750
40000	3600
50000	4550
75000	6630

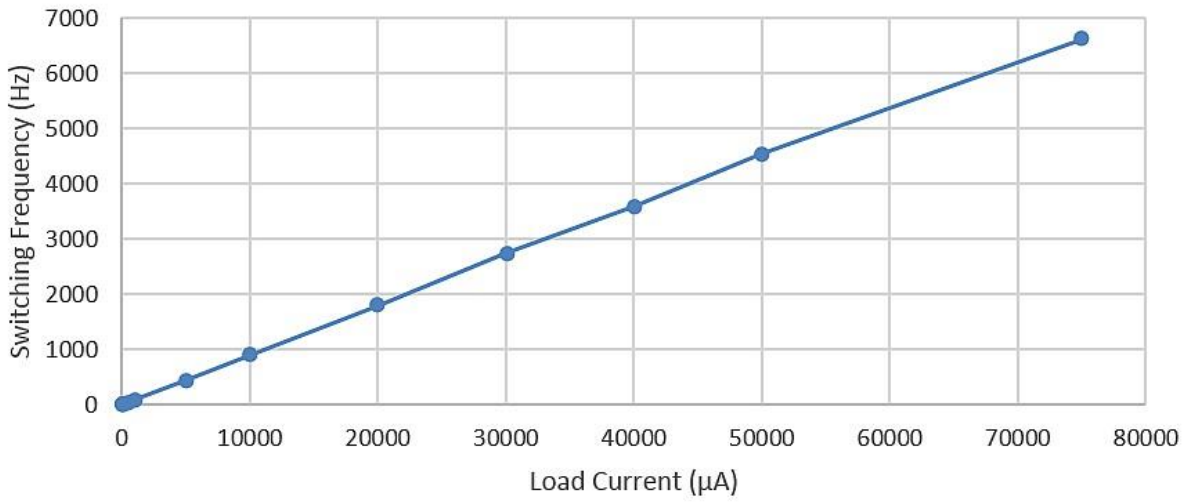

Figure 9: Load Current vs Switching Frequency, 10 µA to 75 mA

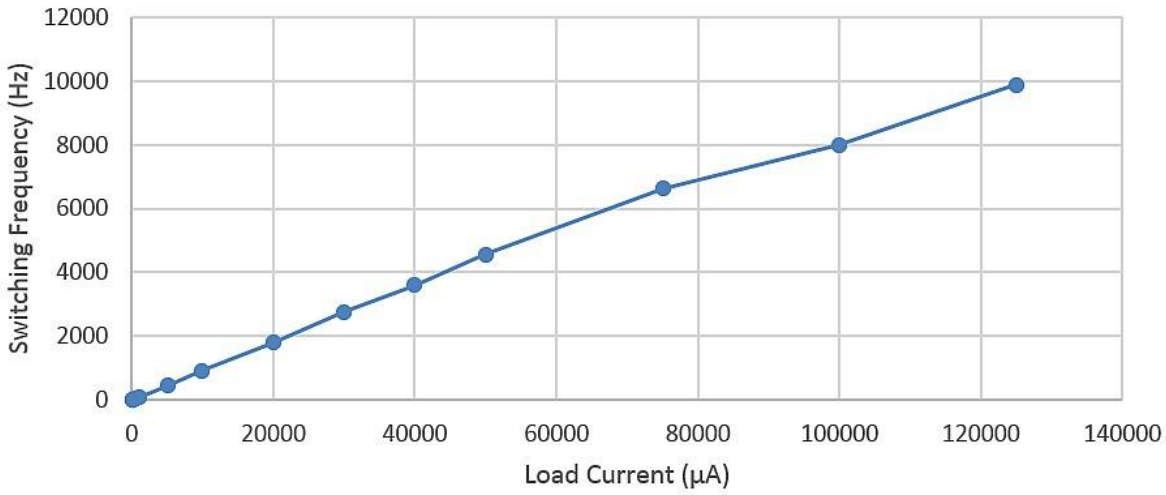

Figure 10: Load Current vs Switching Frequency, 10 µA to 125 mA

Figure 9 shows that the relationship between the load current and the switching frequency is reasonably linear from 10 µA to 20 mA. The relationship becomes less linear however around 100 mA, see Figure 10. This is because the switching capacitor (C2) is being discharged so quickly that the power switches are no longer able to switch fast enough to keep up with demand.

The size of the capacitors used in the coulomb counter may need to be revised according to the application. For example, to track load currents of greater than 100 mA larger capacitors for C2 and C3 are required. Smaller capacitors can be used to improve accuracy of lower load currents.

7 Conclusion

In this application note a coulomb counter was created, using a GreenPAK SLG46867V, that allows a user to monitor how much current their load circuitry draws. This coulomb counter behaves like a buck converter and regulates its output rail to 1824 mV to 2016 mV. With a 10 µF switching capacitor (C2) and a 100 µF decoupling capacitor (C3) on the load, this design's output frequency has a fairly linear relationship with the load current, from 10 µA to 75 mA.

Revision History

Revision	Date	Description
1.0	30-Jan-2018	Initial version

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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