AN-1202 A Boost Converter Design for Energy Harvesting Applications

Energy harvesting is a hot topic. In general the term refers to the harvesting of energy from ambient sources such as ambient light, radio waves, temperature differentials, human or vehicular motion, or sound. With advances in low-power electronics, it has become meaningful to think of powering low-power devices by harvesting such energy. The evolution of supercapacitor (ultracapacitor) technology has provided us with a handy tool to capture such energy. In this Application Note we propose an energy harvesting solution using a supercap that minimizes or eliminates the use of batteries in low power applications such as electronic door locks or data loggers. The design utilizes a GreenPAK™ programmable mixed-signal ASIC as the primary control element. The solution we propose serves a dual purpose in that it also demonstrates how to use a GreenPAK device to design an inductor-based boost converter.

Though the proposed design is based on the standard single-inductor boost converter topology, there are some clear advantages in using the GreenPAK approach compared to using a standard off-the-shelf converter IC. For one, we may integrate the solution with other circuit functions – related or unrelated – in the same IC. Secondly, we can customize the solution by incorporating context-specific control mechanisms in the same GreenPAK chip such as those for supercap overvoltage protection and cell balancing. Thirdly, the inherent design flexibility can be exploited; for example, in the context of energy harvesting, we can design such a solution to work with input voltages less than the typical minimum (~1V) encountered with off-the-shelf ICs.

Broad Design Strategy

In this Note we consider the case of a load requiring a 5V supply. The load may be constant (such as a data logger) or one that requires intermittent bursts of power, such as an electronic door lock [2]. We will explore the impact on the design in the latter case. The overall hardware schematic is shown in Figure 1. Gen1 represents the energy source being harvested. (Note that multiple energy sources can be paralleled though their respective diodes.) We start with providing an overview of the various ingredients required for a practical design and how they work.

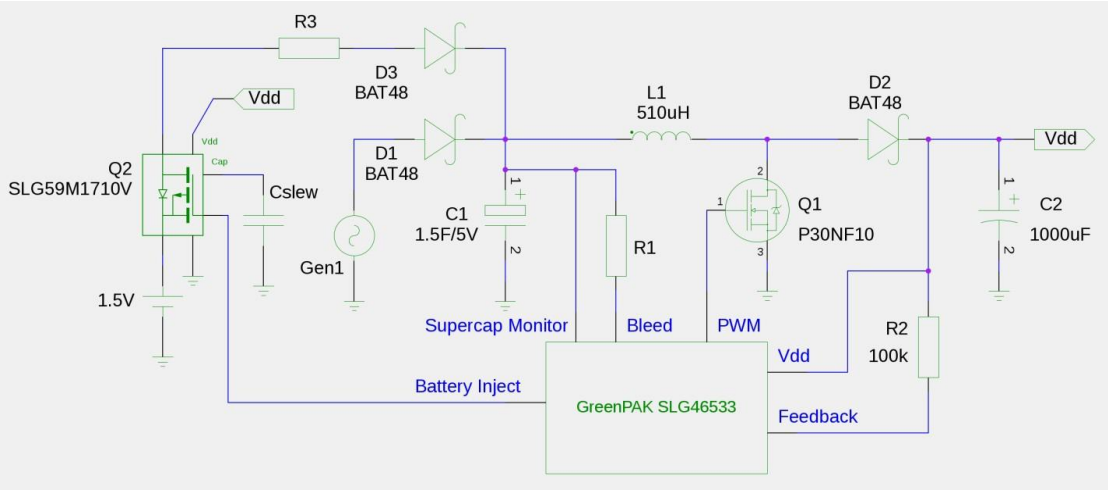

Figure 1. Overall hardware schematic

Energy storage. The design revolves around a single supercap of 1.5F. Supercaps are available with ratings of 2.7V as well as 5V. 5V versions are available without a balancing terminal, making design easier. In our tests we used one from Bussman's PowerStor range which has no balancing terminal.

In the context of harvesting, the topic of maximum power transfer gains importance. A harvesting generator such as a solar panel or piezo generator is usually not affected by output shorts, so one simple strategy is to simply connect a supercap across the generator [3]. This may not result in maximum power transfer, especially when the supercap is completely discharged and presents a virtual short, causing the output to fall to close to zero. However it is simple to implement and universal in application, for two reasons:

- the MPPT point is not necessarily at a voltage that is half of the generator output
- the generator may provide sharp spikes of energy making maximum power transfer tracking difficult or impossible

Therefore, in this Note we propose to go with a supercap that is connected directly across the generator. This also has the advantage of requiring a smaller supercap bank as described below. Note that while a single diode at the input suffices for solar panels, a bridge is more appropriate for ac generators.

Supercap sizing and overvoltage protection are important design considerations. On the one hand the supercap must be large enough to store energy enough to power the load for as long as the generator is inactive. On the other hand, when the generator is active, we must discard excess energy when the supercap is fully charged to prevent overvoltage faults.

DC-DC conversion. The design presented in [2] uses a boost converter to boost the generator voltage to a value that is required by the door-lock opening circuitry and charges a supercap bank to this target voltage. Where the target voltage is greater than 5V, as is often the case, this has the disadvantage that we need to place multiple supercaps in series. Another approach is to place the supercap at the input stage as discussed above, and let it charge to a lower voltage, powering a downstream boost converter. This will result in a smaller supercap bank. In this Note we adopt the latter approach.

In general, DC-DC conversion can be accomplished by using capacitor-based charge pumps or inductor-based converters. If one is looking only for boost conversion then an inductor-based method is a bit simpler, requiring only one stage of conversion. A capacitor-based solution requires two stages: a charge pump that will boost the input by a multiple of 2, followed by a PWM-based buck stage to get to the target voltage (the so-called regulated charge pump). Traditionally inductors are frowned upon due to their bulk, but the fact that we are dealing with relatively low currents reduces the bulk and cost and makes them attractive to use. Further, inductor-based converters are capable of higher output currents [1], and therefore more suited when current bursts significantly above the average consumption are expected such as in a door lock.

In inductor-based converters, the MOSFET switches usually need to handle voltages that may be higher than the target output voltage. They also need to have switching times that are small compared to the switching pulse width. Additionally, we need a MOSFET that exhibits low on-resistance. The MOSFET in Figure 1 is a commonly available low-cost type that fits the bill.

Voltage regulation. Voltage regulation at the output can be achieved by a GreenPAK that controls the duty cycle of the MOSFET based on feedback from the output.

Duty cycle bounding. Note that unlike a capacitor-based converter, in an inductor-based boost converter it is important to ensure that the MOSFET's drive is never taken to 100% duty cycle which would cause the MOSFET to settle into a state of continuous conduction. This would simply discharge the supercap without providing any boost! This means we need to sense the duty cycle when it approaches 100% and prevent it from increasing further.

Low-voltage detection. Once we have determined the duty cycle limit, it may appear from standard converter design math that we can calculate the corresponding [lowest possible] input voltage below which the boost conversion may not work effectively. This is possible in principle but there are practical difficulties when the load current may vary widely as in a door lock, and is also problematic because of component tolerances, stray resistances, parasitic capacitances etc. We

need a run-time test for low voltage.

Once we have been able to detect a low voltage, we may have several choices such as the following; what choice is correct of course depends on the context of the application.

- provide an external signal to the device being powered so that it can take suitable action such as going into a low-power state
- turn off the PWM oscillator to bring down power consumption of the GreenPAK device
- switch from supercap to battery as the power source

Secondary battery support. In some situations it makes sense to have a battery as part of the solution, designed to kick in and deliver a small dose of charge to the supercap when required. A simple candidate scheme of things is illustrated in Figure 1, consisting of GreenFET Q2 controlled by the GreenPAK. Note that the battery feeds into the supercap just as any other harvested energy source would; R3 is used to limit the maximum current and depends on the battery type. Battery support can be configured in several ways; we list a couple of them here:

- have the battery kick in at a voltage *higher* than that which triggers the low-voltage detection described in the preceding para. In this case the low-voltage indication happens only when the battery has finally started to die, and effectively becomes a low-battery indication
- have the battery kick in at a voltage *lower* than that which triggers the low-voltage detection. Here the intent is to allow the device being powered to go into a low-power mode but prevent it from dying altogether if the harvested energy source does not become available for an abnormally long time. This strategy is suitable for example if the device being powered can continue to work – as the GreenPAK can – with voltages that are significantly lower than the nominal Vdd of 5V.

Realization in the GreenPAK Designer

Figure 2 shows the design realized using SLG46533V. We now explain how each of the design ingredients is realized in the Designer.

PWM Operation. The 2MHz output of the OSC block is used for the PWM signal generation in the manner described in Application Notes AN-1117 and AN-1122 – albeit with some minor modifications to suit the present context – so we will only provide a brief summary of the operation here and refer the reader to the detail in those Notes.

The CNT2 and CNT4 blocks, whose data is set to 50, generate SET and RESET signals every 50 clock pulses which feed the SR Latch LUT1 to generate a rectangular PWM waveform; a SET causes the output of LUT1 to go high and a RESET causes it to go low. The period of the PWM waveform is the clock frequency divided by 50, which in this case is 40kHz. When the pulse width (duty cycle) needs to be increased, the DOWN/nUP signal goes low, and this causes the SET signal to occur earlier, thereby increasing the duty cycle. Conversely, when the DOWN/nUP line goes high, the RESET signal occurs earlier, causing a reduction in the duty cycle. The DOWN/nUP signal is derived from ACMP2 which monitors the chip's Vdd. The purpose of CNT0 is to specify a PWM duty cycle update frequency that is slower than the rate of the SET/RESET pulses. The counter value may require some experimentation depending on the load value; values between 2 and 10 are usually effective. For more detail on the working of the basic PWM engine the reader may refer to AN-1117 and AN-1122.

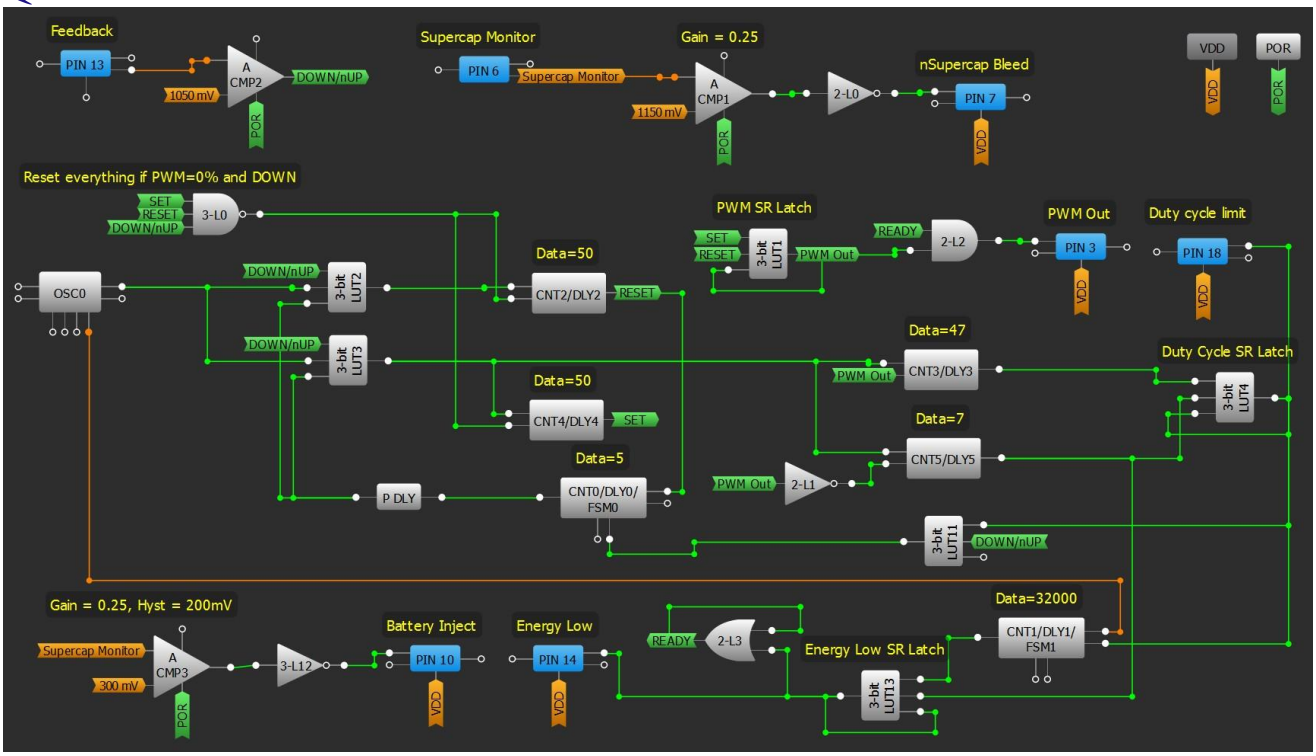

Figure 2. GreenPAK design with SLG46533V

If the SET and RESET signals overlap then the duty cycle is zero. At this stage, we need to check whether this happened because the duty cycle progressively reduced to zero, or whether it progressively increased to 100% and caused an overflow. In our design we have an explicit bounding mechanism on the duty cycle and so the 100% check is not required. Given this, the only other possibility is that at the instant that the SET and RESET signals overlap, the DOWN/nUP signal is high. Then the duty cycle must be held at zero; this is sensed by L0 which disables the PWM and resets the PWM engine.

Duty cycle bounding. Suppose we have decided that the duty cycle should not exceed 95%. The PWM waveform can have as many clock pulses as the Data field of CNT2/CNT4, which means we want to sense a width that is longer than 47 clock pulses. This is accomplished by feeding the PWM signal to DLY3 that has Data=47 and is configured to delay the rising edge. Therefore DLY3 acts as a filter, and as soon as the positive pulse is longer than 47 clock pulses, the delayed rising edge appears on the output and toggles the SR latch LUT4. At this point, if the DOWN/nUP signal is low, then the system is trying to further increase the duty cycle. LUT11 outputs a high and freezes CNT0 (which is responsible for updating the duty cycle) so that the duty cycle cannot increase further. Conversely, DLY5 acts as a filter for detecting when the duty cycle falls to below a set threshold; in the given design, DLY5's Data value is 7, so when the nonpositive pulse of the PWM cycle is longer than 7, a positive pulse is sent to LUT4's reset input which toggles its output to low, and CNT0 resumes normal operation.

Low energy indication. The boost converter tends to work not by providing a stable PWM waveform but by supplying a PWM range. This is due to the fact that ACMP2 is equipped with a 25mV hysteresis which translates to a 0.1V hysteresis at the input. The effect of this hysteresis is that the system cycles between these two hysteresis points constantly. During the upward journey the PWM duty cycle keeps increasing and during the downward journey it keeps decreasing. What happens at lower supercap voltages is that the duty cycle may hit its upper bound during the journey towards the upper hysteresis point, but then once this point has been reached the duty cycle may be reduced as it begins journeying towards the lower hysteresis point. Therefore we need to check if the duty cycle has stayed at its upper bound for a long enough interval to conclude that the supercap voltage is indeed too low to sustain the current load. We do this using DLY1 which is configured as a 1-second rising-edge delay (Data=32000). When the duty cycle has stayed

continuously at its upper bound for this period without recovering, DLY1 outputs a pulse that sets the output of SR Latch LUT13. This output can be used as a signal to effect the low-energy actions listed earlier such as indicating to the device being powered that it should go into low-power mode or switch to a battery backup. When the duty cycle eventually recovers (because, say, harvested energy charges the supercap) then the edge produced by DLY5 resets LUT13 signaling that harvested energy is available again.

Secondary battery support. ACMP3 is designed to be an independent add-on piece to the Designer schematic. A simple rule is used to decide when to turn on GreenPAK Q2 to embellish the energy input: with the IN- and hysteresis values shown, this happens if the supercap voltage falls below 400mV, at which point Q2 is turned on via a high output on the Battery Inject pin. Once this happens, ACMP3 keeps it on till the supercap has charged to 1.2V.

Supercap overvoltage protection. Supercaps must be protected against overvoltage. This is accomplished quite simply by using ACMP1 whose output goes low if the supercap voltage exceeds a predefined value, say 4.5V for a 5V capacitor. When that happens, a bleed resistor appears across the supercap and keeps it from overcharging.

Aside: A DCM Approximation for Energy Harvesting

The boost converter topology we use is quite standard – the detailed math for the general case may be found at [5]. The inductor in such converters can operate in two modes – continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In CCM mode, the voltage ratio between input and output is dependent only on the duty cycle and not on the load. The relationship is given by Vo/Vi = D/(1-D). However CCM requires much larger inductance values, and happens only above a critical current. The minimum inductance required for CCM is given by

$$L_{\min} \geq \frac{V_O \times T_S}{16 \times I_{O(crit)}}$$

where Vo is the output voltage, Ts the time period of the PWM waveform and Io(crit) is the minimum load current at which we would like to have CCM. In the present design the the PWM is at 40kHz. If we desire CCM at 15mA, we need an inductance of at least 520uH, and at least 780uH at 10mA. Clearly in low-power energy harvesting applications, we must usually expect to design for DCM. This must be borne in mind when looking up online calculators for inductor-based converters such as the popular one at [4]; clearly the calculator is intended for CCM operation and can therefore be quite misleading!

With DCM the voltage ratio depends on the load as well as the duty cycle. The precise formula in the DCM case is given by [5]:

$$V_O = V_I \times \frac{1 + \sqrt{1 + \frac{4 \times D^2}{K}}}{2}$$

Where K is defined as:

$$K = \frac{2 \times L}{R \times T_S}$$

Here Vi is the input voltage and R is the load resistance. In passing let us derive a useful approximation for the case where the input voltage is low and the duty cycle is close to unity. This corresponds to our Low Energy case in our design. Such an approximation can be useful to understand the broad behavior of the converter at critical moments.

In the present design, Ts = 25uS and L = 0.51mH so K ~40/R. If R >1k ohm, as we could expect in many low-power energy harvesting applications, then K < 0.04 and √K < 0.2. Applying these

approximations, (2) simplifies to:

$$V_o \approx \frac{V_i D}{\sqrt{K}}$$

Test Results

Since the generator is directly coupled to the supercap, the precise nature of micropower generation is not relevant; what is more relevant is to study the effect of load bursts on the system. For example, a door lock may consume only a few microamps when idle but will typically consume 15-20 mA for 5-6 seconds when operating the lock [2]. In lab tests with the component values shown in Fig 1, the circuit, with an initial supercap voltage of 3.5V, was able to supply 20mA at 5V for 35 seconds before the output voltage dropped momentarily to below 4.75V at which point the emulation was specified to stop. Line regulation was good – the output voltage variation between no-load and 20mA load conditions was less than 2%.

Cautionary note: output overvoltage. In an inductor-based boost converter that has not been designed optimally, there is a likelihood of the output voltage shooting beyond the target Vdd value. We do not want to use a Zener diode across the output because that would mean wasting precious harvested energy! Rather, it is more prudent to examine the reason for overvoltage from first principles and address them through preventive measures in the design. It is also important to prevent spurious or false PWM pulses for the same reason. In tests of the given design we observed that the propensity for overvoltage occurs most commonly in two situations:

- during start-up under no-load conditions
- when load is suddenly disconnected (such as the door lock solenoid being deactivated).

The important parameters that govern behavior in these situations are the Data value for CNT0 which govern the PWM update rate and the Data values for CNT3/CNT5, and these must be experimented with for satisfactory results.

It was also during emulation that any delay in the starting up of ACMP2 caused a false PWM pulse to appear at the output though Vdd was already at its target value and this caused the voltage to shoot further to abnormal levels. L3 and L2 prevent this by waiting for the duty cycle to hit its limit and stay there for a second before gating the PWM output via the READY signal.

In passing note of course that the GreenPAK device as well as Q2 are powered by the output of the converter itself. During emulation or deployment therefore, one must initially charge the output capacitor to 5V and then start up the system.

Conclusion and Extensions

Several extensions are possible to the design proposed in this Note. In general it is conceivable that the generator voltage may be higher or lower than the desired output voltage at various times. Therefore we can create a more general design by having a buck-boost converter rather than just a boost converter. As a more sophisticated option we can also look at the slightly less common (but more capable in some ways) SEPIC topology for the buck-boost converter. Another extension would be to leverage the harvested energy when the supercap is fully charged to charge a battery rather than bleed it away.

References

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↑ 3. Pierre Mars, "Coupling a supercapacitor with a small energy-harvesting source," EDN, June 7, 2012.

↑ 4. https://learn.adafruit.com/diy-boost-calc/the-calculator. Retrieved 25th Sep 2017.

↑ 5. Texas Instruments, "Understanding Boost Power Stages in Switchmode Power Supplies," Application Report SLVA061, March 1999

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