INTRODUCTION TO MULTI-PORT MEMORIES

APPLICATION NOTE AN-253

By Cheryl Brennan

What is a multi-port SRAM?

A multi-port is a static RAM with a dual-port or multi-port cell. Each port has separate address, data and control signals for accessing a common SRAM array.

How many transistors does each cell have?

IDT dual-ports typically use six transistors and two resistors per cell. Figure 1 depicts IDT's standard SRAM cell. It is a four transistor cell with high impedance pull-up resistors to provide the proper circuit biasing. Figure 2 depicts the configuration of IDT's dual-port SRAM cell. This canbe described as a standard four transistor memory cell with two additional transistors to provide an additional access path to the cell for both ports.

Figure 3 shows the configuration of IDT's FourPort SRAM cell. There are an additional four transistors. This allows up to four devices to access the memory simultaneously.

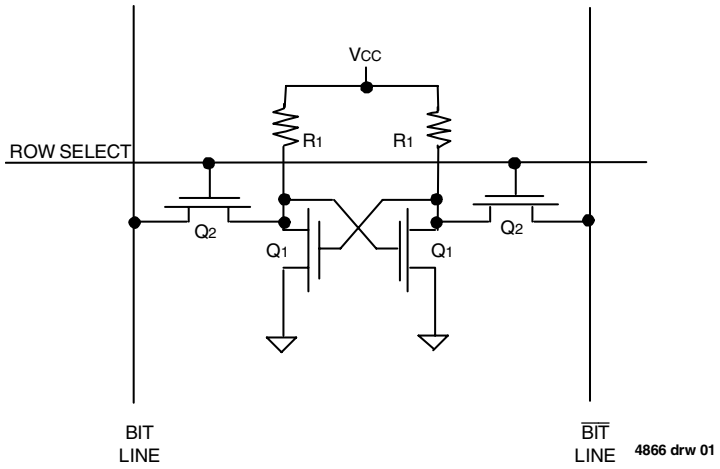

Figure 1. Standard Four Transistor Two Resistor Memory Cell

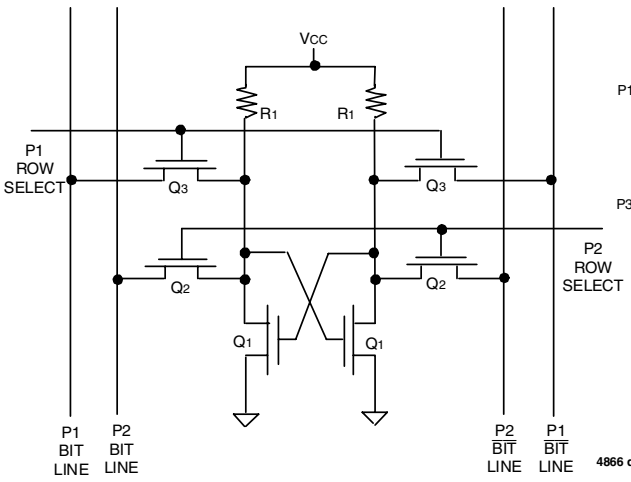

Figure 2. Dual-Port Memory Cell

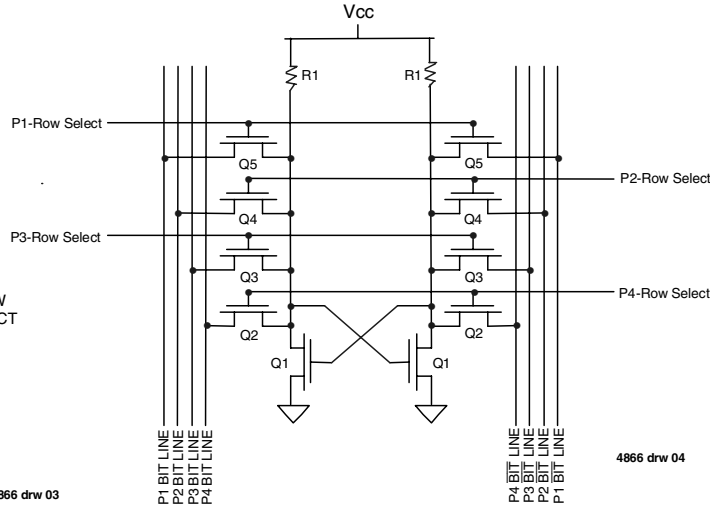

Figure 3. A Simple Example of a FourPort™ SRAM Configuration.

MARCH 2000

What are the different types of multi-port memories available?

- Asynchronous Dual-port SRAMs
- Synchronous Dual-port SRAMs
- FourPort™ SRAMS
- SARAM™ (Sequential Access Random Access Memory)
- Bank-Switchable™ Dual-port SRAMs

What are the differences between these various Multi-Port memories?

Asynchronous Dual-ports SRAMs—These dual-ports respond to address and control pin changes without the need for clocks or counters. These devices allow simultaneous access to a single static SRAM memory location from two busses. Refer to Application Note AN-91, "The Most Commonly Asked Questions About Asynchronous Dual-Ports." Most asynchronous dual-ports have arbitration logic.

Synchronous Dual-ports SRAMs—As the need for bandwidth has increased, there became a greater demand for faster internal operating speeds in dual-ports. The solution was introduced by IDT in 1992. The synchronous Dual-Ports use external clocking and internal counters to allow designers to run at faster speeds than that which can be achieved from standard asynchronous dual-ports. These dual-ports respond synchronously to address and control pin changes in relation to a clock edge. These devices allow simultaneous access to the same location in memory. IDT has two different options available on most synchronous dual-ports, Pipelined and Flow-through. The Pipelined option provides the highest bandwidth. The Flow-through synchronous option is used by designers who want the ease of integrating a synchronous dual-port in their synchronous system design. Additionally, we offer two different pinout architectures of the IDT synchronous dual-ports. In 1999 IDT introduced a 133MHz synchronous dual-port. In order to achieve the 133MHz performance it was necessary to interleave the I/O pins. For more information on the issues above refer to Application Note AN-254, "The Most Commonly Asked Questions About Synchronous Dual-Ports."

FourPort™ SRAMs—These devices need similar to the standard Asynchronous Dual-Ports. These devices allow simultaneous access to a single static SRAM from up to four processors. There are no clocks or counters needed. Most asynchronous dual-ports have arbitration logic. Refer to Application Note AN-91, The Most Commonly Asked Questions About Asynchronous Dual-ports.

SARAM™—The SARAM™ is a Sequential Access Random Access Memory. This device that allows the designer to bridge the asynchronous and synchronous components of a system design. The SARAM™ has a sequential FIFO-like interface on one side and a SRAM on the other side. Refer to Application Note AN-120, "Functional Description of the IDT70825 SARAM™."

Bank-Switchable™ Dual-Port SRAM—The difference between a Dual-Port SRAM and the Bank Switchable Dual-Port SRAM is the number of transistors used in the cell. The Bank Switchable Dual Port uses the standard four transistor memory cell (see Figure 1). The BSDP is divided into four banks of memory. The Bank Switchable Dual-Port allows simultaneous access to the memory array, but each of the four banks can be accessed from only one port at a time.

What application notes are available?

- AN-02—Dual-port Simplify Communications in Computer Systems
- AN-09—Dual-port SRAMs Yield Bit Slice Designs Without Microcode
- AN-14—Dual-port SRAMs with Semaphore Arbitration
- AN-42—Using the IDT7050/7052 FourPort™ SRAMs in DSP and Matrix Processing Applications
- AN-43—The IDT FourPort™ SRAM Facilitates Multiprocessor Designs
- AN-45—Introduction to IDT's FourPort™ SRAM
- AN-59—Using IDT7024 and IDT7025 Dual-Port Static RAMs to Match System Bus Widths
- AN-68—Dual-port SRAM Simplifies PC-to-TMS320 Interface
- AN-70—Dual-port Interrupt Expansion
- AN-91—The Most Commonly Asked Questions About Asynchronous Dual-ports
- AN-120—Functional Description of the IDT70825 SARAM™
- AN-144—Synchronous Dual-Port Static RAMs for DSP and Communication Applications
- AN-253—Introduction to Multi-Port Memories
- AN-254—The Most Commonly Asked Questions About Synchronous Dual-ports
- AN-255—Dual-port Power and Board Layout Discussion

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