NEC

Application Note

V850

32-Bit Single-Chip Microcontrollers

Clock Monitor

V850E Series

V850ES Series

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[MEMO]

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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NEC Electronics America Inc.
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65 030
Fax: 0211-65 03 1327

Sucursal en España
Madrid, Spain
Tel: 091- 504 27 87
Fax: 091- 504 28 60

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Fax: 01-30-67 58 99

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Taipei, Taiwan
Tel: 02-2719-2377
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Introduction

Target Readers

This application note is intended for users who understand the functions of the V850 and will use this product to design application systems.

Purpose

The purpose of this application note is to help users to understand the functionality, benefits and how to use the clock monitor implemented in several microcontrollers of theV850E and V850ES subseries. The clock monitor peripheral an its features differ from device to device.
So, the handling and usage shown in this document is for reference only. Correct operation is not guaranteed if these samples are implemented as they are described here.
The user has to adapt the usage and handling of the clock monitor to his application specific needs.

Organization

This manual consists of the following main sections.

- Reason for implementation of a clock monitor
- Functionality of a clock monitor
- Remarks for usage of a clock monitor in an application
- Hints for handling during stand – by modes
- Handling example when clock monitor has generated a reset

How to Read This Manual

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:

→ Read this manual in the order of the **CONTENTS**. The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what:” field.

- To learn more about the 78K0/Kx2’s hardware functions:

→ See the user’s manual of each 78K0 product.

Conventions

Data significance: Higher digits on the left and lower digits on the right
Active low representation: xxx (overscore over pin or signal name)
Note: Footnote for item marked with **Note** in the text
Caution: Information requiring particular attention
Remark: Supplementary information
Numeral representation: Binary.....xxxx or xxxxB
Decimal xxxx
Hexadecimal .....xxxxH

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CHAPTER 1 BENEFITS OF A CLOCK MONITOR

1.1 Reason and benefit of a clock monitor

At the pins X1/X2, a resonator or quartz is connected to a microcontroller. The frequency which is generated by this oscillator is called mainclock. The mainclock is responsible for all functionality in the microcontroller. It is used to run the software, it clocks the on – board peripherals and is responsible to realise the timing, necessary for the specific application. If the mainclock stops unexpectedly, the microcontroller hangs up and the functionality of the application fails. It is imaginable that in some applications a microcontroller hang up will be a big disaster because this might destroy external environment or jeopardize humans.

The clock monitor is a peripheral, which supervises the mainclock. When the mainclock is much slower than expected or even stops, the clock monitor detects this and reacts on it.

The kind of reaction differs among the microcontrollers. Usually the clock monitor generates an internal reset when the mainclock fails. In some controllers the user has the possibility to select if an internal reset will be generated or a vectored interrupt (NMI) is generated by software. In most controllers, a marker bit is set during clock monitors reset generation. During reset initialisation the user can check if this marker bit is set and run a special software which handles the malfunction.

With the clock monitor peripheral, the microcontroller can react very fast on a mainclock failure and system break down can be prevented. Even some restricted functionality of the application can be realised or information of malfunction can be send to an host.

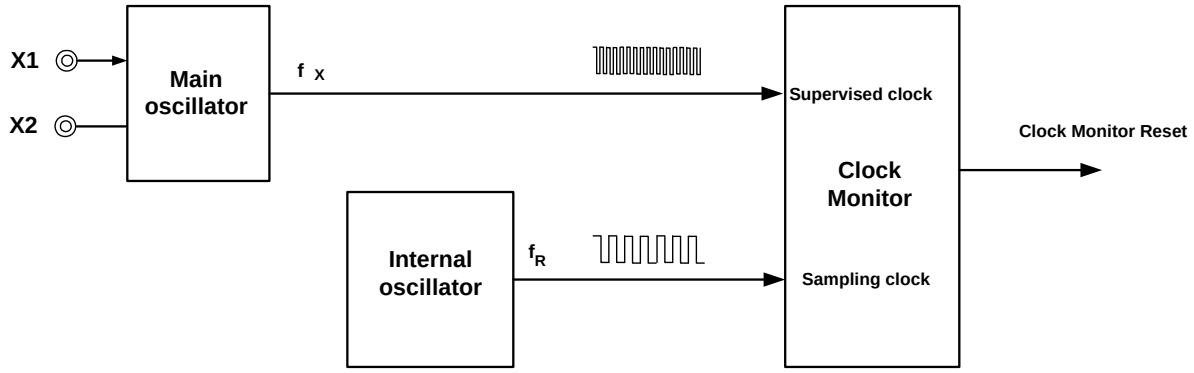
CHAPTER 2 FUNCTIONALITY OF A CLOCK MONITOR

2.1 Principal description of a clock monitor

For the functionality of a clock monitor, a second active frequency is necessary to supervise the mainclock. To be sure that the clock, used for supervision is working in each case, an internal oscillator is used for supervision. This internal oscillator has no connection to external. There is no pin which can influence or even stop the internal oscillator from outside. It is a very reliable kind of oscillator, active just when power supply is connected.

The principal block diagram of a clock monitor is shown in Figure 2-1.

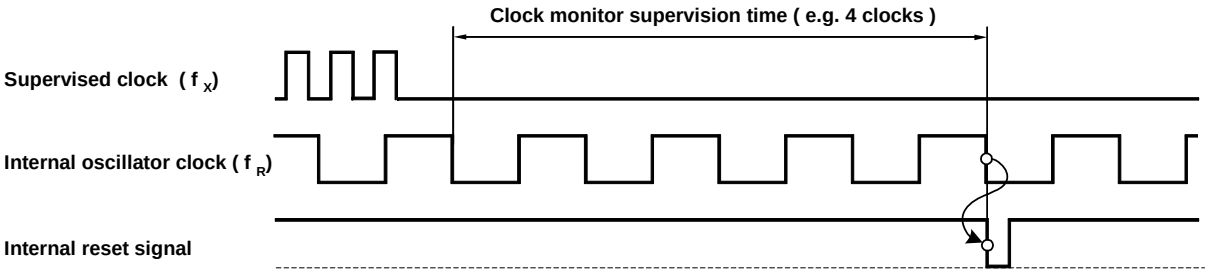
Figure 2-1. Principal block diagram of a clock monitor



The clock monitor samples the mainclock by using the internal oscillator. It generates a reset request signal when the oscillation of the mainclock has stopped or is too slow.

Figure 2-2 shows the internal behaviour when the mainclock fails. In this example, the mainclock supervision time takes four clocks of the internal oscillator. When there is no mainclock during this time frame, an internal reset request is generated.

Figure 2-2. Timing diagram when the mainclock fails



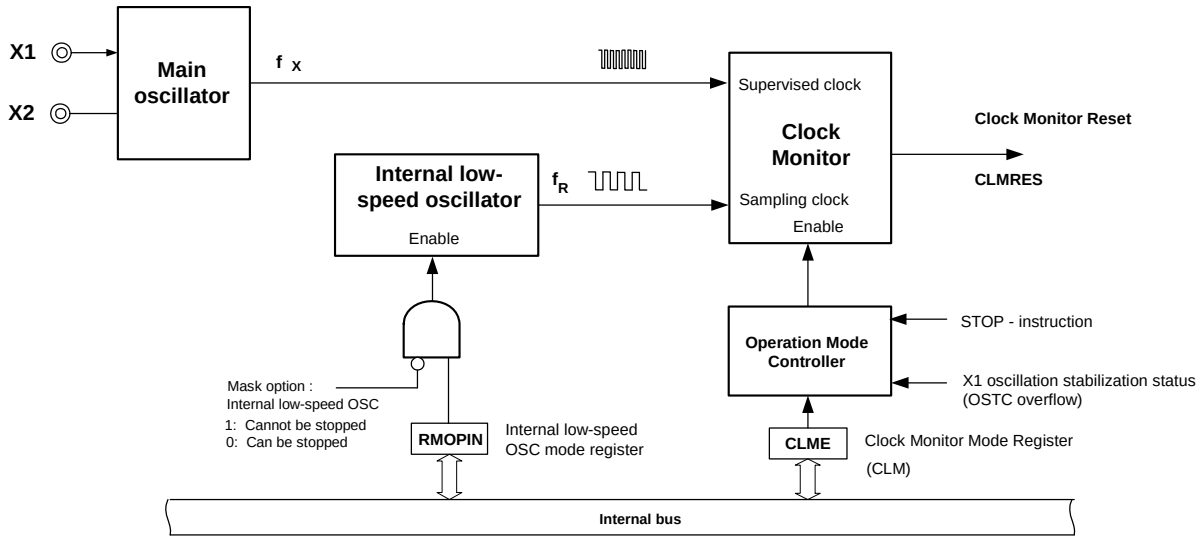
2.2 Controlling the clock monitor

2.2.1 Enabling clock monitor peripheral

In some applications, the clock monitor is not necessary or even not practicable. For this reason, the clock monitor can be switched on by software (CLME = 1) when it will be used in an application. Due to security reasons, if it is switched on once, it can not be switched off by software any more. Only a reset, even that one generated from the clock monitor itself, will reset the clock monitor enable bit (CLME = 0).

After reset release the microcontroller starts with CLME = 0 and the clock monitor is disabled.

Figure 2-3. Principal of a clock monitor with controlling function

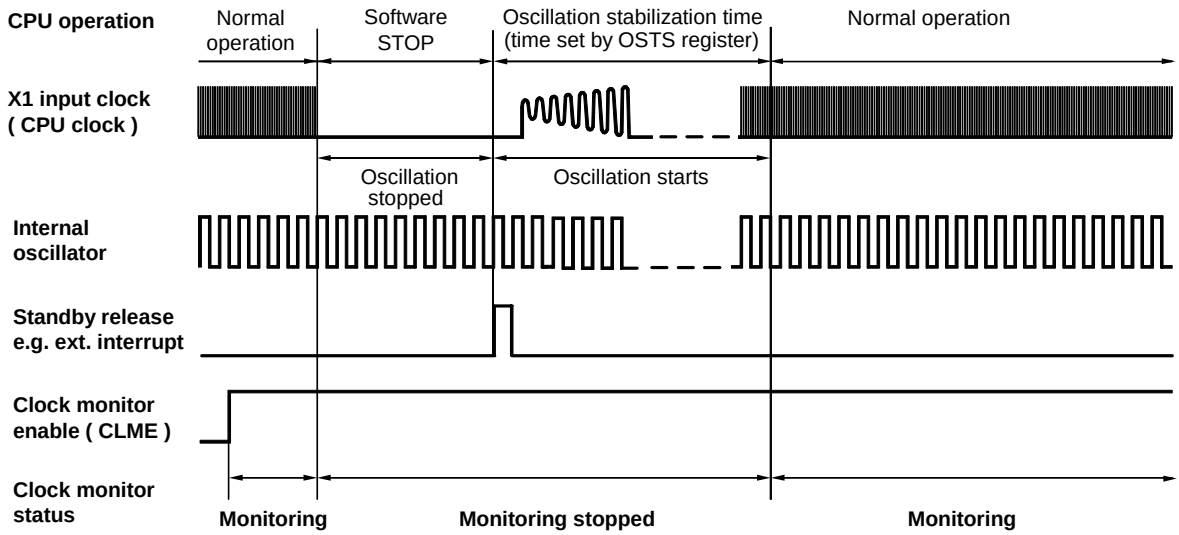


2.2.2 Stopping clock monitoring during STOP – mode

To be able to use the standby modes even when the clock monitor is active, there is a control unit included which takes care that the clock monitor is disabled when the mainclock is stopped in a controlled manner. Remember: once enabled, the clock monitor cannot be stopped by software any more.

When the STOP – mode is entered, the mainclock is stopped. A control logic detects this and stops the supervision during STOP – mode and after reset release during oscillation stabilisation time.

Figure 2-4. Clock monitor operation during STOP mode and after STOP mode release



Within the standby modes HALT, IDLE1 and IDLE2, the mainclock keeps oscillating. When the clock monitor is enabled (CLME = 1) and the internal oscillator remains active, the clock monitor status is “monitoring”.

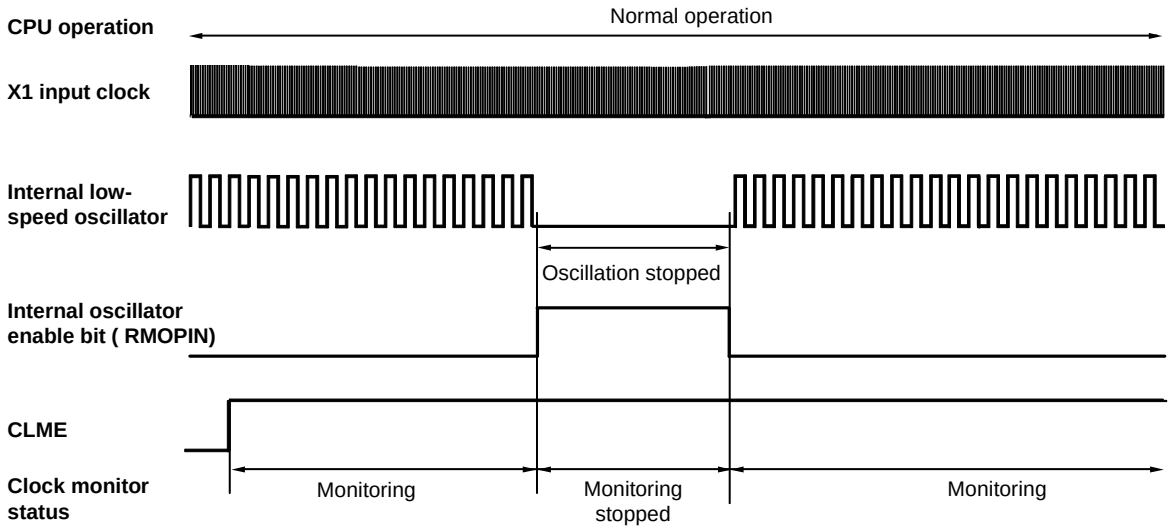
2.2.3 Stopping the clock monitor when the internal oscillator stops

Usually the user can decide if the internal oscillator can be switched on and off via software. This decision is fixed either by a mask option in a mask device or within an option byte in a flash device. So, this decision is fixed for all time due to the fact that the software can not change the option byte or a mask option by accident. So, the user can select either “internal oscillator can be stopped by software” or “internal oscillator can not be stopped by software”.

For supervision of the mainclock it is necessary that the internal oscillator is active. When the option “internal oscillator can be stopped by software” is selected and the internal oscillator is stopped by software, the clock monitor is also stopped. This gives the user the possibility to halt the supervision of the mainclock for a certain time. On one hand this is flexible, on the other hand, this is a security risk. If the mainclock fails while the internal oscillator is stopped, this failure of the mainclock is not detected.

When the internal oscillator is switched on by software again, the supervision function of the clock monitor is available as well again (see: Figure 2-5).

Figure 2-5. Stopping the supervision when internal oscillator stops



CHAPTER 3 BEHAVIOUR AFTER RESET RELEASE

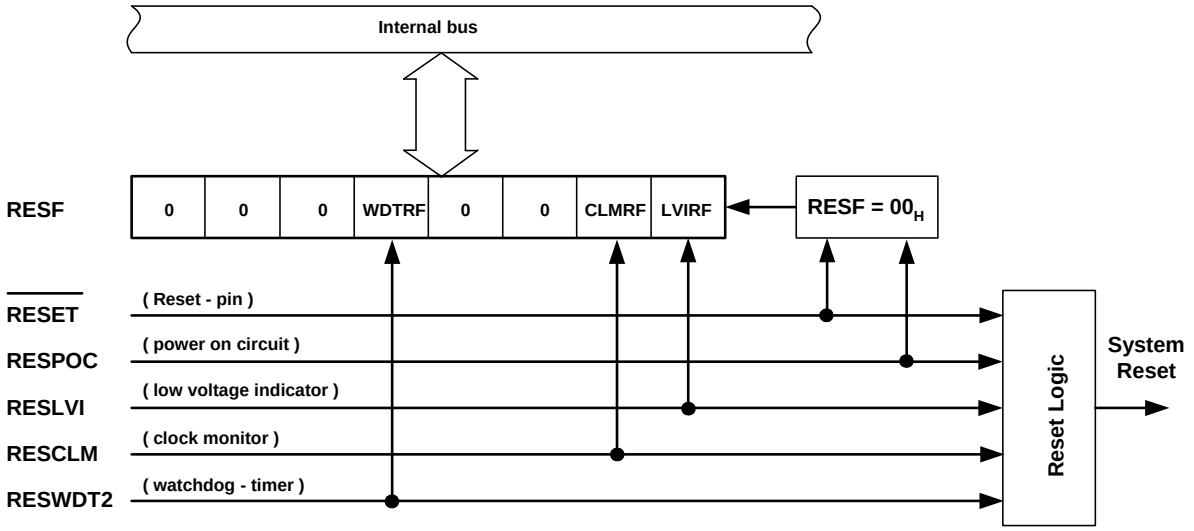
3.1 Detection of the indication for a Reset

Several reasons for a reset are possible. The usual source of a reset is when a reset signal is applied at the external reset – pin or that the internal power – on detection unit (POC) generates a reset. These resets are harmless ones, no functional abnormality has to be assumed.

When a reset is generated from a watchdog – timer (WDT), a low voltage indicator (LVI) or the clock monitor (CLM), an abnormal situation has been detected. In the controller, usually a reset control flag register (RESF) is implemented which stores the source of the reset. When this register is read during the reset software routine, the reason for the previously occurred abnormal operation can be detected.

Figure 3-1 shows an example how such a register is configured. Due to the microcontrollers of the V850 family differs in their peripherals, the specific configuration of the reset control flag register has to be examined in the relevant users manual.

Figure 3-1. Example for a reset control flag register (RESF)



3.2 Handling when a clock monitor reset has occured

After reset release, the software can read this reset control flag register. If the clock monitor reset flag is set, the mainclock has failed before. Now, the software is able to react on such failure. It depends on the application which kind of reaction is useful and possible.

After reset, the controller starts execution of the instructions based on its internal oscillator. So, in case of a clock monitor reset previously, it is not necessary to switch to the faulty mainclock. With its internal CPU clock, reduced functionality of the application should be available. An error message might be send to a host or an error indicator might show the malfunction for servicing.