JTAG TESTING OF MULTICHIP MODULES

APPLICATION NOTE AN-411

Introduction

IDT currently offers multichip modules (MCMs). These MCMs are composed of two or more arrays within a single package. Refer to Figure 1. These multi-array solutions typically offer enhanced functionality and/or greater memory density in a single package and thus save PCB area.

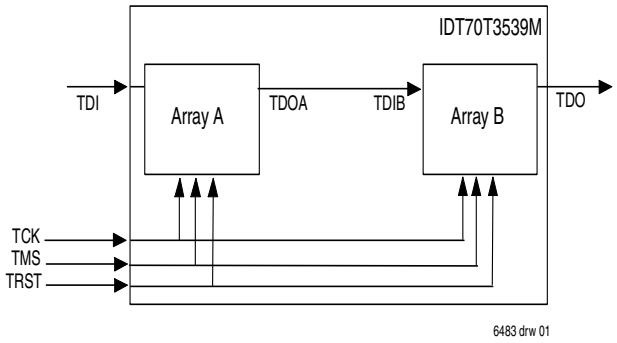

Figure 1. Scan Chain Configuration

IDT's MCMs that offer JTAG functionality are comprised of multiple IEEE 1149.1 (JTAG) compliant arrays. The MCM has all associated JTAG pins: TCK, TMS, TDI, and TDO. However, the MCM cannot be treated as a single JTAG device. Instead its internal netlist must be merged with that of the printed circuit board (PCB). Also, its boundary scan chain topology must be defined. IDT offers the associated BSDL files and netlist to allow JTAG testing of the MCM on a PCB.

The intent of this application note is to provide instruction on how to perform JTAG test pattern generation (TPG) for IDT's MCMs on a PCB. It will guide the user step-by-step through the netlist merge, boundary scan chain topology definition, and test pattern generation procedures. This process generates test vectors which can be used to test the entire PCB's JTAG devices (including one or more MCMs).

These procedures are demonstrated using the Corelis ScanPlus™ software using IDT's 70T3539M MCM & an FPGA as an example. Note that this procedure will be loosely similar to other JTAG TPG software and devices. Please contact the appropriate test software provider for platform-specific information.

JTAG Testing the MCM

Obtaining the MCM's BSDL & Netlist Files

One must first obtain IDT's MCM and BSDL files. These are available on our website at http://www.idt.com. On the website, look up your specific MCM device and find the support files. For this example, we will use the IDT70T3539M. Its file names are listed here for reference:

MCM File Name	
MCM Netlist File	70T3539M.net
MCM BSDL File for Array A	70T3539MBC_A1.bsd
MCM BSDL File for Array B	70T3539MBC_A2.bsd

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IDT's standard array nomenclature is A1, A2, ... An.

Table 1 - JTAG Test Vendor Cross Netlist Support

	Accel (.net)	Allegro (.net/.tel)	CADIF (.paf)	EDIF (.ed*)	Fabmaster (.asc)	Futurenet (.net)	GenCAD (.cad)	GenCAM	IFF (.iff)	Mentor Graphics (.nets)
ASSET InterTech Scan Works®		X	X	X			X	X	X	
JTAG Technologies Test Dev. Package	X	X		X	X	X	X			X
Corelis Scan Plus™	X	X		X		X				X
Teradyne Victory™	X	X		X		X				X
Intellitech Eclipse™	X	X		X	X		X	X		X
Flynn onTAP®	X	X		X						

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Table 1 - JTAG Test Vendor Cross Netlist Support(cont'd)

	Mentor Neutral (.neu)	Orcad (.net)	Pads (.asc/.net)	PCAD	Protel (.net)	PST-Cadence (.dat)	Redac-RINF (.net)	Theda	Veribest (.net)	Victory (.cds)	Viewlogic (pkg/.net)
ASSET InterTech Scan Works®	X					X	X			X	X
JTAG Technologies Test Dev. Package	X	X	X	X	X	X	X	X	X		X
Corelis Scan Plus™		X	X	X	X	X	X	X	X	X	X
Teradyne Victory™		X	X	X	X	X	X	X		X	X
Intellitech Eclipse™	X	X	X	X	X		X	X	X		X
Flynn onTAP®	X	X	X		X				X	X	X

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Conversion of the MCM Internal Netlist to the TPG-Compatible Netlist Format

Tables 1 & 2 show several popular competing JTAG TPG software solutions and their respective netlist format support. This table is not exhaustive. Please refer to the appropriate JTAG test vendor for the latest support.

IDT provides MCM netlists in Telesis (or standard Allegro) format. This format is supported by all JTAG TPG solutions listed in Table 1. However, converting from one format to another is possible if this format is not supported by your platform. Many JTAG TPG vendors provide conversion software to convert to their preferred format. Also, many 3rd party conversion tools are available. Please contact those solution providers for questions regarding use of their specific tools. Refer to Appendix A for a description of the Telesis netlist format.

Merging the MCM Internal Netlist with the PCB Netlist

A merge tool can be used to merge the MCM netlist with the PCB's netlist. Similarly, it can be used to merge a daughtercard's netlist with a motherboard's. Many TPG solution providers offer a merge tool to combine netlists. For example, Intellitech offers "CircuitMerge™", Corelis has "ScanPlus Merge™". ASSET Intertech, Flynn onTAP, and JTAG Technologies also offer this software.

For this example, Corelis ScanPlus Merge™ was used to combine the 70T3539M netlist with the PCB's netlist (PCB includes a Spartan-3 FPGA). The resultant combined netlist was titled "MyPCB.net". This same step should be performed for your particular PCB netlist.

Creation of a Topology File

Referring to Figure 1, the MCM's arrays have the JTAG pins (TDI, TDO) connected in daisy chain fashion. These, in turn, will be connected in similar fashion to the JTAG compliant devices on the PCB. As such, it is necessary to tell the JTAG TPG software the associated ordering of the devices in the scan chain. This is done within the JTAG Boundary Scan Topology File.

On the Corelis platform, the topology file is text based and can be created within a simple text editor. For this example, the following topology file was created in plain text and saved as "MyPCB.top":

```
!MyPCB Topology File - CHAIN  chain1

DEVICES
!
DEVICE   BSDL FILE                  PKG     PUT IN BYPASS
!
   A1    "70T3539MBC_A1.bsd"        BC256       NO
   A2    "70T3539MBC_A2.bsd"        BC256       NO
   A3    "xc3s400_fg320.bsd"        BC256       NO
END_DEVICES
END_CHAIN
```

Note that the devices are listed in sequence from first to last (TDI to TDO) respectively. The arrays within the MCM are called out individually, with the proper BSDL file listed for each array. It is necessary to properly order the memory arrays within the MCM. Here, Array A1 comes before Array A2. This is IDT's standard sequence (A1, A2, ..., An).

Constraint, Netlist Edit, and Merge Library Files

Optionally, the user may create a Constraint file (*.con), Netlist Edit file (*.edt), and Merge Pin Library file (*.lib). The Constraint file allows a user to set nets to specified logic levels and specify other constraints that need to be maintained when generating test vectors for the target board. This is useful for applying static bias to non-boundary scan device enable signals, chip selects, etc. to prevent these devices from interfering with the boundary scan tests.

The Netlist Edit file allows the user to modify the netlist using a separate file without disturbing the original netlist file.

The Merge Pin Libarary file contains instructions for handling

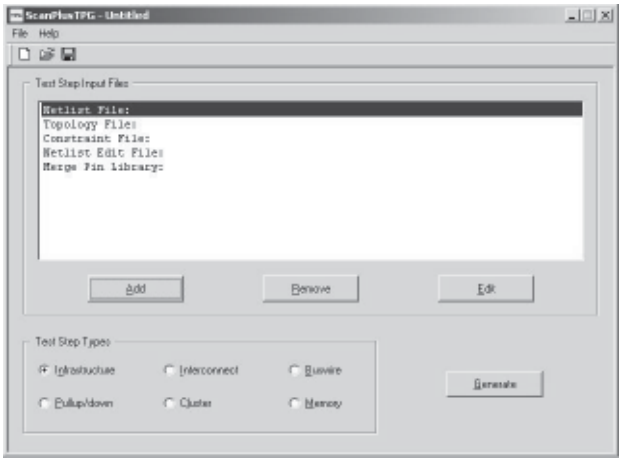
transparent components such as resistors, switches, etc. These devices can be tested "through" without affecting test results.

For this simple example there are no transparent devices or netlist modifications. Thus, we will not use these files.

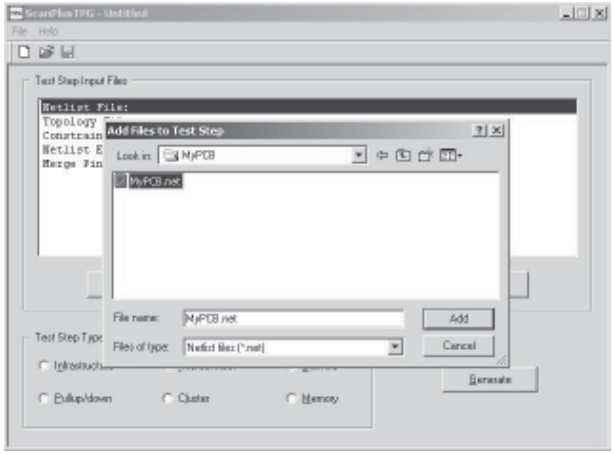
Procedure for Generating Interconnect Test Vectors

The following explains step-by-step how to use the ScanPlus™ TPG Software to generate test vectors:

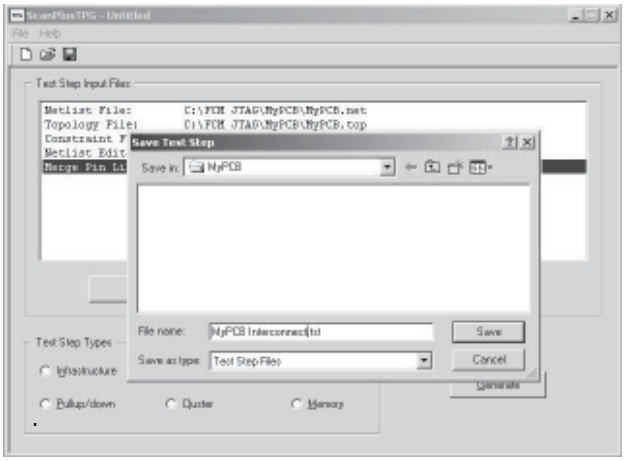
1. First start the ScanPlus™ TPG software. A screen-shot showing the ScanPlus TPG Graphical User Interface (GUI) is shown below.



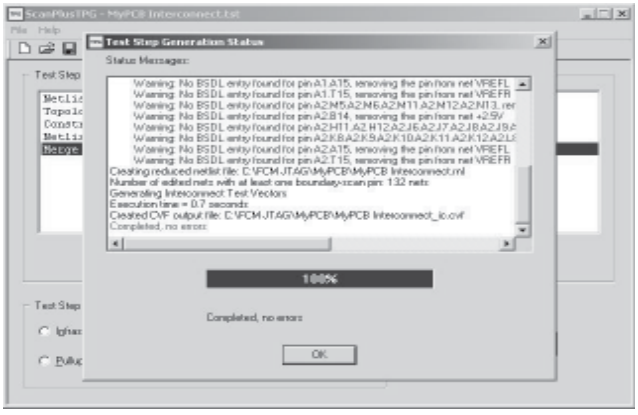
2. Select the "Interconnect" button in the "Test Step Types" area.
3. To select the netlist file, click on the first row "Netlist File:" Click on the "Add" command button. Find the directory where the input files are located. Select the "MyPCB" netlist file (.net) and click on the "Add" command button.



4. To select the topology file, from the ScanPlus TPG main screen, click on the "Topology File:" row. Click the "Add" command button and then select the "MyPCB" topology (.top) file.
5. Note that this example does not require a Constraint file. If you require a Constraint file, click on the "Constraint File:" row. Click the "Add" command button. Select your Constraint file (.con) and click on the "Add" button.
6. Note that this example does not require a Netlist Edit file. However, you may choose to add a Netlist Edit file by selecting the fourth row in the main screen. Click the "Add" command button. Select your netlist edit file (.edt) and click on the "Add" command button.
7. Note that this example does not require a Merge Pin Library file. If you require a Merge Pin Library file, select "Merge Pin Library" from the main window. Click on the "Add" command button. Select your merge library file (.lib) and click the "Add" button.
8. Save this test step by clicking on the toolbar disk icon, or select "Save Test Step" from the "File" menu. This test will generate interconnect test vectors, that will be called "MyPCB Interconnect" test file (.tst) for this example.



9. Click on the "Generate" command button. The software will begin generation of all associated interconnect test vectors. While running the main screen will display any Warning or Error messages. Once completed, the software creates a .cvf file. This file may be used with ScanPlus Runner™ for testing the PCB's interconnections.



Appendix A.
Telesis Netlist File

A netlist file describes all of the nets and pins of a target board. There are many different netlist file formats, but ScanPlusTPG uses the Telesis (or standard Allegro) file format because of its simplicity. The structure of a Telesis netlist file is shown in Table 3. The first keyword is "$PACKAGES" which designates the beginning of the package definition block which may contain one or more device package description entries. Each line consists of a package type designation, a separating exclamation point, a package subtype for value, a separating semicolon, and finally the device ID. Some versions of Telesis omit the package type field and instead put that value in the package subtype/value field. ScanPlusTPG does not use the information in the package description block and ignores it completely. After all package definitions have been specified, the "$NETS" keyword designates the beginning of the net descriptions which contains one or more net description entries. Each net description begins with the name of the net (which is sometimes enclosed in quotes) followed by a semicolon and then a space separated list of device.pin names. If the net description occupies more than one line a comma at the end of a line indicates that more pin names are on the following line. The end of the $NETS" section and the netlist file is designated by the "$END" keyword.

An example of a Telesis netlist is shown in Table 3. Note that this is not a complete and valid netlist, it is a small portion of a netlist intended only to show the appearance.

Table 3 - Telesis Netlist Structure

```
$PACKAGES
 {package type}! {package subtype/value}; {device ID}
...
$NETS
{netname}; {device.pin 1} [device.pin 2] ... [device.pin N]
...
$END
```

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