Introduction

Hardware design in high performance applications is rapidly becoming more complex. Designers typically use solutions they are familiar with and generally prefer the simplest solution available. At first glance a crystal oscillator (XO) seems like an easier solution than using a programmable clock. At first glance, programmable clocks may seem complicated, however, they offer a lot more flexibility and ultimately lead to a more elegant solution.

1 Main Advantages of Programmable Clocks

The VersaClock® family of programmable clocks has many advantages versus XO or crystal devices.

Flexibility is a main advantage of a programmable clock:

From the frequency generation (1 MHz to 350 MHz) to the outputs programming stand point, VersaClock 5, VersaClock 6 and VersaClock 3 can generate a lot of different combinations. The following output types, LVPECL, LVDS, HCSL, LP- HCSL, single ended and differential LVCMOS, are programmable via I2C. It can cover different voltage output levels from 1.8V to 3.3V. See Section 2, “Output Logic Levels for Programmable Clocks” for more details on the output logic levels.

Not to mention that the VersaClock family of products offers the advantage of having multiple configurations programmed in the OTP. Up to 4 configurations (5 for VersaClock 3) can be programmed and selected with SEL pins. That means 16 different frequencies can be generated from the same device.

The performance of VersaClock 5 (0.7 ps RMS phase jitter) and VersaClock 6 (0.5 ps RMS phase jitter) are perfect for Ethernet switch/router, 10G Ethernet and driving FPGA clock requirements (see AN-905).

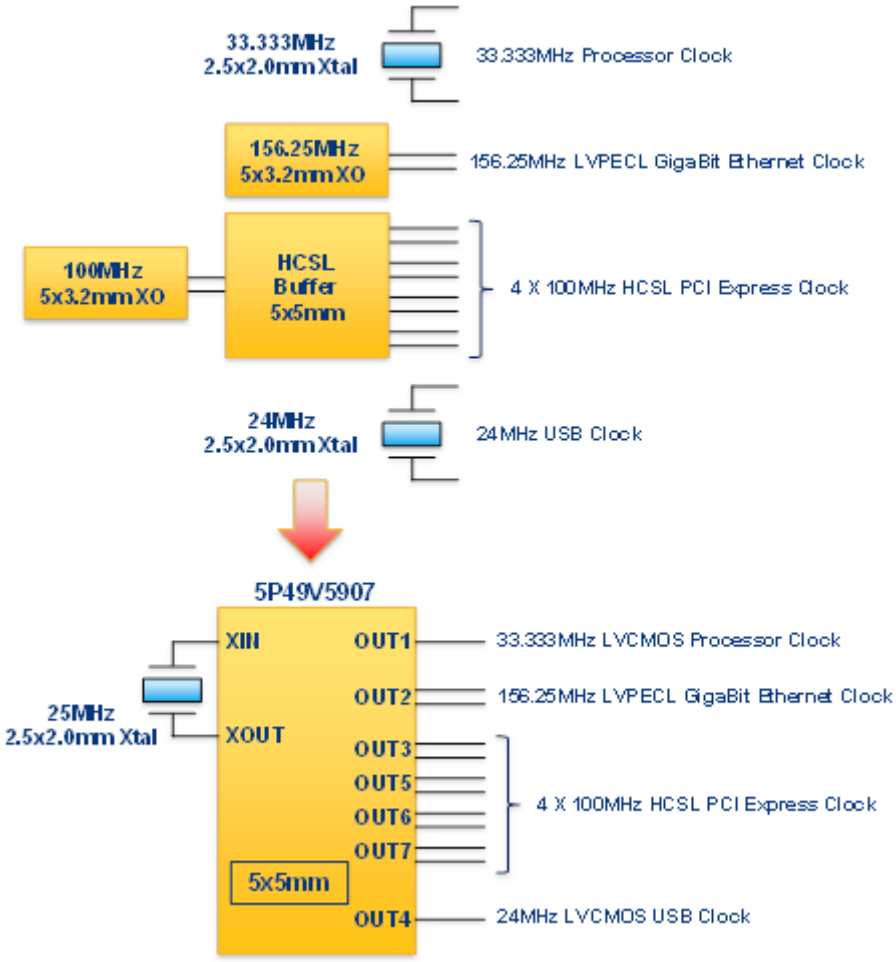
Saving space and cost is another superiority of using programmable clocks. One single device can replace many crystals and XO devices and reduce board size. The number of outputs can go up to 9 outputs for VersaClock 3 (replacing up to 9 crystals or XO).

Figure 1 below illustrates an example application that uses a processor clock, a GigaBit Ethernet clock, four PCI Express clocks and a USB clock.

The original application uses two crystals, each with $5mm^2$ size. There are two XO modules with $16mm^2$ size and one clock generator IC with $25mm^2$. This adds up to $67mm^2$ total space. The VersaClock 5 replacement uses $5mm^2 + 25mm^2 = 30mm^2$ total space, less than half.

Cost savings for this example are 30% ~ 50% depending upon volume and specifications. This is just an average example of what is possible.

Figure 1. Example Application where a 5P49V5907 Replaces Many Devices



The possibility to enable spread spectrum function with VersaClock 3, 5 and 6 or PCIe frequency generators to reduce EMI will be described in Section 5, “Multiple Devices in One”

2 Output Logic Levels for Programmable Clocks

VersaClock generators have individual output buffer power supply pins and the output levels for LVCMOS can be set by applying the desired power supply voltage. When driving a crystal pin from an LVCMOS output this is also useful for adjusting the driving amplitude.

Differential logic types LVDS and HCSL are not dependent upon the power supply value and the power supply level can be different at the driver side and receiver side without causing issues.

LVPECL uses VDD (or VCC) as its reference so it is important to choose the correct power supply value. VersaClock devices can work with both 2.5V and 3.3V power supply values.

PCIe clock generators or buffers can also be used to drive a variety of clock inputs. See application note AN-891 for driving various input types from IDT's Low Power HCSL drivers.

3 Clock Frequency Accuracy

The clock outputs of a clock generator IC are as accurate as the reference clock supplied to the clock generator. When replacing a number of clock products and one of them is a very accurate clock like a TCXO, then it makes sense to preserve the TCXO and use it as a reference for the clock generator so all clocks from the clock generator get the same TCXO precision. In general one selects to use a reference that meets the requirement for the clock with the tightest frequency accuracy spec. All clocks will now meet this tightest spec.

VersaClock devices have capacitors for the crystal load capacitance on the chip and these capacitors are programmable. It is possible to fine-tune the load capacitance to correct for PCB parasitic for better frequency accuracy.

VersaClock generators 5P49V5935 and 5P49V5933 have the reference built in. This has two advantages:

1. It relieves the customer from acquiring the proper frequency reference, either a crystal or oscillator product.
2. Nominal accuracy is better than a plain crystal because the integrated reference is calibrated during production. It can be argued that the integrated reference is also better than the average clock oscillator precision. When the crystal in a clock oscillator is calibrated, there are more manufacturing steps to follow that can shift the final frequency. This results in additional frequency inaccuracy. The VersaClock calibration is done through programming without physical changes to the product after the calibration so the final frequency will remain where you set it.

The 5P49V5935 can be found at:
www.idt.com/products/clocks-timing/clock-generators-frequency-synthesizers-pll-and-differential-clocks/programmable-clock-generators-low-power-programmable-oscillators/5p49v5935-versaclock-5-low-power-programmable-clock-generator-integrated-crystal

4 Frequency Margining

Using the pre-programmed configurations in the VersaClock generators it is possible to switch between fast, slow and nominal frequency sets for frequency margining purpose. Granted, the fast and slow frequency sets will only be used during the qualification phase of the application but nevertheless the frequency margining feature is very popular with the VersaClock generators.

Besides, using different configurations, frequency margining can also be achieved by applying changes through I2C programming.

5 Multiple Devices in One

Another benefit of multiple configurations in VersaClock generators is that the same device can be used in multiple locations with different configurations in each location. This greatly benefits inventory and logistics.

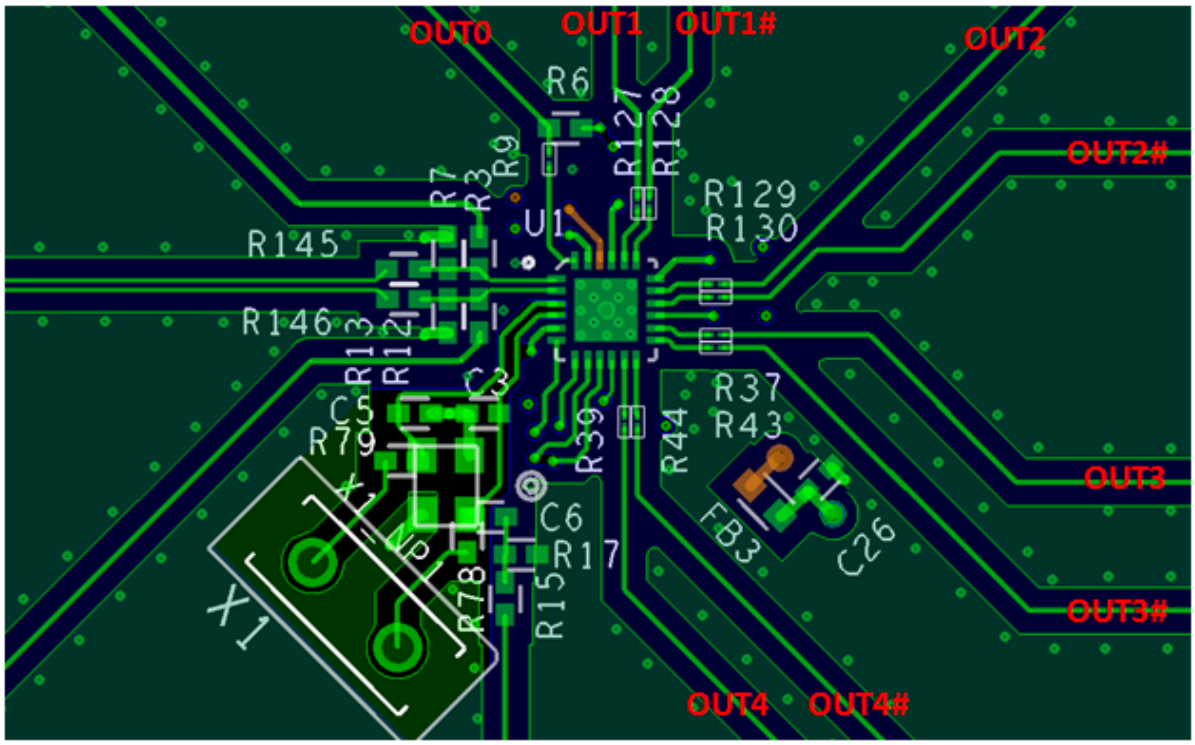
6 Layout Focus

It is important to layout clock traces as transmission lines. Theoretically a transmission line does not radiate and preserves the original waveform. Losses in a clock trace usually are insignificant at frequencies where crystals operate and at frequencies available from VersaClock products. The theoretical loss with a typical 50Ω trace on FR4 is 1dB or 10% in signal amplitude at 500 MHz and 35 cm (14 inches) of trace length. PCBs larger than 70 cm (placing the clock IC near the center) are unlikely.

Replacing XOs is the least complex because the clock generator output only needs to be set to the same logic type as the XO it is replacing. Replacing a crystal may need more care. It is still easy when the IC manufacturer simply states that the crystal oscillator input pin can also be driven with an external clock. See “Appendix A” for a recommended circuit when driving a crystal oscillator input pin.

Figure 2 is a snapshot of a VersaClock 6 Evaluation board layout (around VersaClock 6). All outputs are properly terminated with 33Ω series resistors, followed by 50Ω traces.

Figure 2. Example VersaClock 6 Layout



7 EMI

Whenever the subject is brought up of replacing XOs and crystals with a multiple output clock generator IC there is worry about EMI. The clock generator cannot be close to all target inputs so relatively long clock traces will be needed for some targets. Tests have shown that the clock generator IC is often a cleaner solution when IC bypassing is done properly and clock traces are laid out as transmission lines (stripline or micro strip). For more details about clock generator layout guidelines, please refer to: www.idt.com/document/apn/909-pcb-layout-considerations-designing-idt-versaclock-5-clock-products

Crystal and XO devices can actually emit significant radiation. A few milliamps of RF current pass through the crystal and its traces. The crystal circuit is a resonating tank and damping of the tank should be avoided for reliable operation of the crystal oscillator. The traces to the crystal need to maintain high impedance to ground and therefore cannot be designed as transmission lines. As a result the crystal traces emit electromagnetic radiation.

With XOs the main source of radiation usually is not the clock output when the clock trace is designed properly. The main source of radiation is the power pins. Because of cost, most XOs do not have power supply bypassing inside the package and switching currents will flow in and out of the VDD and GND pins. EMI from power supply connections is proportional to the distance between the actual chip and the closest bypass capacitor. In general it is easier to place bypass capacitors closer to the actual chip with clock generator ICs than it is with an XO. As a result we often see less EMI from a clock generator solution.

VersaClock and PCIe generators have a spread spectrum feature that can help reduce EMI further by 'spreading' the clock. Spread spectrum can reduce cost even more when shielding efforts are no longer necessary to meet EMI requirements. Spread spectrum is a certain type of modulation that essentially causes a certain amount of jitter to spread the energy over a wider range of frequencies. While not suited for every application, more and more systems are designed to be able to handle a certain level of spread spectrum modulation. PCI Express is an example of such an application. With VersaClock generators we can choose the amount of spread spectrum modulation so it can be dialed in to the level the application can tolerate or what is needed to achieve certain EMI performance.

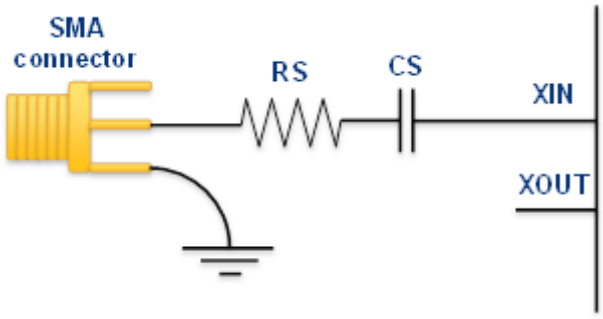
VersaClock 5 devices 5P49V5907 and 5P49V5908 combine PCI Express clock fanout with additional programmable clock outputs so the single device can provide almost all the clock needs of an application.

The 5P49V5907 can be found at:
www.idt.com/products/clocks-timing/clock-generators-frequency-synthesizers-pll-and-differential-clocks/programmable-clock-generators-low-power-programmable-oscillators/5p49v5907-versaclock-5-low-power-programmable-clock-generator

8 Noise / Jitter Considerations

For a clock input there usually is a noise or jitter spec. So when replacing a XO that drives that clock input, the noise and/or jitter requirements usually are known. With a crystal oscillator it is very unlikely to see a noise spec in the IC datasheet unless the datasheet describes how to drive an external clock into the crystal oscillator input pin. Crystal oscillators are very low noise by nature and the noise properties are not very dependent upon the crystal manufacturer so there is no motivation for the IC manufacturer to publish the actual requirements. However, knowing the overall requirements for the system that the IC is a part of, a ballpark value for crystal oscillator noise can be predicted. When the ballpark noise requirement is in line with the clock generator noise performance, an actual test can be done using a sample of the clock generator on its evaluation board, wired into the target crystal pin. An SMA connector can be wired to the XIN pin and attached through a 50Ω coax cable to the evaluation board for the clock generator. See below example:

Figure 3. Wiring an Evaluation Board Clock into a Crystal Pin



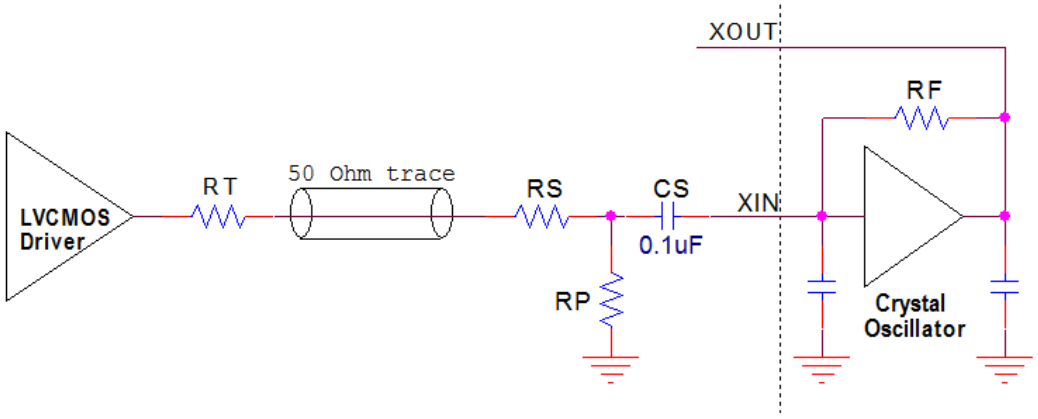
Also see “Appendix A” for optional signal adjustments for optimum performance. When the evaluation board output is AC coupled, CS will not be needed. Connect the SMA connector ground as close as possible to the IC ground pin for the crystal oscillator to avoid adding in ground noise.

Differential clocks can be wired similarly, where 50Ω coax cables are replacing 50Ω traces. The original termination scheme can be preserved where possibly the evaluation board needs to be adjusted for the source side of the termination.

Appendix A

Figure 4 is a generic circuit for driving a crystal pin from a single ended LVCMOS clock output.

Figure 4. Driving XIN from an LVCMOS Output



On-chip crystal oscillators are commonly designed around an inverting amplifier. There are capacitors to match the load capacitance of the crystal and a feedback resistor RF for DC bias (see Figure 1). Instead of connecting a crystal between the XIN and XOUT pins, XIN can also be driven with a single ended clock signal. In that case XOUT will be left open. When using CS for AC coupling, the crystal oscillator's DC bias remains functional.

RS and RP are optional. RS on its own (no RP) can help slow down rise and fall times of the signal at XIN. The circuit is originally designed for use with a crystal where the waveform at XIN will be sinusoidal. There may be extra cross-talk into other circuits on the IC when applying fast clock edges to XIN and RS can help slow the edges down. Common values for RS are 100Ω to 1000Ω. RS is essentially in series with the 50Ω output impedance of the PCB trace. Without RS (RS=0) the rise/fall times at XIN will be dominated by the RC-time of 50Ω with the XIN input capacitance, for example 50Ω × 24pF = 1.2ns. Adding RS=100Ω will triple the rise/fall times to 3.6ns.

A combination of RS and RP works as an attenuator in case the LVCMOS clock amplitude is too large for XIN to handle. The easiest way to control the amplitude is with the LVCMOS driver power supply voltage but when we have limited choice of power supply voltages or the amplitude needs to be smaller than the lowest available power supply voltage, RS and RP can be used to set certain attenuation. The attenuation can be calculated with $V_{XIN} = V_{LVCMOS} \times RP / (RP + RS + 50)$. The output impedance of the RS & RP network controls the rise/fall times. The output impedance is RP parallel to (RS+50). For example when RS=50Ω and RP=100Ω, the amplitude at XIN will be $V_{XIN} = V_{LVCMOS} \times 100 / (50+50) = V_{LVCMOS} \times 0.5$. The output impedance of the network is RP // (RS+50) = 100 // (50+50) = 50Ω. In case the XIN input capacitance is 24pF, the rise/fall times will be about 1.2ns.

The value of RT depends upon the output impedance of the LVCMOS driver. In case the LVCMOS driver output impedance is 17Ω, the value of RT needs to be 33Ω to add up to 50Ω for matching with 50Ω PCB trace impedance. RT needs to be placed near the LVCMOS driver output pin. RS, RP and CS need to be placed near the XIN input pin.

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