AHL EMC Design Considerations

Electromagnetic Compatibility (EMC) compliance is a key component of every automotive system design. Although the requirements for the Automotive High-Definition Link (AHL) platform are typical, this document presents good design practices and a few component requirements to help achieve testing success.

Contents

1. What is EMC?

Electromagnetic Compatibility (EMC) is a the ability of a system to operate correctly in the presence of external noise. A related concept is Electromagnetic Interference (EMI), a measure of noise generated by a system that might affect the surrounding environment. Whether multiple systems in close proximity will operate correctly is a difficult question, so there are standards that quantify the amount of noise a system can either generate or tolerate, and define specific measurement setups to test it. Standards include CISPR25, ISO 11452-2, and ISO 11452-4.

2. What causes EMI?

Noise is typically generated in AC circuits. Noise is created when a portion of an AC signal does not travel to or is not fully dissipated at its destination. Noise can couple to nearby components and signal paths, or noise can radiate directly; partly because, it is inherent in system design. A voltage potential between two points creates an electric field. Current flow between two points creates a magnetic field. In a modern PCB design, components and traces are placed as close together as possible creating parasitic capacitance between neighbors. Every real component or PCB trace has inherent inductance. When closely spaced, the mutual inductance or mutual capacitance between neighbors allows a portion of a signal to reach an unintended destination.

A signal reaching an unintended destination might not be a problem on a single board, but it can become a problem when this noise couples to the wiring harness. The harness becomes a conduit for the noise to travel to other systems and affect its operation; this is known as conducted emissions. Another conduit is space. Energy can be directly emitted from components or traces and reach unintended targets through the air; this is known as radiated emissions. Conducted emissions, radiated emissions, or both can corrupt system operations.

3. Good Signal Integrity Practice

The fundamental piece of any EMI/EMC mitigation scheme is good signal integrity. The basic principal is to transmit the required signal energy from the source and dissipate it at the intended destination. In an AHL system, this is the video signal. An additional goal is to keep noise energy local so that it is not conducted to other parts of a system. A signal integrity plan should minimize the generation of noise and keep generated noise from spreading to other parts of the system or other systems. This section discusses general PCB design practice as it relates to good EMI/EMC design.

3.1 Signal Termination

AHL is designed to communicate across low-cost UTP cables and to have shunt termination on both ends of the cable. A common cable type, CAT5, has a differential impedance Zdiff = 100Ω, which is accomplished by connecting a 49.9Ω from the P-signal and another from N to GND. Twisted pair cables also have common mode impedance that occurs when both P and N are driven with the same potential. To completely terminate the cable, the common mode impedance Z0cm must also be terminated. This is not a cable specification like differential impedance, because it highly depends on the other wires or cables in the signal harness. To get an accurate value, this should be measured with a VNA, but an approximation is often adequate.

The two resistors that provide differential termination R_{term_diff} = R1 + R2 also provide common mode termination except R_{term_cm} = R1 || R2 or ~25Ω, which is too small in almost all cases. In a harness that has several other wires (other than the P and N AHL signals), R_{term_cm} > 65Ω. Choosing a value ~75Ω is much closer than 25Ω. This is accomplished by using a Y-termination scheme (see Figure 1).

Note: A pi network can deliver differential and common mode termination, but because it is difficult to visualize and diagram, it is left for the reader to explore.

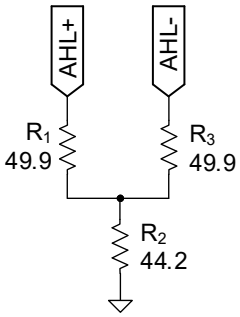

Figure 1. AHL Y-Termination

IMPORTANT: R1 and R3 are determined by Z0 of the cable; R2 is determined by the cable and other wires in the signal harness. *IMPORTANT:* Common mode signals are a primary source of EMI.

Termination resistors should have 1% tolerance because the delta between components causes a proportional portion of the signal to be converted from differential to common mode. Although common mode termination lowers the effect, it is better to not have a common mode signal.

Also, the signal harness requires at least one additional wire for common mode termination because the common mode current requires a return path. If the P and N signals are the only wires in the harness, the common mode current return could be radiated or coupled to the nearest ground; this makes common mode termination impossible for an EMI test.

Z0cm is implementation-dependent and relies on the other wires in the signal pair harness, so the accuracy in determining Z0cm affects how accurately you can set Zterm_cm.

3.2 Signal Traces

PCB trace signals can be an EMI source. The best way to minimize this is to terminate signals so that energy is not bouncing between the source and destination. Signals that have termination at both the source and destination are not problematic when the termination matches the characteristic impedance (Z0) of its PCB trace. When everything matches, there are no reflections. CMOS signals often do not have termination. A good approach is to use source termination: this places a resistor in series with an output signal near the output pin that has a value when summed with *Zout of the IC* equals *Z0 of its PCB trace*. In practice, traces with Z0 = 50Ω are a good choice, and for most CMOS outputs, a series resistor Rs = 22Ω or 33Ω creates a good match. This approach reduces EMI in two ways: (1) Rs reduces the current on the trace, and (2) there is a single reflection at the destination but that reflection is fully dissipated back at the source.

3.3 Clock Signals

Clock signals might be local to a single IC, or they might propagate to many locations on a PCB. In both cases, the best approach is to use the minimum amount of energy that allows the system to operate under all specified conditions. This can be done by minimizing energy in the clock generation circuit. For multi-IC clock connections, using a series resistor to minimize the current running around the board lowers potential EMI. Specific recommendations for AHL ICs are described in the section AHL Oscillator Circuit.

3.4 Power Rail Decoupling

In theory, power rails are DC connections and should not produce AC noise; however in practice, the ICs connected by power rails also connect to devices that have switching or AC signals, a portion of which is coupled to these traces. This is problematic because this noise is coupled to all connected ICs on that trace. The best way to combat this is with proper power supply decoupling. The goal is to keep any generated noise local. There are many opinions on the best practice, but the key for effective decoupling is minimizing parasitic inductance.

Decoupling creates a local loop that prevents noise from propagating across a board. One or more capacitors are connected across the power rail and ground pin and closely to an IC. So as PCB traces have self inductance, set traces that are short and wide, and use a minimal amount of vias as they too have inductance. Often in the industry, the paralleling of three capacitors is recommend with values one decade apart; although this was true for leaded capacitors before the advent of SMT components, the value of this approach today is marginal. The ESL of SMT capacitors is low compared to the layout loop inductance even when using different sized capacitors. It is typically impractical to put three capacitors in parallel for each power pin.

The best approach is to put a single cap with the largest value that component size allows. Minimize the distance from the IC and use as few vias in the loop as practical.

3.5 Power Planes

Routing power from power sources to ICs with PCB planes is a good approach. The power plane acts like an extra wide trace giving it low self inductance. For smaller boards and ICs with a single power rail this is a great approach. With large, complicated PCBs with ICs that have three or more power rails, it becomes more complicated. While the low inductance of planes is still a good attribute, there are possible pitfalls. Problems can arise when a board has many power plane partitions with signals in an adjacent layer.

A transmission line has two components, the signal trace and the reference plane. With a four-layer board, the power layer is often used as a reference plane for signals. For any controlled impedance trace, it is critical that there are no breaks or gaps in the reference plane. If a signal trace runs over two or more power planes, it causes a discontinuity in the signal return. For high speed signals (>1MHz), the return current tries to flow directly below the signal trace. If a discontinuity is encountered, the return current finds the lowest impedance path back to the reference plane. This unconstrained path is an EMI source and must be eliminated. Stitching capacitors can be used to couple different power planes allowing the return current to roughly follow the signal; but by adding vias and additional components, parasitics are added which can be EMI sources.

The best approach is to never have a gap or void in a signal return path.

3.6 PCB Stack-up

There are many opinions on PCB stack-up. AHL would be termed as a medium speed system with normal requirements. PCBs require impedance control on the video inputs to the RAA279971, video outputs from the RAA279972, and the AHL signal on both boards. Three stack-ups are suggested in Figure 2. Layer 1 or Layer 4 must be partly signal layers because ICs are soldered to one or both. For this reason, Option 1 is commonly chosen.

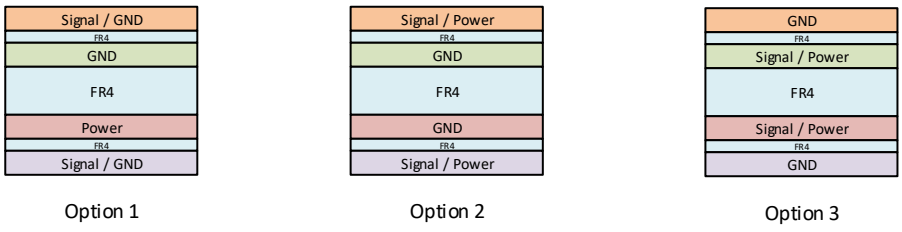

Figure 2. AHL Possible PCB Stack-Ups

A problem with Option 1 is that it uses the power plane as a signal return path and so has the potential of routing over voids mentioned in the Power Planes section. While Option 2 eliminates the possibility of routing signals over power voids, it makes power routing more complicated. Power traces are mixed with signals that can lead to many vias, and wider traces that lower self inductance are required for power which can be an issue for high current devices. Option 3 routes signals internally which can reduce radiated emissions; however, this option is not recommended because not only does it complicate debugging but properly designed transmission lines should not radiate. Option 3 solves a non-existent problem.

4. AHL Specific Recommendations

In this section, signal integrity rules are applied to a pair of AHL boards and cable. In all AHL systems, there are at least two boards, Tx and Rx. Good signal integrity practices need to be applied in the design of each. For non-AHL ICs on Tx and Rx boards, use general rules such as those in section Good Signal Integrity Practice.

4.1 AHL Signal Termination

In Good Signal Integrity Practice, section Signal Termination is a general discussion of termination, but the given example is the usual case for AHL and can be followed as documented. A cable with Z0 = 75Ω is a possible option; in this case, R1 + R3 = 75Ω so that R1 = R3 = 37.4Ω. From an EMI standpoint, this does not make a difference, the only requirement is that the termination matches the cable. Common mode termination is also different. R2 in Figure 1 must change so that R_{term_cm} = R1 || R3 + R2 equals Z0cm of the signal harness. For either option, Z0cm must be accurately known for proper termination.

4.2 AHL Signal Traces

The AHL signal is a differential signal requiring differential PCB traces, so the P trace and N trace must be equal in length to avoid mode conversion from differential to common mode. If single-ended signaling is used for either parallel video inputs (VDx) on the Tx and/or outputs on the Rx series, termination is recommended. If traces are short, skip this approach.

4.3 AHL Oscillator Circuit

Tx and Rx devices each use a Pierce crystal oscillator circuit with an external damping resistor. Load capacitance and resistor values are recommended by the crystal manufacture. To minimize EMI, the resistance of the damping resistor Rd should be as large as possible while maintaining reliable oscillation over all system conditions: voltage, temperature, and others. This method reduces the voltage swing and current on Clk_out; and, the clock frequency is 27MHz, so this reduces both the frequency and its harmonics.

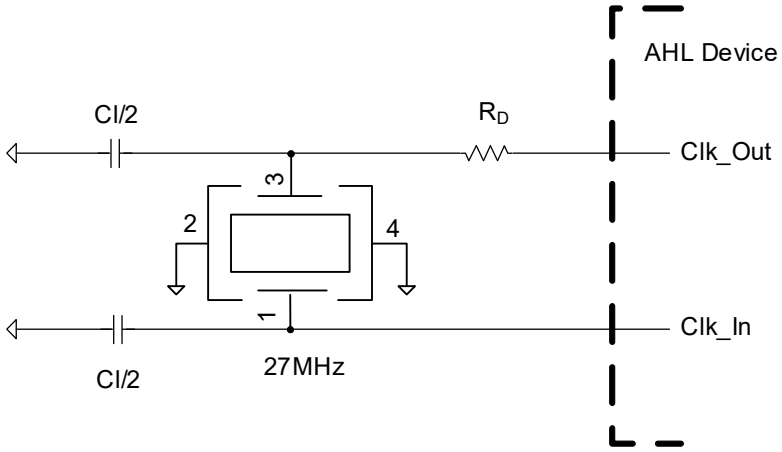

Figure 3. AHL Oscillator Circuit

The oscillator circuit should be located as close as possible to the AHL device in the PCB layout and on the same layer. The area of the loop on the board formed by Clk_Out, Rd, crystal, and Clk_In should be minimized. The radiated emissions are proportional to the area of this loop.

The oscillator circuit is powered by VDDIO which can be set between 1.62V and 3.6V. Lower values reduce the oscillator voltage swing and current an in turn lower EMI. On the RAA279972, the oscillator power is combined with other pins so reducing it has additional considerations. The RAA279971 has 2 VDDIO pins, so the oscillator is only combined with I^2C. See device datasheets for details.

4.4 Power Rails

Power rails provide a low resistance path from power management devices to IC pins. Both AHL devices have two power rails or three if VDDIO is chosen to be < 3.3V. In addition there are multiple VD supply and Vcore pins in a mixed sequence, see the datasheets for pin configurations. This makes routing signals over a layer of power partitions a possibility. The issue arises when the stack-up shown in Figure 2 Option 1 is chosen. With many interlaced power rails, routing signals over a single power partition becomes harder. One solution is routing high speed signals that need a controlled impedance on a layer with an adjacent ground layer and slower signals on the layer over the power planes. Another possibility is to try Option 2 and use routed power to each pin. Vias when using routed power are not problematic because their self inductance hinders the propagation of supply noise.

4.5 AHL decoupling

AHL has normal decoupling requirements covered by Good Signal Integrity Practice in the section for Power Rail Decoupling. A bulk capacitor is connected to the output of the power management circuit with a bypass cap placed by each power pin. A recommended EMI layout technique is shown in Figure 4. In this example, the chip is on the top layer and a VDDVD pin is shown. The EPAD is mirrored on the top and bottom layers. A minimum length trace connects the pin to a via to the bottom layer where power is connected. A 0402 1µF capacitor is connected by a short trace to an image of the EPAD pad directly under the device pin. The capacitor pad is on the EPAD footprint. The bottom layer EPAD is connected to the EPAD on the top layer through multiple vias. The traces are directly under each other and the via in the two views is the same one.

This design has several benefits. First, the bypass cap is as close to the chip as possible minimizing loop inductance. Second, putting the cap on the bottom makes more room for routing signals on the top layer. Lastly, a benefit that is most important for EMI: the area of the bypass loop current is the smallest, this is an important EMI concept. Radiated emissions are proportional to the area of a current loop; in this case, the loop is vertical, and the width of the loop is the thickness of the board.

The last component of decoupling is a ferrite bead located between the bypass capacitor and the bulk capacitor for each power rail. A ferrite is not needed for each power pin if it is on the same rail. A ferrite is not needed for each power pin if it is on the same rail. Ferrite beads serve two purposes. The first purpose is to isolate power rails that share the same potential. This keeps noise from coupling from one supply rail to another. The second and more important for EMI reduction is that it forces more current through the bypass capacitor by making the long loop through the bulk capacitor higher impedance. *Note:* The ferrite bead should be located close to the bypass cap, but this is not critical.

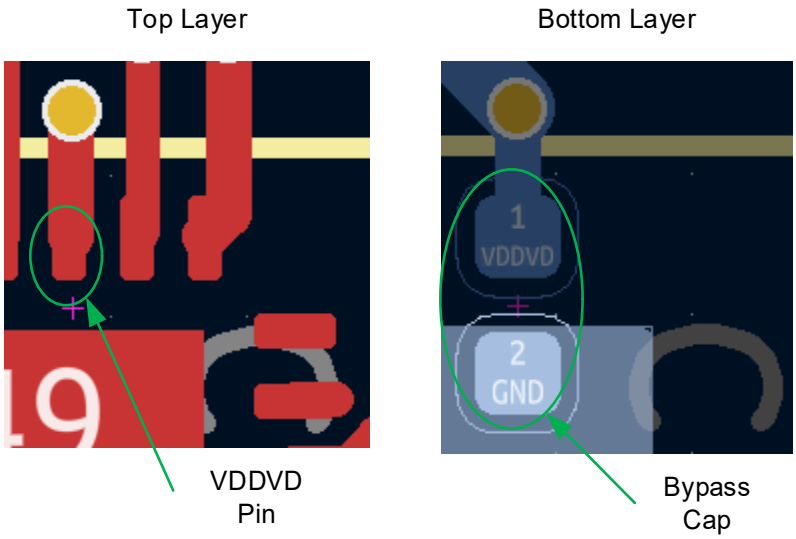

Figure 4. Bypass Capacitor Layout

5. Self Testing Features

AHL devices have a few hardware features that can facilitate self testing. The RAA279971 device has a built in video pattern generator that can create 10 different video patterns without an external source. The pattern can be selected and enabled or disabled through user firmware or TW_Terminal. Figure 5 shows the Encoder window with both the Test Pattern drop-down list and the Enable checkbox circled in red. The user can further adjust the Y, Cb, and Cr values to achieve a signal magnitude similar to the end application. These adjustments are marked in green. Figure 7 shows Pattern 5 displayed on and LCD panel.

Renesas EMC testing used Pattern 5 and default gain. Pattern 6 is not a realistic video pattern for EMC testing.

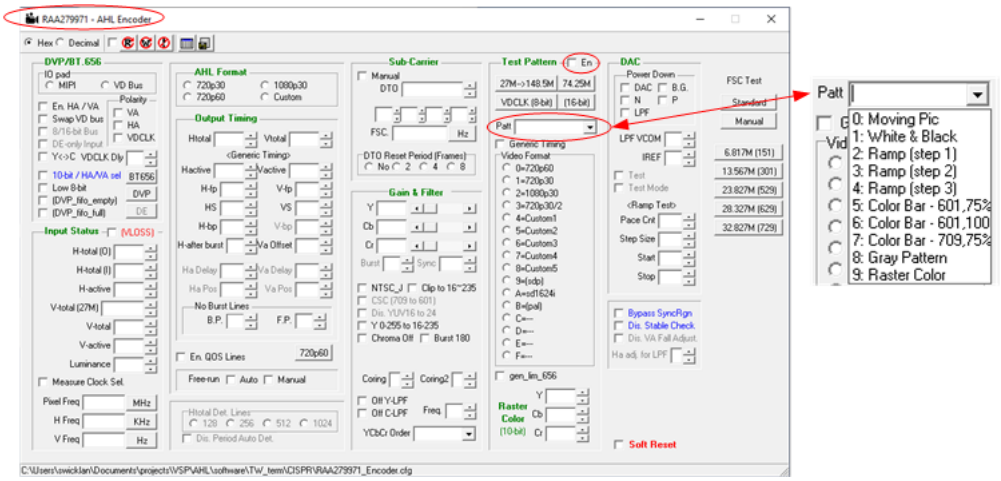

Figure 5. Test Pattern Activation

It has 100% color saturation that often causes clipping of the signal. Clipping the signal creates higher frequency components that do not exist in a properly adjusted system and should not be used.

Test pattern status can be monitored in the decoder without an LCD panel by reading sync, color status bits, and AGC gain in the decoder. Even with an LCD panel, it is recommended to monitor AGC gain to ensure that the system is working properly and the test signal has a realistic magnitude. Gain values should be between 16 and 240. Figure 6 shows the location of these in the TW_Terminal decoder window.

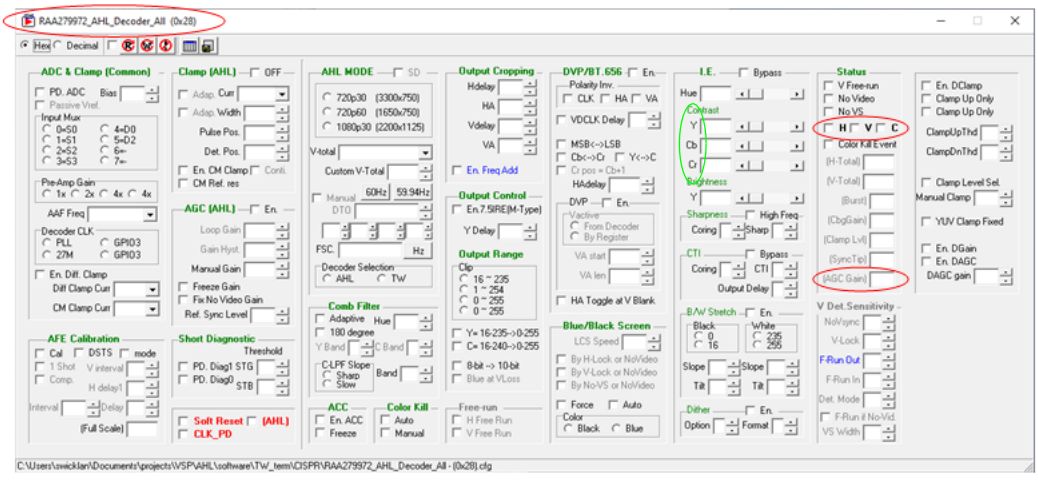

Figure 6. Test Pattern Status

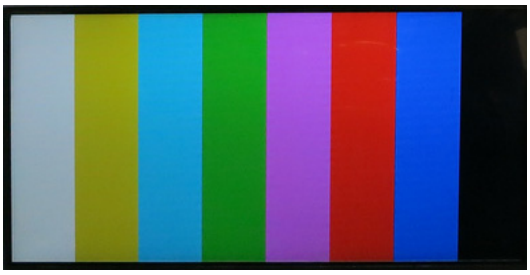

Figure 7. Color Bar Test Pattern

The user always has the option of writing custom firmware for EMI testing. The registers mentioned in this section are described in the datasheet for the AHL encoder and decoder devices.

6. EMI Testing

As mentioned in this application note, there are several tests required for a system to be fully EMI compliant. The tests are system level and designed to test a product as it would be installed in an automobile, and the final result is a tested system that shows AHL does not present any unusual problems.

6.1 CISPR25 Testing

The test is comprised of three different configurations. Radiated Emissions that are measured in three locations, one meter from each board and one meter from the center of the cable. Conducted Current Emissions is measured with an inductive probe in two locations, 5cm and 75cm from the DUT. AHL has two DUTs, the Tx and Rx boards creating four measurement locations. The last test is Conducted Voltage that measures the noise coupled from the system to the wiring harness of a car; this test is done through a LISN that provides a 50Ω test port connected to a spectrum analyzer. This connection can be a single connection to the Rx board if it passes power to the Tx board, or each side can be powered separately requiring measurement of both DUTs. Figure 8 shows a schematic level view of testing.

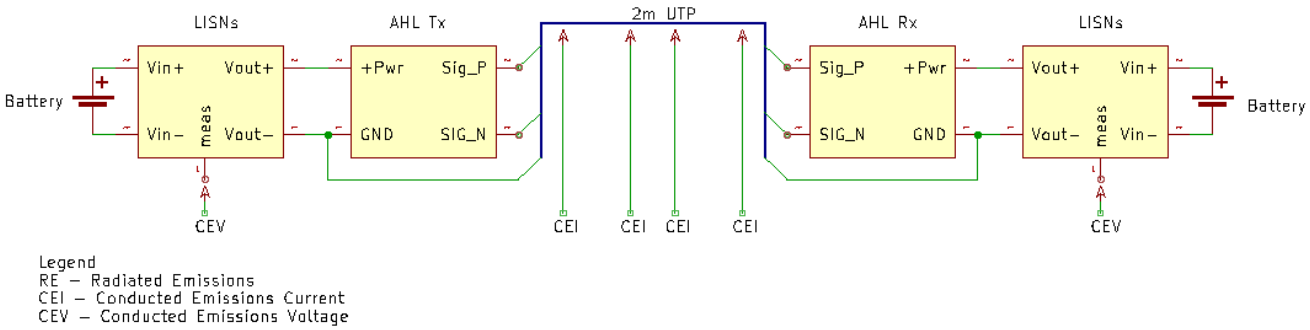

Figure 8. CISPR25 Emission Setup

For noise to radiate, a frequency source coupled to an antenna is required. The antenna could be a component with parasitics, a section of trace, or a current loop on a board. These emissions are largely eliminated with good signal integrity practice. Following the recommendations in sections Good Signal Integrity Practice and AHL Specific Recommendations should take care of these.

Conducted emissions sometimes require specific schemes to prevent noise from coupling onto the power harness and between signaling boards. On AHL, DUTs ferrite beads were added to boards between the power connector, the board power, and ground planes, which is shown in Figure 9. Lcev was added on both V+ and V- paths.

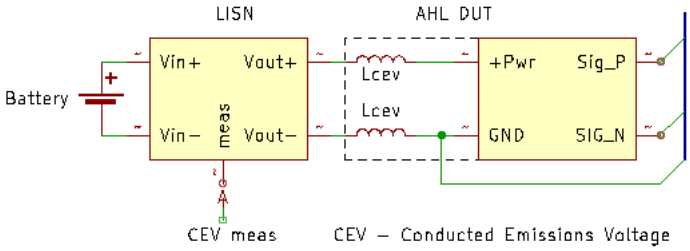

Figure 9. Conducted Voltage Mitigation

The ferrite beads increase the AC impedance of the path to the battery forcing more of the voltage noise through the decoupling capacitors in the power management circuit. The ferrite beads should be between 200 and 500Ω at 100MHz and rated to handle the total current on the respective board (or both boards if there is a single harness connection).

The Conducted Current Test measures common mode noise on the signal cable. Noise can be passed from power rails and ground to the signal cable through the AHL signal pins. Common mode noise can also come from mode conversion of the AHL signal because of either component mismatch in the termination circuit or poor signal integrity practices. To mitigate common mode noise, a common mode choke was added to the signal path, which is shown in Figure 10.

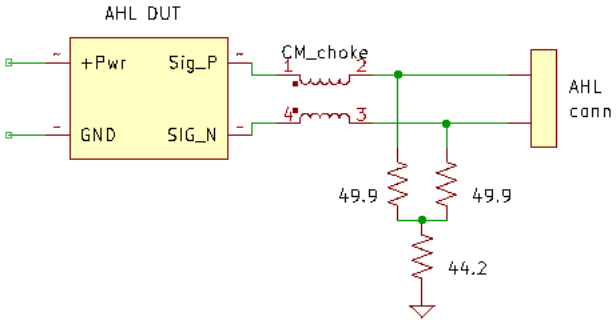

Figure 10. Common Mode Current Mitigation

The common mode choke has an impedance Zcm that is in series with Rcm. Common mode noise is reduced by this voltage divider before it reaches the cable. *IMPORTANT:* The cm choke must be between the termination and the IC.

6.2 BCI Testing

In Bulk Current Injection (BCI) testing, a specified magnitude of noise current over a swept frequency range is magnetically coupled onto the signal cable. AHL was tested to ISO 11452-4, Level 4 using the substitution method. There are three positions for the injection probe required for this test. A full frequency sweep is done at each position. The test requires the system to operate normally at each specified noise frequency. Because AHL is a video transport system, testing requires a setup with an LCD panel to observe video performance. A camera records the LCD condition and transports it out of the test chamber so that it can be observed throughout the test.

In a video system, the failure criteria is not a simple threshold. While a total loss of picture is clearly a failure, some noise on the LCD might be allowed. The criteria chosen should be clearly documented in the certification report. Figure 11 shows three different severities of noise. *Note:* These images are examples displaying directly injected noise and not actual BCI test results.

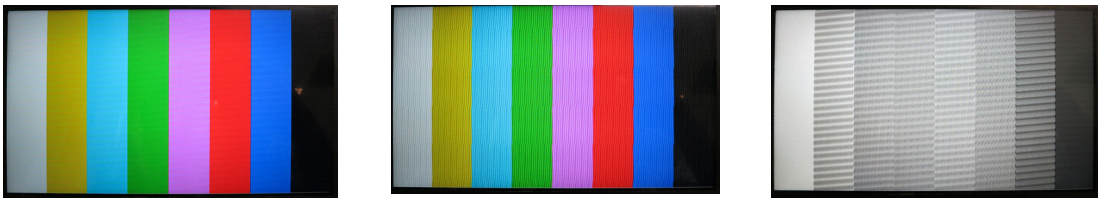

Figure 11. Levels of LCD Noise

In the Slight Noise image, darker horizontal lines are visible, and the color bars and colors are clearly visible. The image is likely considered a pass. The Severe Noise image has significant horizontal lines and the color is lost. The basic outline of the color bars is visible; most often, this is a clear fail. The case for Moderate Noise image is not so clear. Noise is visible, but the colors and the shapes are mostly intact. Cases can be made that this is either a pass or fail.

A key component in reducing BCI noise is a common mode choke. Fortunately the common mode choke used for CISPR25 common mode current mitigation, Figure 10 reduces BCI generated noise as well. No additional components are needed.

6.3 Transmitter Power

It is a common practice to carry power to the AHL transmitter board through the same harness as the video signal. In this type of system, the designer must mitigate the BCI current on the power, ground, and signal lines. BCI noise on the power rails can couple to the video signal on either the transmit or receiver boards causing a video failure. A common mode choke on each board of the appropriate power rating can be used, and another solution is having ferrite beads on both ends to reduce noise. This approach would reduce both differential and common mode noise, which is preferred because there is no need for any AC signals on power lines. Either scheme works making the decision one of cost: two common mode chokes versus four ferrite beads.

7. EMI Component Strategy

To lower EMI, a number of strategies have been discussed in this application note. Figure 12 shows the typically added components for EMI testing. The 49.9Ω differential termination resistors and 0.1µF DC blocking capacitors are not EMI specific but are required for every AHL design. They are shown because their position relative to the EMI components is critical.

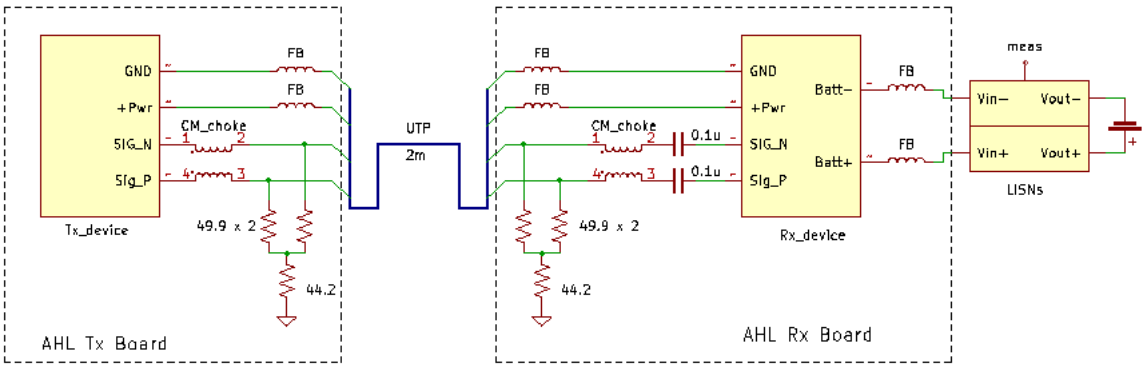

Figure 12. EMI Mitigation Components

EMI component values are not shown because they are design dependent. Guidelines for picking components are discussed in sections Good Signal Integrity Practice and AHL Specific Recommendations.

8. Summary

In summary, AHL devices do not present unusual problems for EMI compliance. Good signal integrity practices must be followed. A pair of common mode chokes required on the video signals are the only EMI components added. Additionally, power lines must be addressed, and ferrite beads are normally required to reduce the noise reaching the wiring harness.

9. Revision History

Revision	Date	Description
1.00	Dec 5, 2022	Initial release.

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