

The ICL7650S: A New Era in Glitch-Free Chopper Stabilized Amplifiers

Introduction

Op Amps

Historically, the biggest single problem with the application of op amps has been the input offset voltage. This is indicated by the fact that almost all important op amps from the μ A741 and LM101 on have offered offset null adjustment pins, special screening to low offset voltage values, and/or internal V_{OS} trimming (laser or Zener-zap). Also consider the extensive series of specifications devoted to its variability with temperature, time, common-mode voltage (CMRR), power supply (PSRR), output voltage (A_{VOL}), and sometimes even down to variation of temperature drift with offset null correction. Contrast this with the treatment afforded one other important (error-causing) input parameter, input bias current, which usually gets just a specified value under one set of conditions, a variation over temperature, and a term relating to its matching between the two inputs. If variation with common-mode voltage, power supply voltage, etc., is covered, it is generally only in a "typical curve" buried in the middle of the data sheet.

The answers to this concern have been many and varied. Several modules use chopper stabilization to provide very low offset voltages, although most of these do not provide differential inputs and they also have problems with input frequencies near the chopping rate (see Intermodulation Effects). The devices are typically bulky and expensive, and the two-path approach frequently used (Figure 1) tends to adversely affect settling times; the high-speed path and the

low-speed path will settle to different points unless the pole-zero pairs are extremely well matched. The only monolithic chopper-stabilized devices previously available are probably best described as disappointing and expensive.

Therefore, considerable effort has been expended to improve the offset and drift characteristics of standard op amp devices, and some very good results have been achieved with several bipolar input devices, such as the OP-05 and OP-07. Careful die layout and circuit balance, in many cases combined with internal offset null trimming, bring initial offset voltages under $100\mu V$, and temperature drifts below $0.5\mu V/^\circ C$. Although this is over an order of magnitude better than a good grade of μ A741 or LM101A, there is still much room for, but little realistic hope of, substantial further improvement in this direction. In addition, the requisite screening of parts is expensive, even with currently available levels of automation.

Technology

In the last few years, a new technology, in the shape of CMOS, has entered the analog field, and has led to the introduction of a range of products previously only dreamed of. Most spectacular, perhaps, has been its rapid dominance of the A/D and D/A converter market (Figures 2 and 3). Today very few converter systems are being designed that don't use CMOS devices specifically intended for this purpose, and in most cases they provide virtually the whole function. More recently, CMOS technology has moved into the more traditional building blocks of analog circuits, so that now CMOS versions of the standard bipolar op amps, regulators, and timers are available, with comparable or better specifications, lower power dissipation, and close to competitive pricing (Figures 4-6). However, although these devices have solved many traditional op amp problems. input offset voltage and low frequency noise voltage were not among them. Using the op amp and analog switch capabilities of this CMOS technology, Intersil introduced in early 1979 a new approach to the low offset voltage requirement, the Commutating Auto-Zero or C_{AZ} amp, shown in Figure 7.

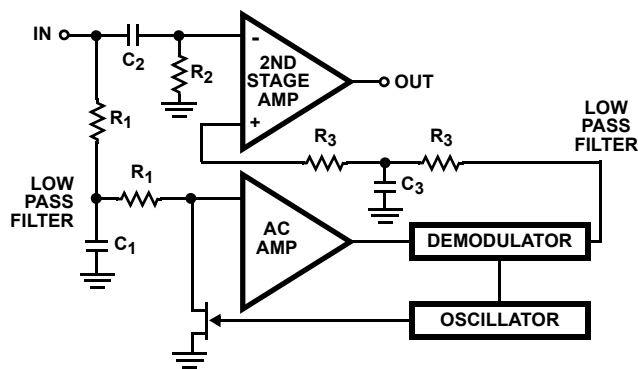


FIGURE 1. TYPICAL MODULE CHOPPER-STABILIZED AMPLIFIER

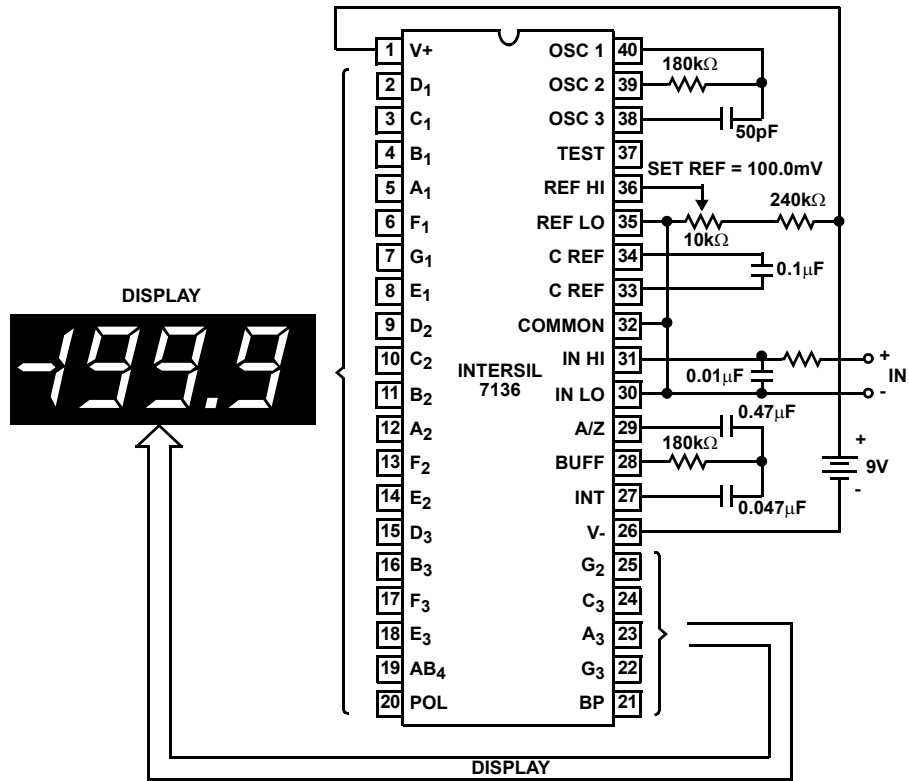


FIGURE 2. LCD DIGITAL PANEL METER USING THE ICL7136 CMOS A/D CONVERTER

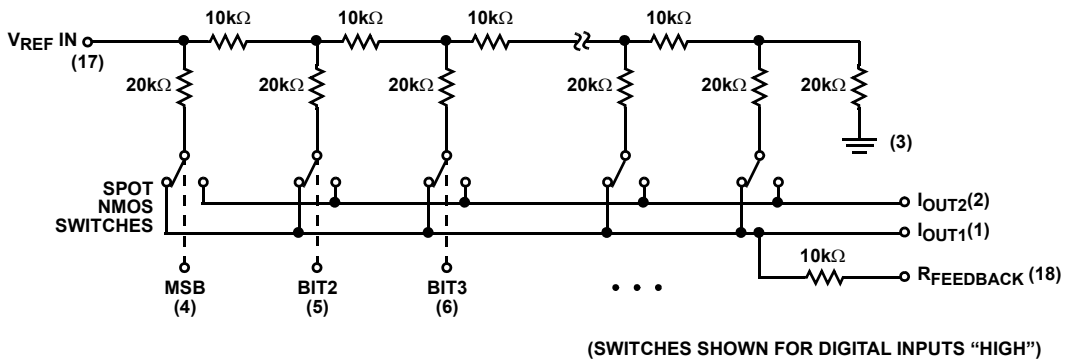


FIGURE 3. CMOS D/A CONVERTER FUNCTIONAL DIAGRAM (AD7541)

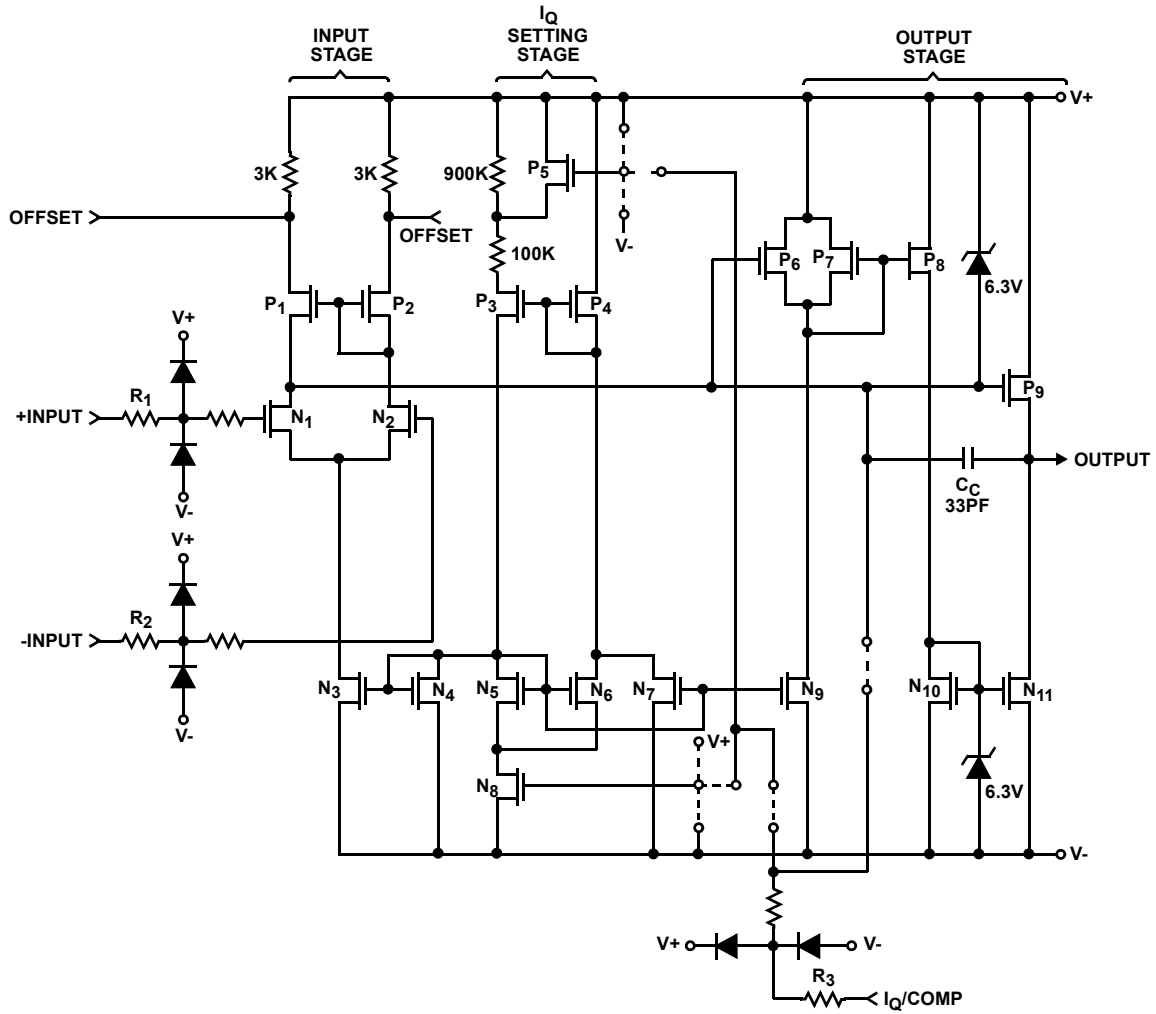


FIGURE 4. CMOS OP AMP SCHEMATIC (ICL7611 FAMILY)

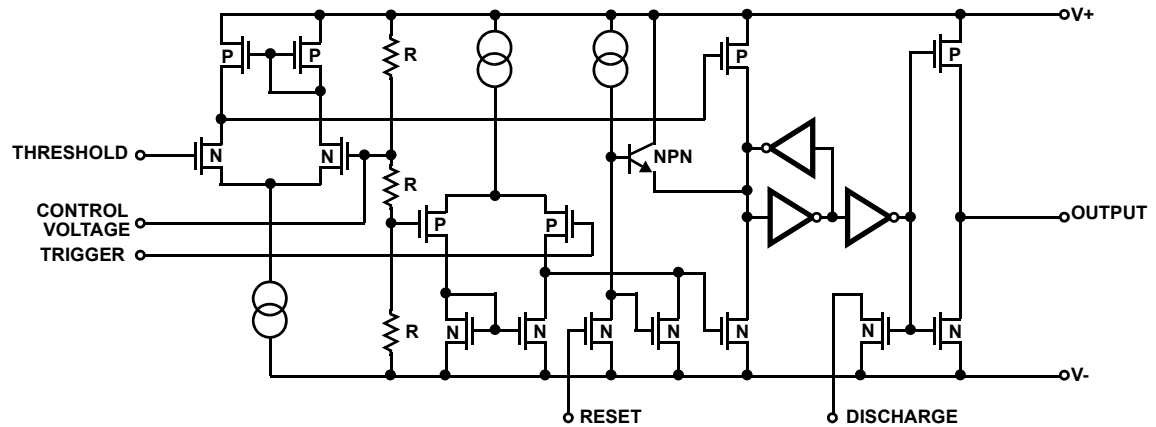


FIGURE 5. ICM7555/7556 CMOS SINGLE AND DUAL TIMERS

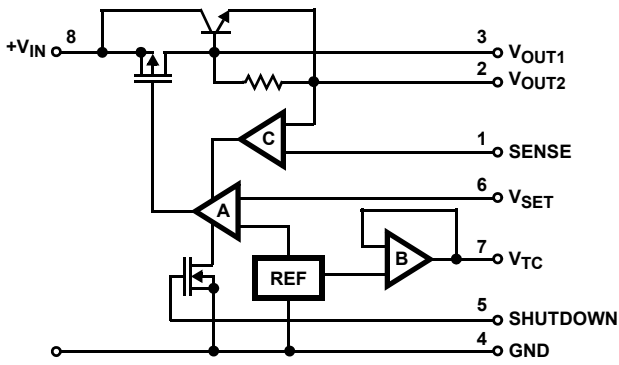


FIGURE 6. FUNCTIONAL DIAGRAM OF THE ICL7663 CMOS REGULATOR

These devices at once became the best monolithic amplifiers available in terms of offset voltage (at $5\mu\text{V}$) and time and temperature drift. They utilize two internal op amps, one active while the other auto-zeroes itself into an external capacitor. Upon commutation, the roles change and the active op amp uses its capacitor to cancel its offset. Two capacitors are needed, but the values and characteristics are not critical. Although offering three orders of magnitude improvement over the input characteristics of the $\mu\text{A}741/\text{LM}101\text{A}$ type, and nearly two orders of magnitude over the best bipolar devices in offset and drift, the C_{AZ} principle has some disadvantages. The input current does not exploit the CMOS capability fully, and there is appreciable spiking at both the input and output (Figure 8). This can be largely removed by filtering, but that limits the available bandwidth.

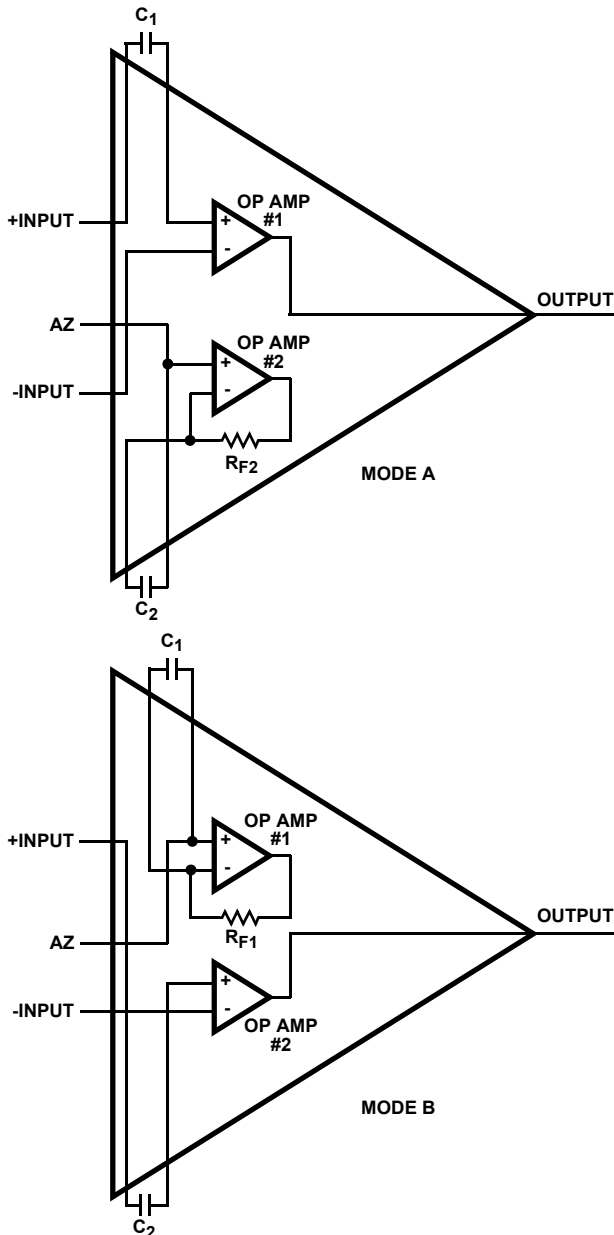


FIGURE 7. ICL7600/ICL7601 COMMUTATING AUTO-ZERO (C_{AZ}) OPERATIONAL AMPLIFIER SHOWING TWO-CYCLE OPERATION

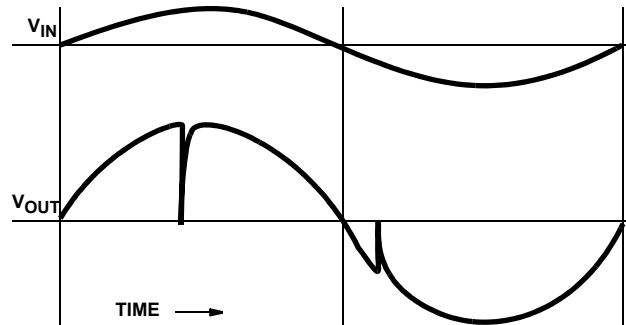


FIGURE 8. OUTPUT SPIKES DUE TO COMMUTATING OPERATION

Synthesis

Intersil therefore decided to try to overcome all these problems by applying the capabilities of CMOS technology to the principle of the chopper-stabilized amplifier. The result is the ICL7650, whose Functional Diagram is shown in Figure 9. The use of a single full-time main amplifier avoids any output glitches, and input switching glitches are minimized by careful area- and charge-balancing on the network of input switches. The chopping operation is performed by means of a nulling amplifier, which shares one input with the main amplifier. The other input is switched alternately between the two main amplifier inputs (Figure 10). When the inputs are shorted, its output drives a null point on itself, and when the inputs are across those of the main amplifier, it drives a null point on that amplifier. The two null points are the back-gates (often called “body connections”) on the mirror transistors of the input stage, and by bypassing these to the equivalent point on the other leg with external capacitors, a simple low-leakage automatic offset null arrangement is achieved. Full differential input capability is retained, and the impedances on the two inputs are well balanced. The input stage legs are merged, as shown in Figure 11, to reduce the input noise and improve balance and high-frequency CMRR, etc.

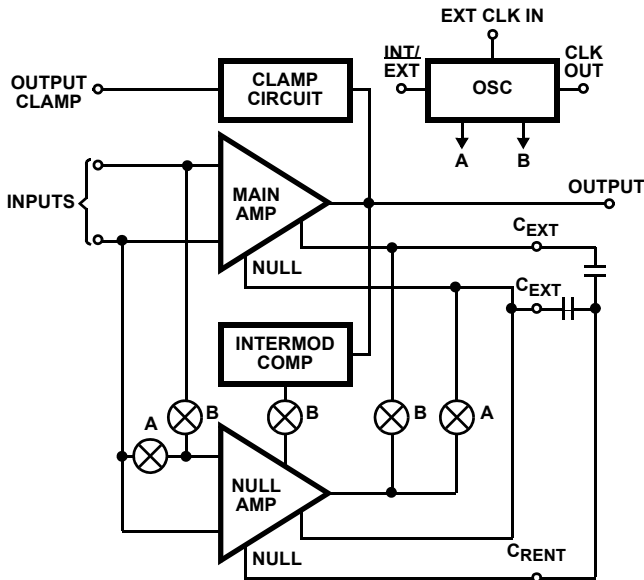


FIGURE 9. FUNCTIONAL DIAGRAM OF ICL7650S

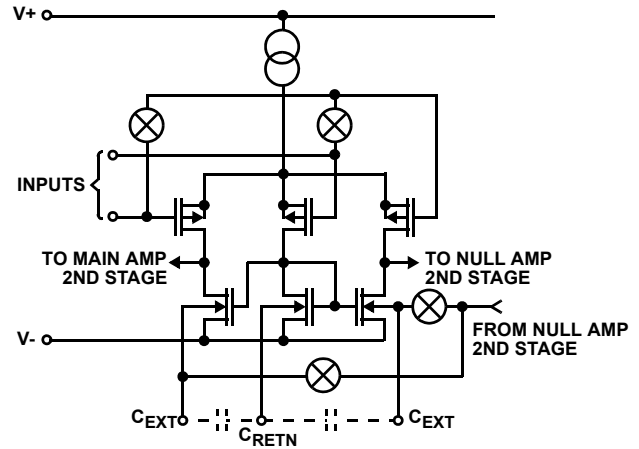


FIGURE 11. THREE-LEGGED INPUT STAGE (SIMPLIFIED)

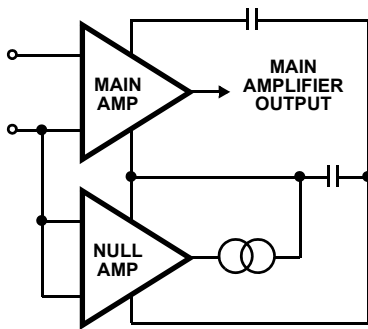
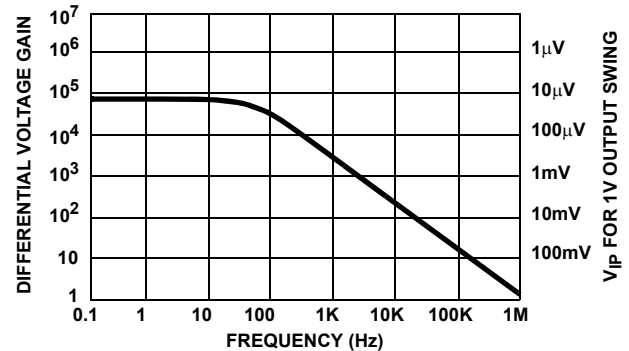


FIGURE 10A. NULLING ITSELF

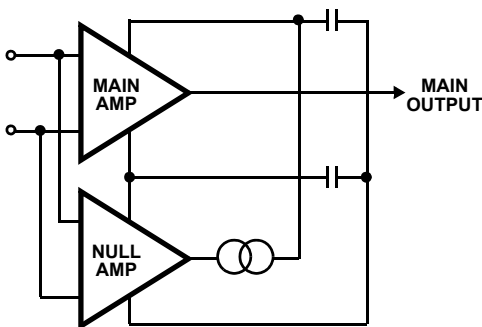


FIGURE 10B. NULLING MAIN AMPLIFIER

FIGURE 10. TWO PHASES OF NULLING OPERATION

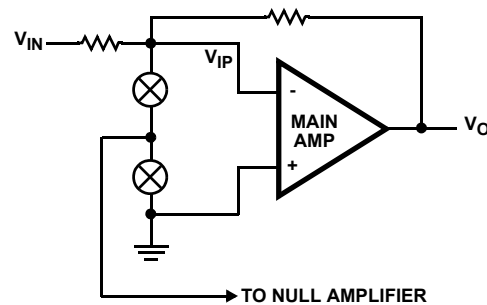


FIGURE 12. GAIN ROLL-OFF AND INPUT VOLTAGE (MAIN AMPLIFIER ALONE WITHOUT NULL SYSTEM) VS FREQUENCY

The circuit automatically provides correction (at DC) for CMRR, PSRR, and AVOL, to the same level as for VOS (typically under 1mV), and the I_B remains in the low pA area, set by the leakage of the input switches (also acting as protection diodes) and the small net charge injection. The latter is doubly-balanced both by careful device matching and by the excellent recovery of any residual injection, due to the equipotential nature of the inputs. The open-loop gain bandwidth product and the slew-rate are set purely by the main amplifier. The null system time constant is controlled by the effective g_m to the output of the nulling amplifier and the external capacitors, and is readily controlled to be much longer than the chopping period. In addition, the "injection" of the nulling signal into the first stage of the main amplifier ensures that the pole-zero match at this cross-over point is no problem.

Intermodulation Effects

Two residual problems remain with the usual chopper-stabilized amplifier circuits. One of these is the intermodulation between applied signals and the chopping frequency, as mentioned earlier. This arises because the main amplifier has finite gain near this frequency, and so develops a small differential input signal to sustain the requisite output (distinct from any DC offset voltage). This signal is, of course, at the signal frequency, and has an amplitude determined by the gain roll-off characteristics (Figure 12) and the signal amplitude, and will be seen by the nulling circuit as an error signal equivalent to an input offset voltage. This circuit will then attempt to null out the input signal during the active null time. If the difference in frequency between the signal and the chopping rate is large compared to the null circuit time constant, this attempt will essentially fail, since the proposed direction of change will vary between (or during) each null time in such a way to lead to little net resultant. On the other hand, if the signal and chopping frequencies are close together (in terms of the time constant), the null circuit will respond at the beat frequency, leading to two undesirable results. First, the gain and phase characteristics will be disturbed in the neighborhood of the chopping frequency, since the amplifier input signal will be partially reduced, with some delay. Second, the effective input will include a component at the beat frequency, not present in the true input.

The ICL7650 minimizes this problem by the simple expedient of introducing a compensating dynamic offset voltage in the nulling amplifier. This is possible since, at the frequency range of interest, the AC signal that causes the problem is a function only of the compensation capacitor, the input stage g_{mS} , and the output signal amplitude. By adding another capacitor from the output signal of the main amplifier to the corresponding summing point in the nulling amplifier, with a value which is correctly scaled to allow for the ratio of the input stage g_{mS} , and connecting it only during the time when the main amplifier is being nulled, the nulling amplifier does not see the input-related signal at the main amplifier. Thus, no nulling signal is generated, and no beat frequency is generated. The required matching of the g_m and capacitor values is readily achieved, since they are all on a monolithic die, and the result is a device with virtually no interference between the normal operation of the main amplifier and the chopping action of the nulling amplifier.

Overload Effects

The second traditional problem with chopper-stabilized amplifiers relates to their behavior under overload. Once again the problem arises through the presence of an input signal on the main amplifier which is not due to the input offset voltage. In this case, the presence of a large signal in the system leads to the output running up against the supply rails. Under these conditions the amplifier no longer has control, and the voltage at its input becomes only a function of the feedback network, the input signal, and the output swing limit of the amplifier, as shown in Figure 13. The nulling amplifier, however, has no means of knowing that this is the problem, and will attempt to "rectify" it by driving the null network to remove this input signal. This effort cannot succeed, and in fact will increase the

depth of overload. If this condition is maintained long enough (compared to the nulling time constant), the null circuit itself will also be driven to its limit. Thus, when the input signal returns to an inrange value, the input offset voltage will be skewed heavily to one side. If the nulling range of the amplifier exceeds the input signal range, frequently the case in the high-gain applications common for such devices, the output will remain stuck at the supply rail until the null circuit has almost recovered. Since the null amplifier driving signal may be quite small, recovery may take a long time.

Several possible methods can be used to combat this effect. One is to detect the output limiting condition, and to stop the chopping operation during the time that this does (or can) occur. This has two disadvantages. It may not be possible to predict such overrange conditions, nor easy to detect their occurrence either. Further, even if this is done successfully, the nulling system will be unable to correct the inevitable loss of true null caused by leakage currents on the null points, etc. Thus, an extended overrange interval with the chopping stopped can leave the null badly disturbed, perhaps as much as when the chopping is active. Nevertheless, in situations where an overrange occurrence is predictable or readily detectable, and lasts only for a limited time, the technique is very useful. The ICL7650 facilitates this form of overload effect amelioration by providing an EXT CLK IN pin (in the 14-pin versions), which can be held "low", stopping the chopping action in a position where no capacitor charging can occur, and by allowing judicious use of the CLAMP pin (see below) as an overload detector.

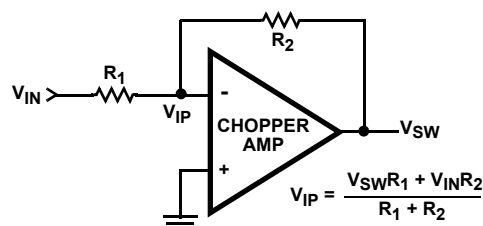


FIGURE 13. VOLTAGES IN INVERTING AMPLIFIER WITH OVERLOAD INPUT

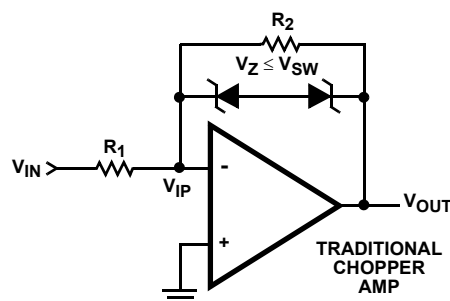


FIGURE 14. AVOIDING OVERLOAD WITH ZENER CLAMPS

The other technique for avoiding the overload problem involves adding a nonlinear element to the feedback network, so that overrange inputs do not cause the output to limit against the supply rail. One possible way of doing this is to parallel the feedback element with a pair of Zener diodes which conduct just before the limiting would occur, as shown in Figure 14 for the inverting configuration. The noninverting arrangement is

similar, but only reduces the gain to unity after the Zeners conduct. One disadvantage with this circuit is that the Zener voltage is quite critical, especially if the supply voltage variation is significant and the maximum allowable swing is desired. The ICL7650 avoids both of these problems by providing a CLAMP pin which will conduct current in the appropriate direction whenever the output voltage gets within a few hundred mV of either supply. The internal schematic is indicated in Figure 15A, and the output current characteristics as a function of the voltage margin to the supply rails in Figure 15B. The leakage currents due to the small N and P channel MOSFETs are negligible, and they can only be turned on if their common sources, tied to the output, get close to the relevant rail. If this pin is tied to the inverting input to the amplifier, and the impedance at this point is adequate, the desired limiting is readily achieved, with no disturbance to the null network, and usually negligible effect on the input bias current. The only penalties paid for this overload protection are a slight limitation on the output swing, and an increase in the input current on the inverting input when the output swings close to the rail. Also, the input circuit is not quite so easily guarded on a PC board if the CLAMP pin is used.

Device Characteristics

The net result, then, of all this technical wizardry is an op amp with quite remarkable characteristics. The input error- related parameters are unprecedented in a monolithic device, and rare indeed against all competitors, with a V_{OS} of under $5\mu V$ (typically under $1\mu V$) and an input bias current of no more than $10pA$. The V_{OS} value is maintained over the full range of the power supply, input common-mode, output swing, and temperature ranges. In other words the PSRR, CMRR, A_{VOL} , and dV_{OS}/dT or drift are all virtually unmeasurable, and well over 120dB, 120dB, 140dB, and under $10nV/^{\circ}C$, respectively. The long-term drift, which we can consider to be very low frequency noise (as indeed it is from a device physics point of view), is also undetectable.

The other device characteristics also compare favorably with those of the $\mu A741$ and LM101 type. The Gain-Bandwidth product and slew rate are both about 3 times higher, at 2MHz and $2.5V/\mu s$ respectively, the supply current is about the same, at 2mA (3.5mA Max), the stability margin is similar, and the output swings between the supply rails. The only significant limitations on its use are the reduced supply voltage range ($\pm 8V$ Max) and the $10k\Omega$ load limitation. These are becoming less important with the growth of $\pm 5V$ analog systems, and also can be readily side-stepped, as shown in the Applications section below.

And to cap it all, this paragon of op amp virtue is a moderate-sized monolithic die made with a high-yielding mature low-cost process, so the device cost is quite low.

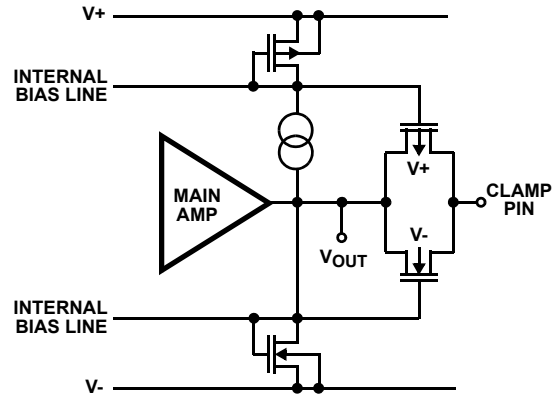


FIGURE 15A. OUTPUT CLAMP CIRCUIT

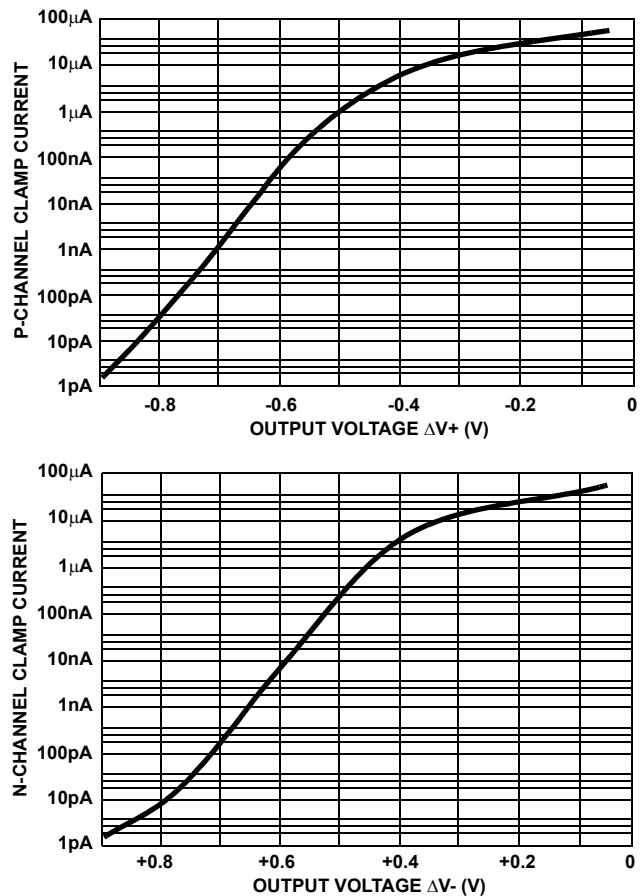


FIGURE 15B. CONDUCTION CHARACTERISTICS

Applications

So much has been written about op amp applications over the last few decades that there is little point in trying to reproduce it all, even with revised specifications and capabilities. The most important point to be appreciated is that in any application where the performance of the circuit can be significantly enhanced by a reduction of input offset voltage and/or bias current, the ICL7650S can be put right to work. Further, any circuit using a null-trimming pot is an immediate candidate for replacement, since the cost of purchase, insertion, initial adjustment, and especially periodic readjustment will generally be greater than the initial small premium for this device and two capacitors. Otherwise, the finite space available here will be used to present the particulars of this substitution as germane to the ICL7650S, followed by the details of some circuits that utilize the specific capabilities of the part particularly well, and some combinations with other devices that concatenate their respective features.

The normal substitution requires nothing but the replacement of any null trim pot with two required capacitors. In the case of the 14-pin devices, the pinout corresponds to that of the LM108 type device, so substitution of the ICL7650S for a (rare) 14-pin LM101/A, LM107, μ A741, OP-05/OP-07, or any similar part, can be done most readily with the 8-pin version. The alternative involves a minor PC board change. If good overload recovery is a requirement for the application, the connections to the CLAMP pin (see Overload Effects) should be made according to the basic configurations of Figure 16. The impedance at the point of attachment needs to be high enough, at least at DC, to permit the worst case input signal to be accommodated within the capability of the CLAMP pin output current, according to the curve of Figure 15B. Usually this is easily managed in the case of the inverting configuration, but in the non-inverting case, some additional input clamping may be necessary. Some alternatives for doing this are shown in Figure 17.

One frequent use of an op amp is as a comparator. This cannot be done with the usual chopper amplifiers because of their terrible behavior under overload conditions, the normal operating mode for an op amp so used (see Overload Effects). However, the optional overload avoidance feature built-in to the ICL7650 allows its use in many of these applications, as shown in Figure 18. The current from the CLAMP pin forces the inverting input to follow the signal input (within the output swing and input common-mode ranges), and the transfer characteristic is essentially a reflection of the characteristic of Figure 15B. The comparison voltage must be capable of absorbing the CLAMP pin current without distress to itself or other parts of the system. Only one polarity of comparison is possible with a high input impedance, but if a low impedance drive input is available, the roles can be reversed to achieve the other polarity. The speed of the circuit is limited to input ramp rates under 100V/s for the most accurate performance, but above this rate the timing errors of most comparators exceed their input offset errors in any case.

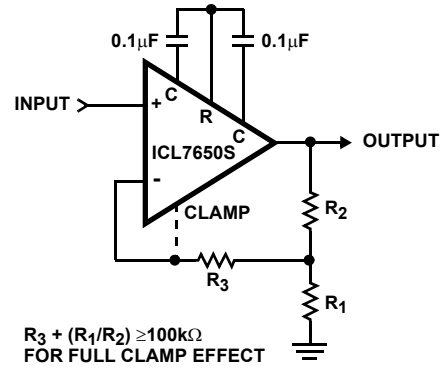


FIGURE 16A. NON-INVERTING AMPLIFIER

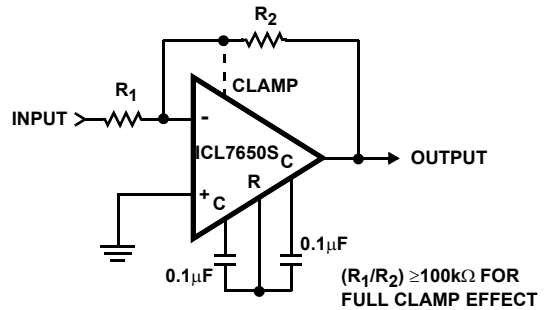


FIGURE 16B. INVERTING AMPLIFIER

FIGURE 16. NON-INVERTING AND INVERTING CONFIGURATIONS WITH (OPTIONAL) CLAMP CIRCUIT CONNECTION

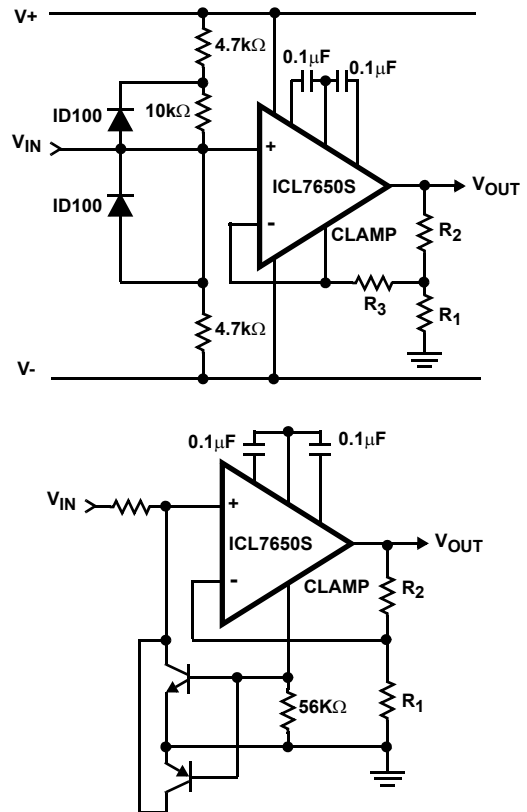


FIGURE 17. SOME OTHER CLAMPING CONFIGURATIONS FOR NON-INVERTING AMPLIFIERS

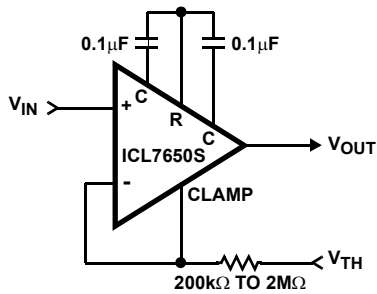


FIGURE 18. LOW OFFSET COMPARATOR

The usual instrumentation amplifier configurations work extremely well with the ICL7650. The standard three op amp configuration (Figure 19) has unbeatable CMRR, a function only of the resistors in practice. With a differential input A/D converter, such as the Intersil ICL71X6, 71X7 or 7135, just two ICL7650S will maintain high differential gain without any common-mode gain, ideal for pre-amplification of signals from such bridge-type transducers as strain gauges, etc. The arrangement is shown in Figure 20. This also works well with thermocouples whose shielding is grounded at the sensing end, especially in a noisy environment. Note that the offset and drift of the ICL7650 will contribute less than 1°C initial error and less than 0.2°C drift error to an absolute Platinum - Platinum/Rhodium Type S thermocouple between 0°C and 1750°C, or to a Type B thermocouple between 500°C and 1820°C (over the operating temperature range of the

ICL7650). This is less than the errors associated with standard thermocouples themselves. Naturally, to realize this performance, all the other little thermocouples between the leads, the PC board, any IC socket, and the other components, etc., will have to be carefully handled. This topic is discussed in Achieving the Full Benefits.

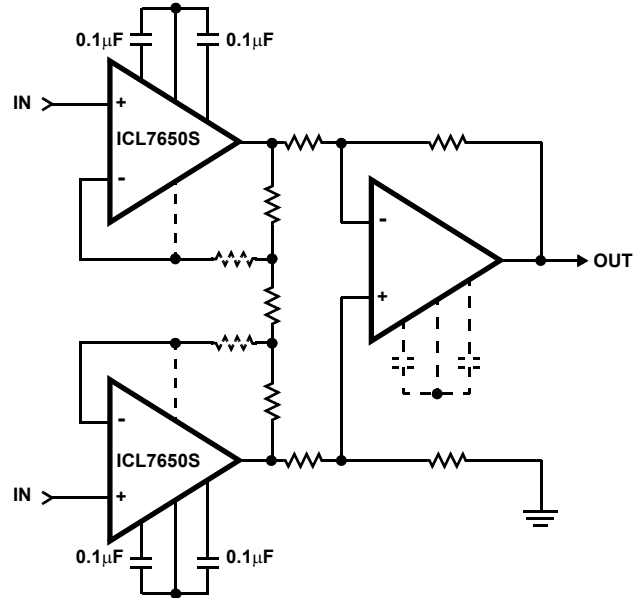


FIGURE 19. 3 OP AMP INSTRUMENTATION AMPLIFIER

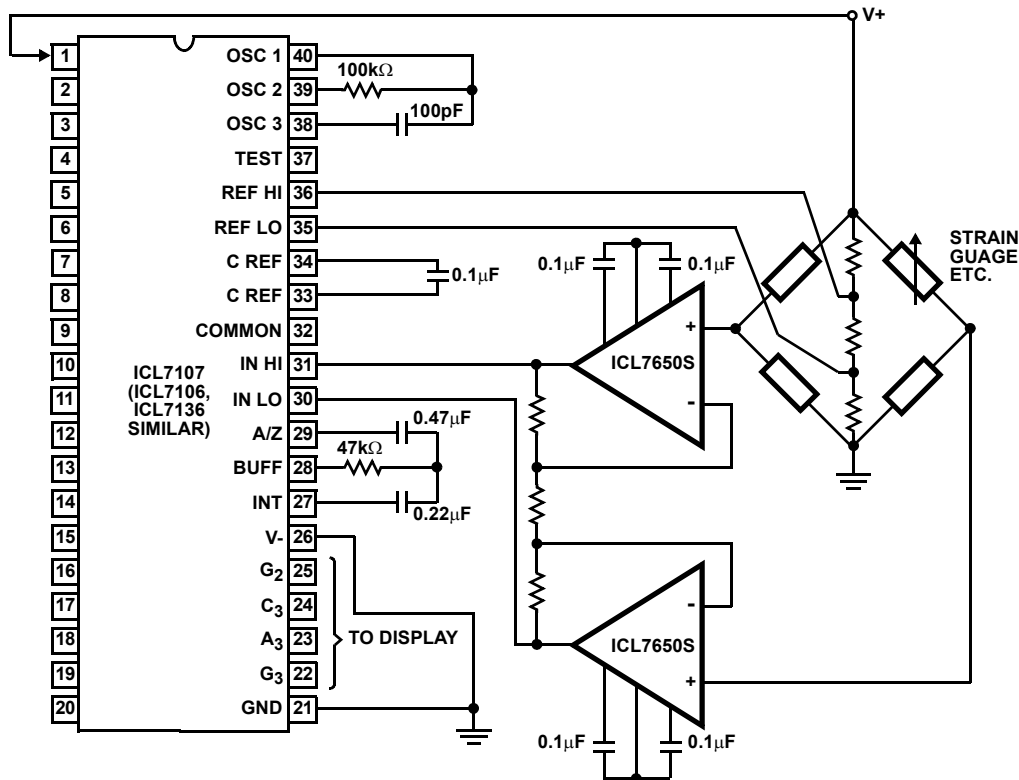


FIGURE 20. 2 OP AMP DIFFERENTIAL PREAMP FOR ICL7106/7 FAMILIES

Conventional logarithmic amplifiers have very high dynamic ranges in the current input mode, but in the voltage input mode they end up severely limited by errors associated with the input offset voltage of the input op amp. Two methods are available to combat this problem with the ICL7650. The device itself may be used as the main amplifier, as suggested in Figure 21. This will give a wide dynamic range of close to 6 decades. However, this arrangement lacks the built-in temperature compensation and scale factor adjustment of such monolithic log amps as the Intersil ICL8048. These can be combined with the same dynamic range enhancement by using the ICL7650 to offset null an ICL8048, as shown in Figure 24. The time constant of the nulling network needs to be high enough to avoid loop stability problems. The input current of the system will not be degraded by this configuration, so 6 decades of dynamic range will be available in both voltage and current input modes.

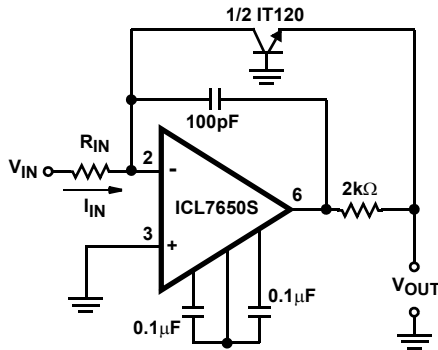


FIGURE 21. BASIC LOG AMPLIFIER

Although the overall performance of the ICL7650 is unprecedented, there are some parameters for which other devices remain better, and it does have some limitations. We have already mentioned the supply voltage limitation, for which the promised circumvention appears in Figure 22. The two JFETs have I_{DSS} values well above the supply current requirement of the ICL7650S, and so operate close to “pinch-off”. These “pinch-off” voltages constitute the supply voltages to the ICL7650S, and must meet the specifications required, readily done with the parts listed. By bootstrapping the JFET gates to the output, a follower circuit whose input and output can span the full supply range can be constructed. High voltage JFETs would permit even higher supply voltages. A small amount of high-frequency roll-off is usually needed in the boot-strap to prevent RF instability.

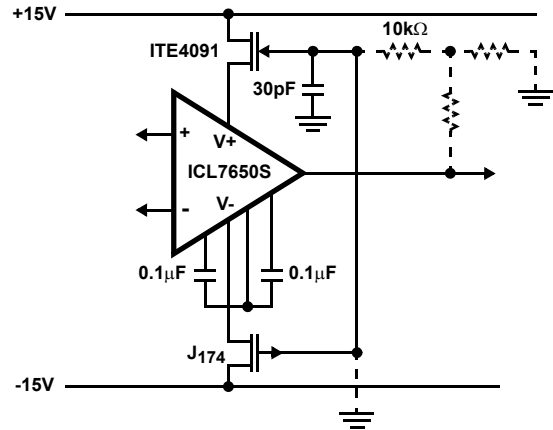


FIGURE 22. OPERATING WITH ±15V SUPPLIES

The output drive limitations may be readily overcome by buffering the ICL7650S with a device such as the μ A741, after the fashion of Figure 23. This has the additional advantage of reducing the dissipation in the ICL7650S due to the load, and the thermal effects associated therewith (see Achieving the Full Benefits). These two circuits may be amalgamated in several ways to combine higher voltage operation with heavy load driving capability, such as those shown in Figure 25. One or more of these can be used to construct a configuration that will act correctly in any inverting or noninverting application, for any gain required. These circuits can be used to substitute for virtually any chopper-stabilized module, and most other standard op amps also, with a substantial improvement in input parameters and no loss in output characteristics.

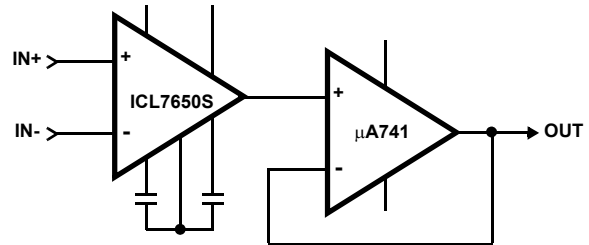


FIGURE 23. USING 741 TO BOOST OUTPUT DRIVE CAPABILITY

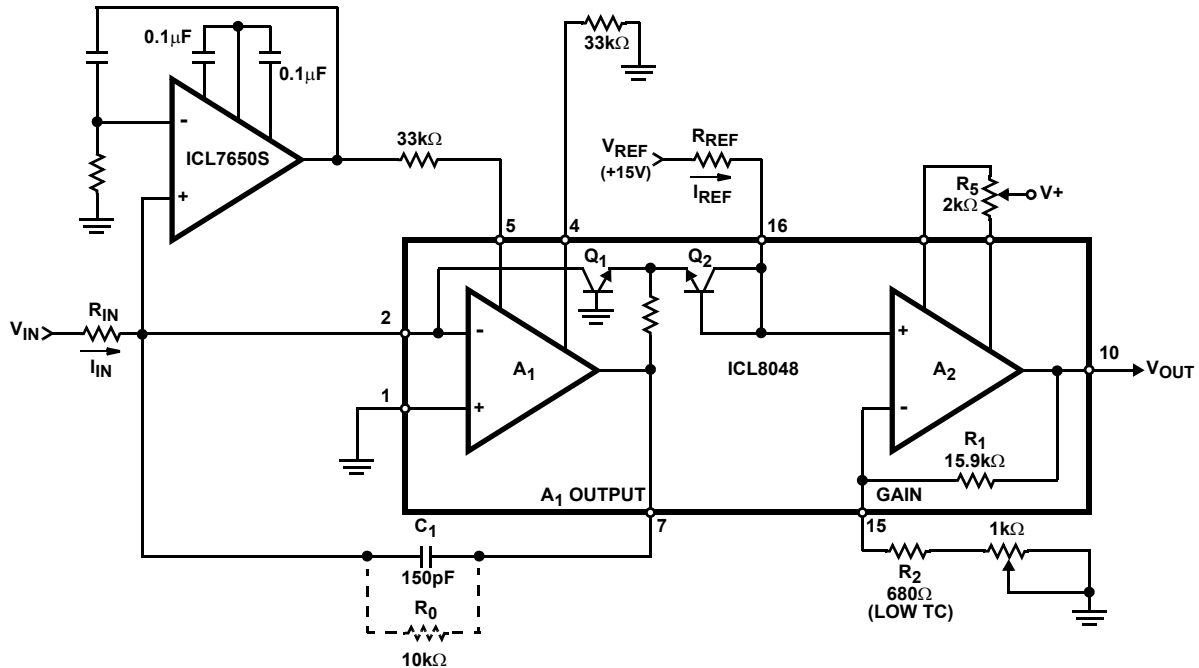


FIGURE 24. ICL8048 OFFSET NULLED BY ICL7650S

The high slew-rate and/or bandwidth of devices such as the HA2500/10/20 and the HA2600/20 families is not, of course, preserved by the arrangements of Figure 25. For these types of devices, the concept used in Figure 23 is preferable. Figure 26 shows two methods of doing this for several high speed devices, and Table 1 gives suitable component values. Note that although the input offset voltage is that of the ICL7650S, the input current will generally be dominated by that of the other device. Also, no protection is provided against overload, and intermodulation is back (see Intermodulation Effects and Overload Effects). These three can be reduced or eliminated by extra complexity in the circuits, at the expense of further loss in generality. Figure 27 shows one method of balancing out the intermodulation terms, and a similar clamp circuit to that of the ICL7650S added externally.

A similar combination of the exceptional low noise performance of the OP-05 (and OP-07) with the ICL7650S is also possible, and incidentally gives the lowest available overall noise performance in any bandwidth from true DC to any other frequency of use with op amps. In this case, the roll-off in the external nulling network should be low enough in frequency to ensure that the cross-over between the two devices does not degrade the performance in the bandwidth of concern. The schematic, in Figure 28, is otherwise the same as that of Figure 26, and Table 1 includes the values for this circuit also. Many other combination circuits have been published in the literature, and the ICL7650S can be used to advantage in the majority of them.

TABLE 1.

DEVICE FAMILY	WORST FAMILY V_{OE} (mV) OVER TEMP.	LOWEST SUPPLY VOLTAGE $\pm V$	FIGURE 26A CIRCUIT				FIGURE 26B CIRCUIT		
			$R_A(\Omega)$	$R_S(\Omega)$	V_S	N_A PIN	$R_A(\Omega)$	N_A PIN	N_G PIN
$\mu A741$	7.5	3.0	82K	2000	-	1	680K	1	5
LM101	10.0	3.0	2M	1M	-	5	1M	5	1
LM118	15.0	5.0	330K	180K	+	5	150K	5	1
LF155, 6, 7 (Note 1)	13.0	5.0	120K	5.1K	+	1	560K	1	5
HA2500 (Note 2)	14.0	10.0	6.8K	100	+	5	62K	5	1
HA2600	7.0	5.0	620K	18K	+	1	620K	1	5
CA3140	30.0 (Note 3)	4.5	1M	10K	-	5	240K	5	1
OP-05	1.6	3.0	1.6M	18K	+	8	2.4M	8	1
OP-07	0.25	3.0	10M	150K	+	8	10M	8	1

NOTES:

1. LF 155, 156, 157 require 12K resistors from pin 1 and 5 to $V+$, in addition to the resistors mentioned above.
2. ICL7650 supplies are $\pm 8V$ Max; HA2500 is not specified, but will work, with supplies under $\pm 10V$.
3. Unspecified; Value inferred from other data.

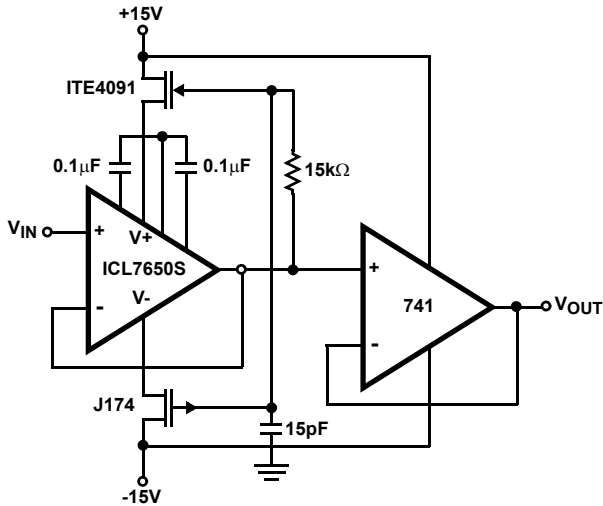


FIGURE 25A.

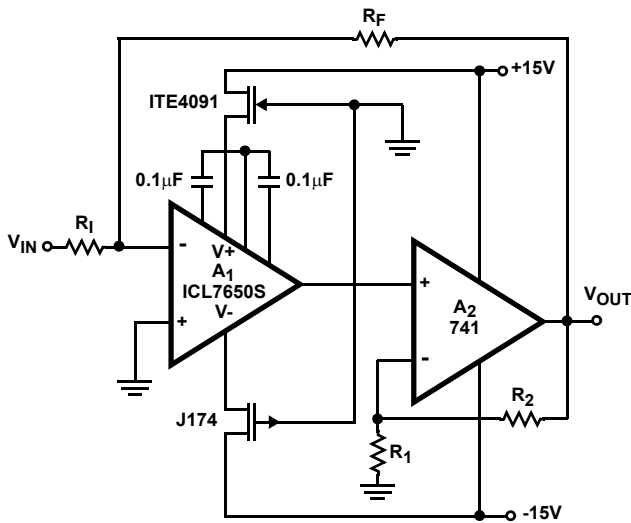


FIGURE 25B.

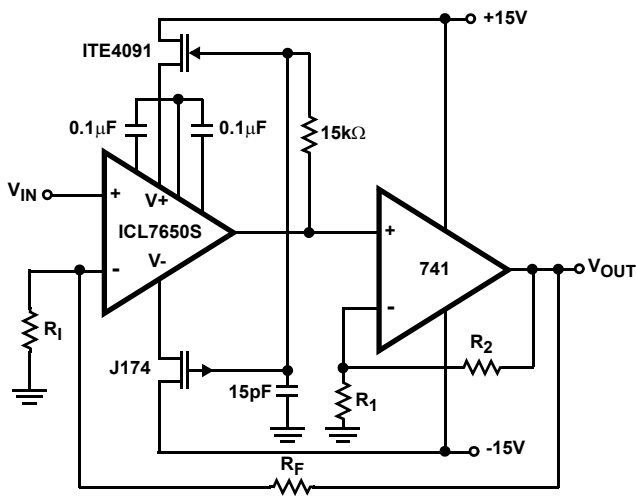


FIGURE 25C.

FIGURE 25. SEVERAL HIGH VOLTAGE-HIGH LOAD COMBINATION CIRCUITS

Achieving the Full Benefits

The ICL7650S brings a new level of accuracy to the analog world, and in doing so exposes a new set of problems and difficulties in the environment of the typical op amp, previously masked by device errors. The standard care taken with ground loops is even more necessary here, and the prevention of PC board leakage is also more important. The pinout on the 14-pin device has been arranged so as to allow easy guarding of the input pins, and the same can be done on the TO-99 device by using a 10-pin outline mounting configuration, as shown in Figure 29. If the CLAMP pin is being used, the configurations of Figure 30 may be found more useful. Careful cleaning with TCE or alcohol, followed by a compressed air blow-dry, is advisable, and an epoxy or silicone rubber coating will prevent subsequent contamination. Careful use of Teflon® or similar standoffs may be helpful in stubborn cases of PC board troubles.

The impedances of the driving nodes for the offset null storage capacitors are quite high, as explained above, and care should be taken in the PC board layout to avoid coupling stray signals into these points. A pseudo guard ring tied to V- could be applied in exceptionally difficult cases. The CAP RETN pin (14-pin parts only) is somewhat less sensitive, but should be treated with respect also.

Some consideration should be given to the capacitors themselves. On initial turn-on, and also if radical changes in common-mode or power supply voltages occur, the voltages on these capacitors must change to the (new) desired values. A capacitor with high dielectric absorption, such as a ceramic type, will absorb back part of the change in charge during the respective holding time during several clock cycles, or even for many seconds, leading to a significant initial (or recovery) settling time. If either of these is critical, a polypropylene capacitor should be used, although in many cases a mylar or similar film capacitor would be adequate. Another disadvantage of ceramic capacitors is that they frequently generate a significant amount of 1/f or "flicker" noise, which will be fed into the system through the null pins. For this reason, it is recommended that a film type capacitor be used, even though any low-leakage capacitor will "work".

The ultimate limitations to any high accuracy DC amplifier are the thermo-electric or Peltier effects in all the thermocouple junctions between dissimilar materials. The junctions of concern to us here are those between the silicon (N- or P- type) and the aluminum metallization on the die, the aluminum to bond-wire and bond-wire to header post or lead frame, and the post/lead to PC board junctions. If all these are at the same temperature, then no problems will arise, since an equal number of identical junctions are interposed on the return path. The power dissipation within the IC die is inherently low, and most applications will not add very much to that, so we can consider the die temperature to be fairly uniform. Thus, the thermocouples out to the bond-wires can be neglected unless a heavy load resistance is applied. The same is reasonably true for the bond-wire to post/lead junction. However, the post/lead to PC board junction can be a serious problem. The thermo-electric coefficient of the usual Kovar-copper junction present here is of the order of $30\mu V/^\circ C$, and the thermal contact between the individual junc-

tions is not very good. A temperature gradient of as little as 0.1°C/inch will lead to an error as large as the typical offset voltage of the ICL7650S! A point-source (power transistor, say) with a 10°C temperature rise must be kept 5 to 6 inches away, and a similar line-source would need to be many feet away. Even air currents from a standard forced-air heating system can cause gradients approaching this level. Similar effects can occur with other circuit elements, although generally their lead materials have lower thermo- electric coefficients.

The cure for these potential problems lies in exercising care in both the circuit design and the board layout. The power dissipation in the ICL7650S should be kept low (use the circuits of Figures 23, 25, 26 for load driving if needed), and power-dissipating components should be kept well away. A cooling fan or blower is undesirable unless an enclosure is used around the op amp and its associated components. and in any case the air flow should not pass over this area after a power-dissipating area. Low thermo-electric coefficient connections should be used wherever possible, and in all cases the PC board layout should emphasize thermal balance in loop paths.

Summary

The ICL7650S represents a significant step-function in op amp performance (one that should not have occurred until 1990, according to one recent Wescon presentation). The design brings chopper-stabilized performance to a new level of availability, while making it virtually transparent to the user. Although it is too early to predict the demise of the trimming potentiometer industry, nevertheless this device and its successors can be expected to replace the need for many of them and their periodic re-adjustment, frequently without increasing the initial cost, and certainly with favorable lifetime cost benefits. The combination circuits suggested here allow an even closer approach to the “perfect op amp” than has ever been available before, and at remarkably low cost.

One side-effect of the remarkable performance potential of the ICL7650S is that several subtle error-causing effects that have previously been largely masked by the inherent errors of the available op amps, are now uncovered. Great care must be exercised to achieve the full performance benefits the device can offer. These caveats do not, of course, apply in cases where a simple replacement of a less accurate or less stable device is contemplated. The high degree of “user-transparency” achieved in the chopping operation promises a minimum of applications problems, borne out by the rapid acceptance of the device in a wide range of applications.

The author would like to acknowledge the design efforts of Lee Evans and Dane Snow in turning the concept of the device into such a magnificent reality, and Andy Wolff for refining, expanding, and testing many of the circuit application ideas presented here. An additional acknowledgment should go to Bob Darling of Rutgers University for the basic concept of Figure 22. A list of relevant application notes and article reprints that may be found helpful in pursuing the ideas opened up in this one follows:

A018 “Do’s and Don’ts of Applying A/D Converters”, by Peter Bradshaw and Skip Osgood.

A020 “A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing”, by Ed Sliger.

R017 “CMOS Chopper Op Amp Does Away with Glitches”, by Peter Bradshaw, Electronic Design, Aug. 2, 1980.

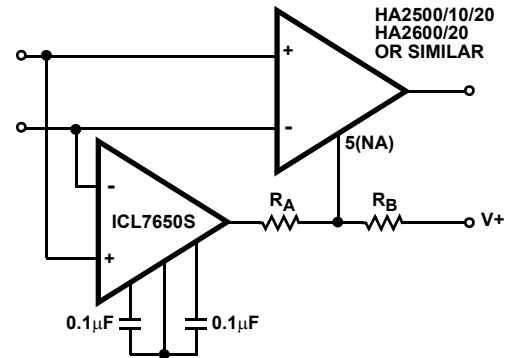


FIGURE 26A.

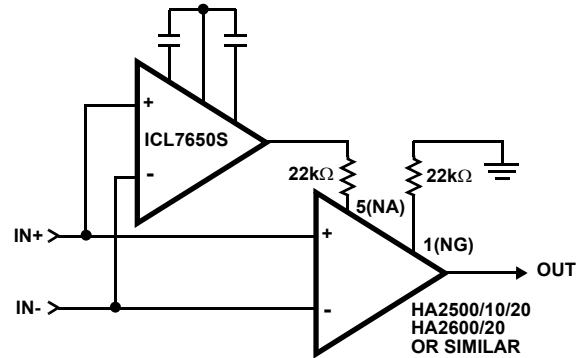


FIGURE 26B.

FIGURE 26. HA2500 OR HA2600 OFFSET NULLED BY ICL7650S

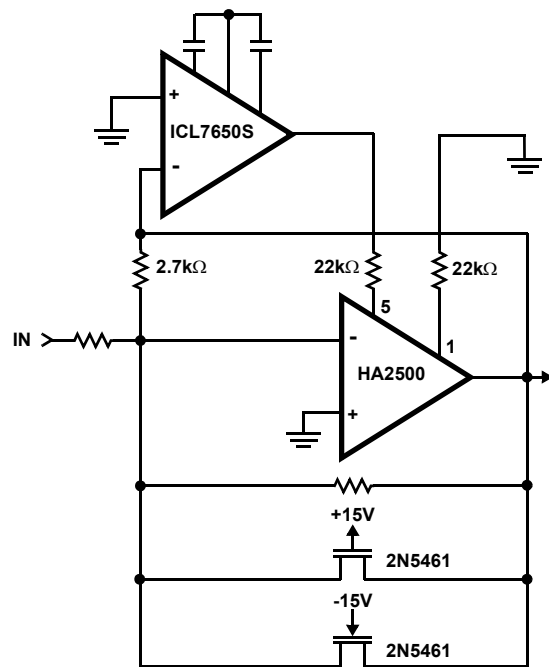


FIGURE 27. NULLED HA2500 WITH DYNAMIC CORRECTION AND OVERLOAD CLAMP

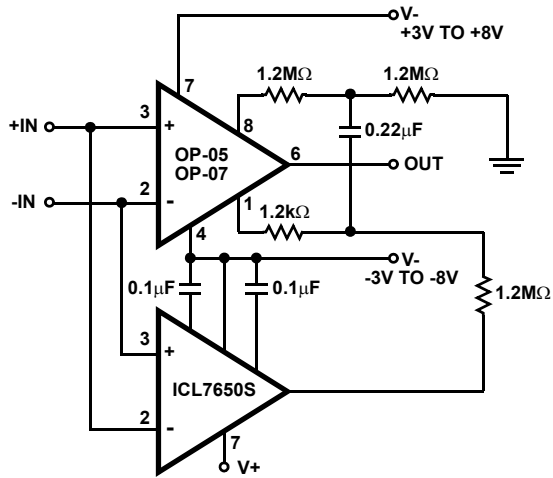


FIGURE 28. AUTO-NULLING CIRCUIT FOR OP-05/OP-07

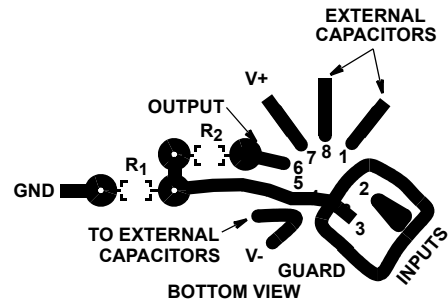


FIGURE 30A. NON-INVERTING AMPLIFIER WITH CLAMP

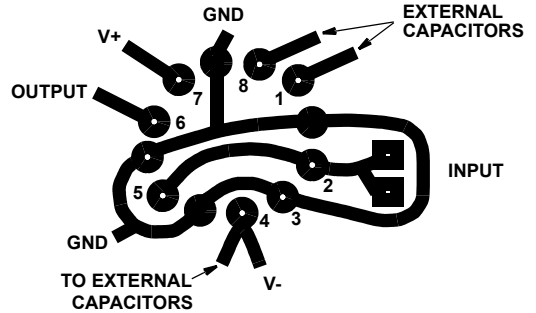


FIGURE 30B. INVERTING AMPLIFIER WITH CLAMP

FIGURE 30. INPUT GUARDING WITH CLAMP PIN

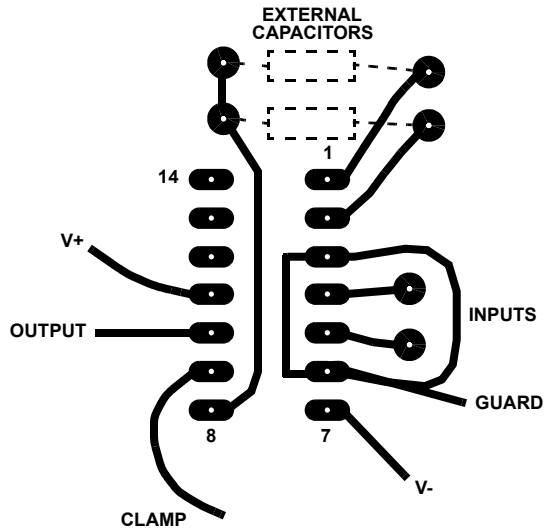


FIGURE 29A. 14-PIN PART

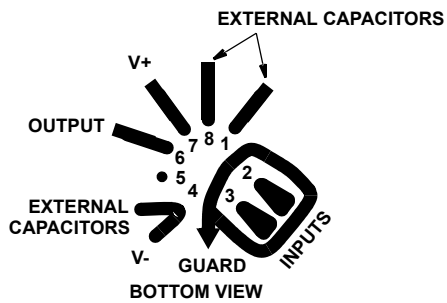


FIGURE 29B. TO-99 PACKAGE

FIGURE 29. BOARD LAYOUTS FOR INPUT GUARDING

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