Application Note AN111

Implementing Ultra-Deep Power Down Mode in AT25xx Series and AT45xx Series

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Revision History

Revison Number	Date	Tasks
A0	August 14, 2019	Implementing Ultra-Deep Power Down Mode in AT25xx and AT45xx Application Note initial release

Introduction

With any low-power design, the designer has the choice between choosing low-power components or switching off the power to peripheral devices. When considering the choice of non-volatile external flash memories, the designer has the same two options available to them - ultra-low power or switched power. This application note discusses the benefits and drawbacks for each option from a system operation, power consumption and reliability perspective. The document presents a third option of an ultra-deep power-down mode (UDPD) that simplifies a system design while improving reliability and reducing BOM costs. Instructions on how to implement UDPD mode are provided. UDPD is available on the following parts - AT45DBxxxE series Dataflash™, AT25DF / XE series Fusion, and AT25XE / FF series FusionHD™.

External flash memory design

Despite the proliferation of microcontroller (MCU) devices with embedded flash and a wealth of low-power modes in which they can operate, more and more systems still require an external flash memory device to supplement the on-chip flash for expansion reasons. Over-the-Air (OTA) updates, datalogging, user profiles, and other applications all contribute to this. A typical design using an external flash memory may look something like that shown in Fig. 1, where power is continuously supplied to the flash device.
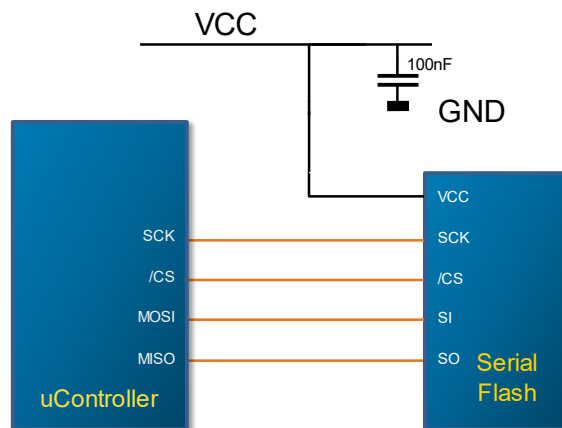

Fig. 1 A typical design using an external flash memory

For many applications this is an acceptable solution, as the standby current for the flash when the Serial Flash Chip Select Signal (/CS) is not asserted and the memory is in standby mode is typically about 10uA to 20uA. There is also an option to go into the command-driven deep power down mode, which reduces standby power even more to typically ~2uA to ~5uA. In some other systems, for example energy harvesting or small battery powered devices, even 2uA may still represent too high a current consumption value. Additionally, and in applications where the flash is accessed infrequently or very rarely used, 2uA standby for extended periods may represent an excessive drain on the power supply and energy reserves which reduces over all battery / system operating life.

External flash with simple power switching control circuit

To improve the system battery life, designers often implement a simple power switching control circuit so that the peripheral device or flash memory can be powered down when not in use. A typical circuit for this is shown in Fig. 2. This allows for the power to the flash device to be managed under software control through a spare MCU GPIO pin so that serial flash is only powered when required.
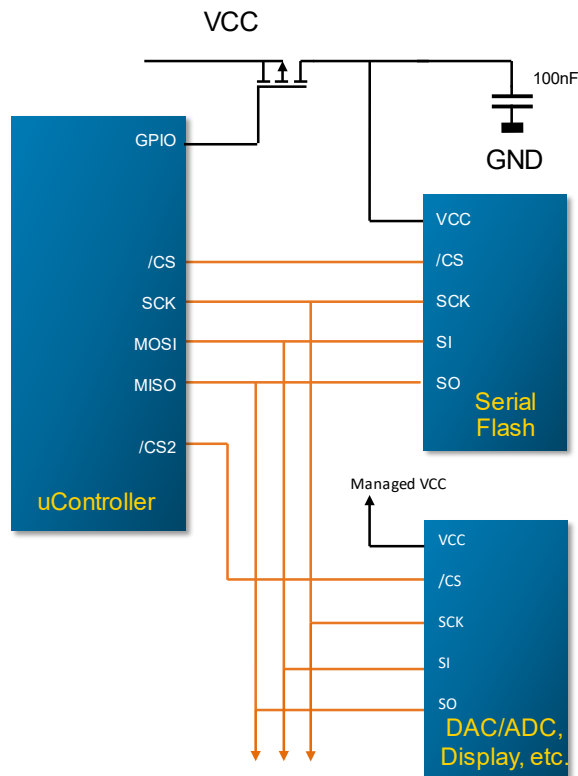
VCC

100nF

GPIO

GND

VCC

/CS   /CS

SCK   SCK

MOSI   SI

MISO   SO

/CS2   Serial
                        Flash

uController

Managed VCC

VCC

/CS

SCK

SI

SO   DAC/ADC,
           Display, etc.

Fig. 2 Serial Flash External Power Control Circuit

False Economy!

Consider a typical logic-level MOSFET device as shown in Fig. 2 to control the VCC to the memory, such as the DMHC3025LSD from Diodes Inc. It is noted in its documentation that this MOSFET has a zero gate voltage drain current of up to 500nA and gate-source leakage up to 1uA, leading to a total quiescent current of up to 1.5uA. This value is not much better than regular serial flash standard deep power down standby current that consumes typically 2uA. The inclusion of the MOSFET to completely switch off the serial memory VCC will reduce the standby power of the memory to zero, but the MOSFET itself has a potential leakage current and drain current of up to 1.5uA, which is only 500nA better than the memory in normal standby at up to 2uA.

Reliability concerns

The solution utilizing an external FET or LDO with control gate to control power to a peripheral device VCC pin is becoming more common; however this does also require an extra MCU GPIO pin, and will have some reliability concerns where multiple peripheral devices share a common SPI bus and where the individual devices have switched VCC pins.

When using such circuits, care must also be taken to manage the SPI bus connection before the power is turned off, to ensure that no I/O pins are maintained at the supply voltage when the chip VCC is at zero. In the application shown in Fig. 2, if the VCC to the flash is switched off and VCC = 0V on the flash, continuing to access the other SPI controlled devices will result in SPI bus signals also appearing on the Serial Flash SPI pins. In this scenario, the high VCC on peripheral SPI bus pins when VCC for that device is at zero, would result in the I/O protection diodes being forward biased, and the device potentially will draw power through the I/O pins themselves. This could lead to short-term or long-term reliability concerns and operational problems.

As a possible solution to this situation and using a circuit to switch VCC , the designer could consider a separate SPI bus for the serial memory where VCC can be turned off. They could then use a second SPI bus where all other SPI devices that remain powered at different times to the serial memory can reside.

The Ultra-Deep Power-Down (UDPD) Option

The Adesto® Fusion, FusionHD (AT25XExxx) and DataFlash (AT45DBxxxE/F) devices have standby and deep power down modes which result in a current consumption similar to or lower than other industry standard flash devices, but also offer an additional mode which takes the quiescent current down to less than 200nA for Fusion, 100nA for FusionHD and less than 400nA for Dataflash. This is achieved by integrating the power control circuitry into the memory device and allowing the master device (MCU) to control the power mode through the serial flash SPI command interface. This saves the GPIO pin for other purposes. See the diagram in Fig. 3.

Benefits to this solution are:
- It consumes much less power than standard deep power down.
- It does not require an external MOSFET.
- It allows the designer to use the same SPI bus for other peripherals and therefore simplify the design.
- It mitigates reliability concerns as the VCC pin is always connected to VCC, and power is controlled internally.
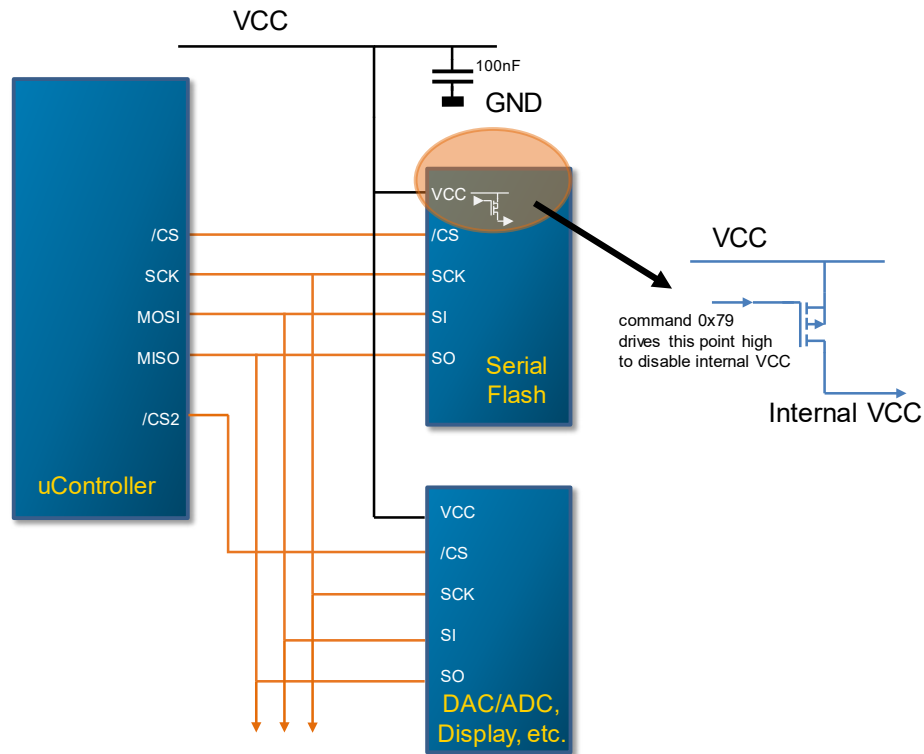
Fig. 3 Serial memory power control managed internally and driven through the SPI command interface

Additional benefits to this solution are:
- It saves a GPIO pin that would be used for switching the external MOSFET or LDO.
- It simplifies the software because it eliminates the surplus MOSFET/LDO control routines.
- It provides for a cleaner PCB design and reduced BoM.

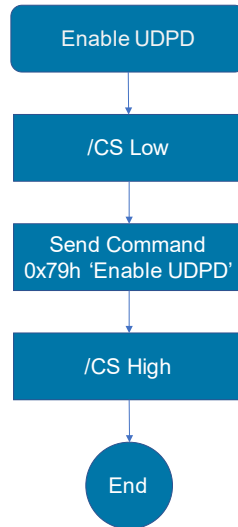## Using Ultra-Deep Power-Down

To use the UDPD Mode:

Fig. 4 Flow chart to enable UDPD

This will instruct the device to shut down additional internal circuitry to bring the supply current down to a minimum operating level. Ultra-deep power-down (UDPD) in FusionHD can also be entered with the B9 command when the Power Down Mode bit in Status Register 4, bit 7 is set. The B9 command will then emulate the 79 command providing enhanced flexibility and configuration options. When the device is in this UDPD state, all commands, including Status Register Read, will be ignored. (An exception is that the ABh command -Exit Deep Power Down / Exit Ultra-Deep Power-Down - will be accepted in Fusion HD). Since all commands are ignored, this UDPD mode can be used to further protect the flash device from inadvertent writes, program or erase operations.

Note: The UDPD command will be ignored if an internal self-timed operation such as program or ease is in progress.

To exit this UDPD mode in the Fusion and Dataflash devices, the /CS pin is asserted for a minimum of tXUDPD, which is about 70us. After this time, a new command can be clocked in, or /CS can be de-asserted leaving the flash in standby.

The much faster FusionHD devices require the Exit Deep Down command 'ABh' to be issued. For this device, JEDEC Reset and HW Reset (when enabled) can also be used to exit UDPD.

All devices will exit the UDPD mode if the power is cycled.

Conclusions

Choosing the proper low-power memory can be a critical system design factor for energy harvesting or small battery powered devices. Adesto's serial flash memory solutions offer the designer the option to simplify the design, reduce risk, improve reliability and save on external components, greatly simplifying the circuit and reducing bill of materials cost. This solution also allow designers to save an MCU GPIO pin and simplify software in that no consideration must be given to the state of the SPI bus when the flash device is put into ultra-deep power-down (UDPD) mode. This feature, along with such other features like Active Status Interrupt and a wide operating voltage, will make it easier for a system designer to achieve a design with the maximum possible life from the smallest batteries.