Capacitive Sensor Microcontrollers

CTSU Capacitive Touch Electrode Design Guide

Introduction

This application note describes how to design electrode patterns, with sample patterns for reference, for MCUs embedding the Capacitive Touch Sensing Unit (CTSU)

Target Device

RX Family, RA Family, and RL78 Family MCUs and Renesas Synergy™ embedding the CTSU

(CTSU indicates CTSU2, CTSU2L, CTSU2SL, etc.)

Contents

1. Outline

Capacitive touch button sensitivity and anti-noise performance are both influenced by the shape and size of the touch electrode pad (herein referred to as “electrode”), wire routing, patterns surrounding the electrode, overlay panel thickness, inclusion of air gap, internal configuration of product housing, and other factors. All of these factors need to be taken into consideration when designing the electrode as well as the surrounding area.

This application note describes how to design electrode pads and wiring as well as how to deal with related issues and potential problems when using the Renesas Touch Capacitance Senor Unit (CTSU). It also provides recommended applications.

2. Self-capacitance Method Buttons: Electrode Layout Patterns

2.1 Outline of Design Recommendations

The following provides reference information for designing self-capacitance method buttons on a two-sided printed board. We recommend using a 2- or more layer board and placing a shield guard of a cross-hatched GND pattern around the electrodes to suppress parasitic capacitance fluctuations due to the surrounding environment and noise factors. We also recommend using an ESD countermeasure by shielding the outer circumference of the board with a GND plane pattern. The numbers listed here correspond to the numbers in each figure, excluding numbers 8 and 9. Each item is described in detail later.

① Electrode shape: square or circle
② Electrode size: 10mm to 15mm
③ Electrode proximity: Electrodes should be placed with ample distance so that they do not react simultaneously to the target human interface, (referred to as “finger” in this document); suggested interval: button size x 0.8 or more
④ Wire width: approx. 0.15mm to 0.20mm for printed board
⑤ Wiring length: Make the wiring as short as possible. On corners, form a 45-degree angle, not a right angle.
⑥ Wiring spacing:
  (A) Make spacing as wide as possible to prevent false detection by neighboring electrodes.
  (B) 1.27mm pitch
⑦ Cross-hatched GND pattern width: 5mm
⑧ Cross-hatched GND pattern and button/wiring spacing
  (A) area around electrodes: 5mm (B) area around wiring: 3mm or more
  Cover the electrode area as well as the wiring and opposite surface with a cross-hatched pattern. Also place a cross-hatched pattern in the empty spaces, and connect the 2 surfaces of cross-hatched patterns through vias.
  Refer to section “2.5 Anti-Noise Layout Pattern Designs” for cross-hatched pattern dimensions, active shield (CTSU2 only), and other anti-noise countermeasures.
⑨ Electrode + wiring capacitance: 50pF or less
⑩ Electrode + wiring resistance: 2kΩ or less (including damping resistor with reference value of 560Ω)

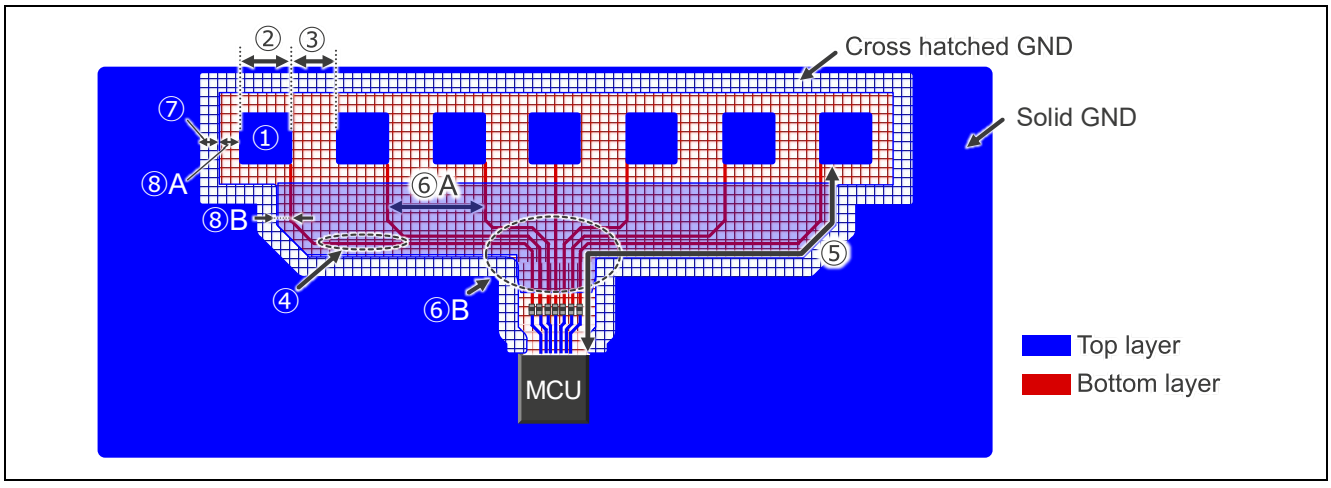


Figure2-1. Example of Anti-noise Layout Pattern for Self-capacitance Method Buttons

2.2 Self-capacitance Method Overview

Figure2-2 shows the self-capacitance generated in the electrode. A single electrode connected to the capacitive sensor in the self-capacitance method button measures capacitance C. The value of C is a composite of parasitic capacitance Cp formed by the electrode and surrounding conductors and parasitic capacitance Cf formed by the electrode and the finger. The size of the capacitance can be considered in the capacitor equation $C = \varepsilon \frac{S}{d}$ (see note). Cp is constant as the surrounding devices are static, but Cf increases as the finger gets closer. By setting a threshold for the amount of increase in Cf, you can determine whether the touch button is ON or OFF. Note that if the finger actually touches the electrode, it will short and no longer be able to measure capacitance. Normally, there is an overlay panel of a few mm between the electrode and the finger.

Note) C: capacitance, ε : Relative permittivity, S: electrode facing area, d: inter-electrode distance

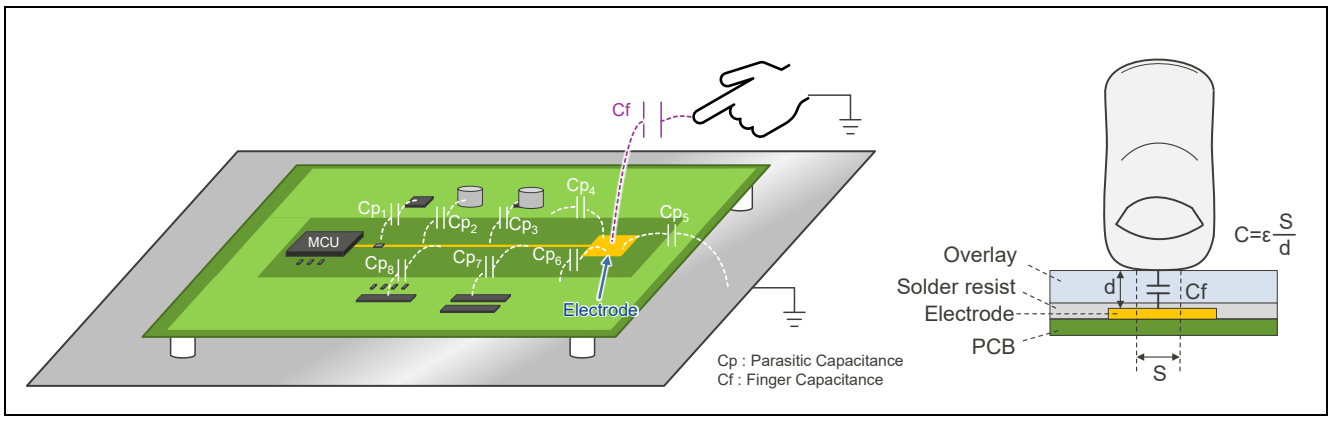


Figure2-2. Image of Self-capacitance Generated in the Electrode

2.3 Principle of CTSU Self-capacitance Method Detection

Figure2-3 shows an overview of the CTSU internal configuration for the self-capacitance method. The CTSU outputs a digital count value proportional to capacitance C of the connected electrode, and determines whether the touch button is ON or OFF by software. When the electrode is connected to the CTSU, it performs as a switched capacitor controlled by the sensor drive pulse and estimates capacitance from the charge/discharge current to C. The CTSU measurement block has a current-frequency conversion function which inputs a current equivalent to the charge/discharge current and outputs a frequency proportional to the amount of current. For details on the detection principle, refer to the application note “RX113 Group CTSU Basis of Cap Touch Detection.”

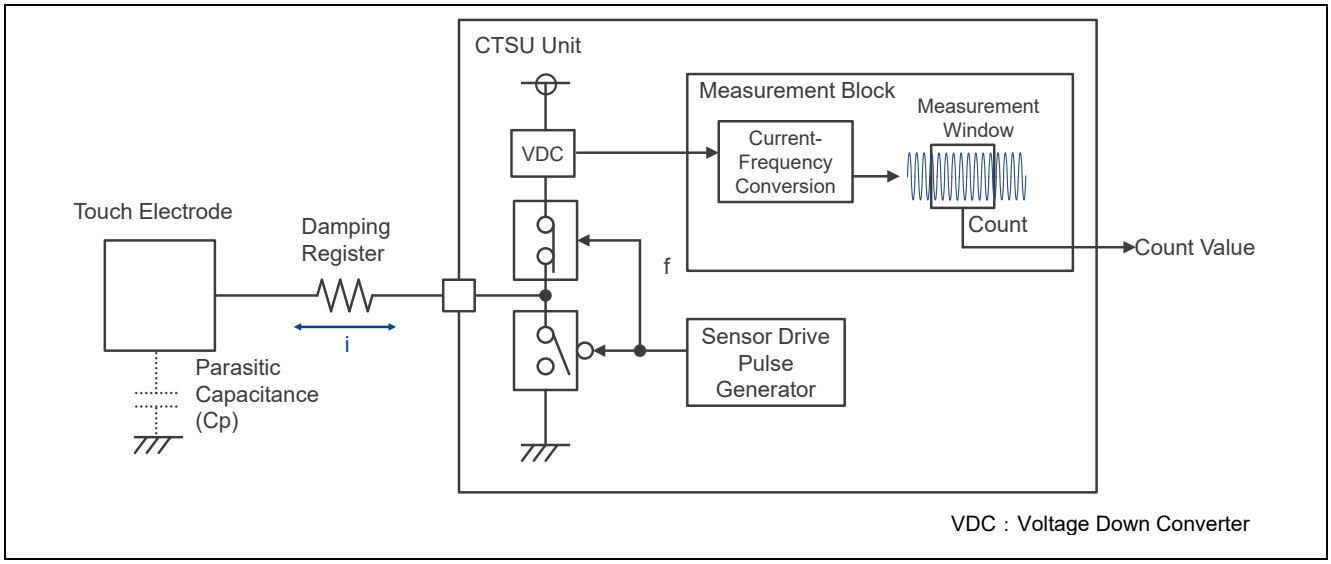


Figure2-3. Internal Configuration Overview of Self-capacitance CTSU

Figure2-4 shows an image of CTSU measurement. When one cycle of the sensor drive pulse frequency is shorter than the C charge/discharge time and the charge/discharge is insufficient, not enough current flows to C and the count value is smaller than the ideal value. When parasitic capacitance is large, it may be possible to take a measurement by lowering the sensor drive pulse frequency. When the sensor drive pulse frequency is lowered, the CTSU can measure a maximum of 50pF. Note that when the sensor drive pulse frequency is decreased, the number of measurements per unit time by the current-frequency conversion function also declines. The sensitivity of the electrode is likely to decrease as well. The unit time can be increased by adjusting the register setting value in the CTSU, but the amount of time required to complete the measurement will also increase. When designing a capacitive electrode circuit, conditions for button sensitivity, measurement time and noise immunity must be met.

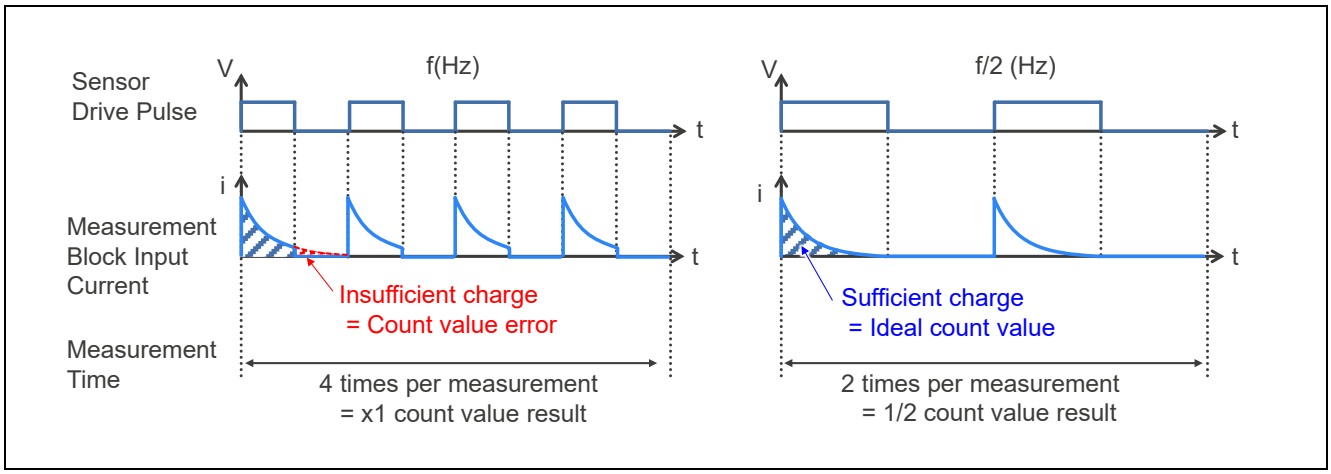


Figure2-4. Image of CTSU Measurement

Figure2-5 shows an image of GND patterns and parasitic capacitance. When using a printed board, place a GND plane pattern directly under the wiring pattern as a general anti-noise countermeasure. In the self-capacitance button, the parasitic capacitance Cp_{GND} generated by the electrode and GND plane pattern is much larger than Cf and exceeds the measurement range of the CTSU. So, when designing the self-capacitance button, do not place a GND plane pattern directly under the electrode. If an anti-noise countermeasure is needed, use a cross-hatched GND pattern to reduce the increase in parasitic capacitance.

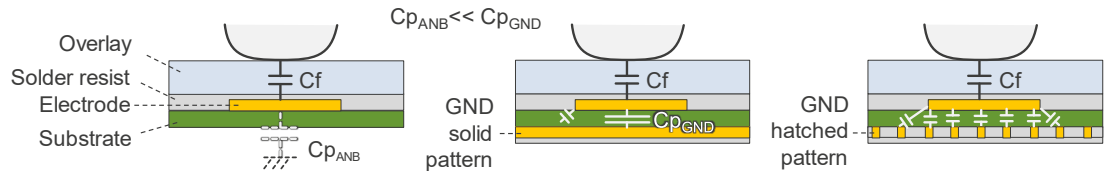


Figure2-5. Image of GND Pattern and Parasitic Capacitance

2.4 Electrode Pattern Design

When designing a self-capacitive touch button circuit, design the pattern and select the material so that the following conditions are met.

- Electrostatic capacity C: 50pF or less
- Resistance value R: 2kΩ or less (including damping resistor)

Figure Figure2-6 shows a self-capacitance electrode circuit. The touch button circuit configuration comprises the touch electrode, electrode wiring, and damping resistor. The reference value of the CTSU damping resistor is 560Ω. Note that touch button circuit C is also affected by parasitic capacitance with objects around the board such as the GND pattern, overlay panel, and body chassis. Normal measurement values may not be obtained when using values other than the above design values. The total capacity value for each electrode can be confirmed using QE for Capacitive Touch.

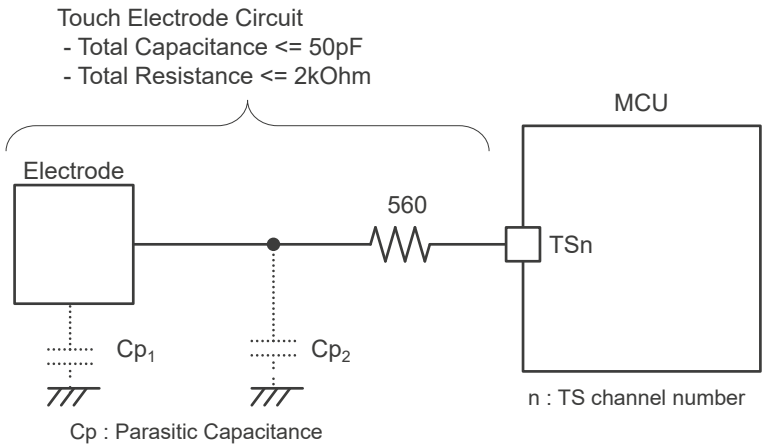


Figure2-6. Self-capacitance Method Electrode Circuit

2.4.1 Electrode pads and wiring

The following offers recommended shapes for button electrodes and wiring conditions.

- Shape: square or circular plane patterns
- Size: 10 x 10 to 15 x 15mm
- Electrode interval: To avoid crosstalk, use an interval wide enough to prevent simultaneous response by adjacent electrodes based on finger or other touch interface
  Target interval size: electrode button size x 0.8 or more
- Interval between electrode and GND pattern: 5mm or more
- Do not place wiring or a pattern for another function, or a GND plane pattern directly under an electrode. When a GND pattern is necessary as an anti-noise countermeasure, place a cross-hatched GND pattern.

Crosstalk refers to capacitive coupling between adjacent electrodes or capacitive coupling between a finger and adjacent electrodes when the target electrode is touched. For more details, see section “2.6 Effect of Panel Thickness.”

Fig. 2-7 shows the recommended electrode shapes and size. Size and shape are fairly flexible and can be determined based on the button design of the panel on the final product. Make sure that the size is not extremely large or extremely small with respect to the part of the human body (finger, etc.) that will be operating the product. If the pad is square, round the corners of the electrode with a radius of 0.5 to 1.0 mm to reduce the effects of noise.

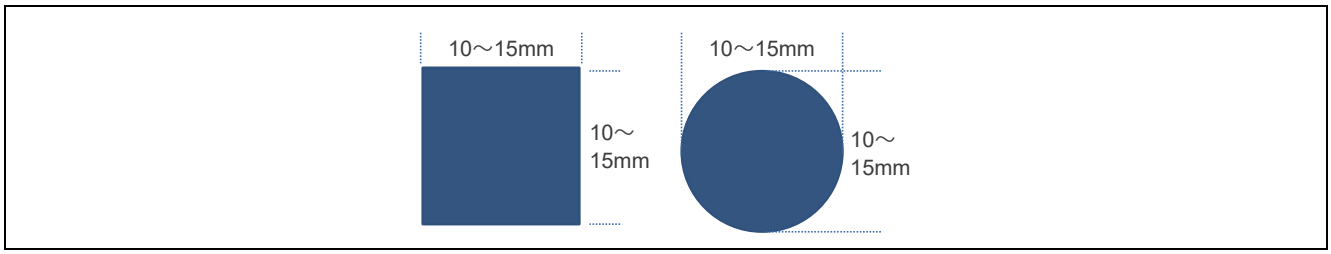


Figure2-7. Recommended Electrode Shapes and Size

Figure2-8 shows shapes that are not recommended for electrodes—triangles with angles of 90 degrees or less and E-shapes with narrow line width and long total length. These shapes are not recommended as they tend to perform as antennas and degrade the RF noise immunity.

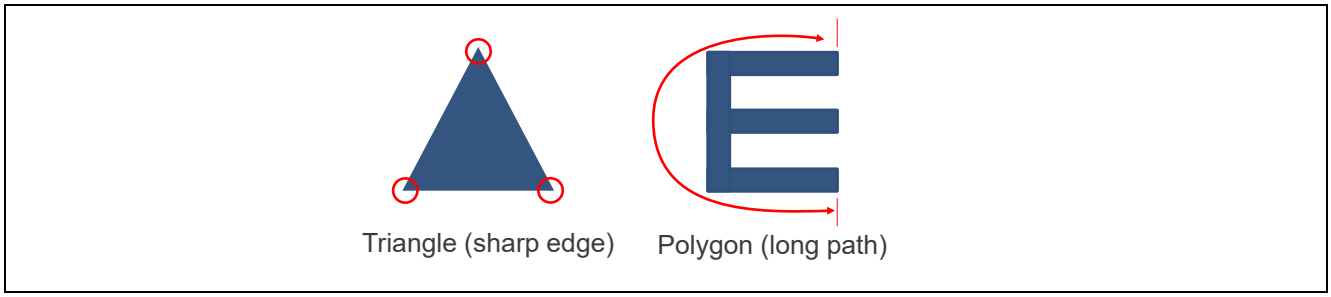


Figure2-8. Unsuitable Electrode Shapes

2.4.2 Wiring

The wiring part of the electrode has a small parasitic capacitance and is easily affected by external noise. Noise immunity can be improved by suitably arranging the wiring spacing and GND pattern. In addition, the CTSU also functions as a shield because, other than during measurements, the TS pins and wiring are fixed at the GND level. Since the coupling capacitance changes depending on the wiring width and length, adjust the wiring spacing and the spacing between wiring and the GND pattern so that the conditions for total parasitic capacitance are satisfied.

Recommended layout and dimensions of wiring are listed below.

- Wiring width: 0.15mm（the thinnest wire capable through mass production）
- Wiring spacing: 1.27mm pitch
  However, leave at least 5mm, more if possible, between the electrode pad circumference (about twice the length of the electrode pad)
- Wiring and cross-hatched GND pattern spacing: 1.27mm (1.27mm pitch)
- Wiring and GND pattern spacing: 3mm or more

Make sure the design satisfies the following wiring requirements as well.

- Keep the wiring as short as possible.
- Try to have as few corners in the wiring as possible; make corners 45 degrees or rounded.
- Drill vias at the edge of the electrode pad and layout wiring on the back side. This helps reduce malfunctions when wires are touched. However, keep the number of vias at a minimum as they tend to increase parasitic capacitance.
- As an anti-noise countermeasure, place a cross-hatched GND pattern directly under the electrode and wiring.
- The wire routing extending from the electrode is vulnerable to noise as there is no cross-hatched GND pattern directly under the wiring. Bring the cross-hatched GND as close as 0.5mm to this part.
- Do not place wiring other than that used for the touch function directly under the electrode wiring. If you must do so, make the wiring orthogonal and minimize the facing area.

Figure2-9 shows an example of the wiring section of a double-layer board layout example.

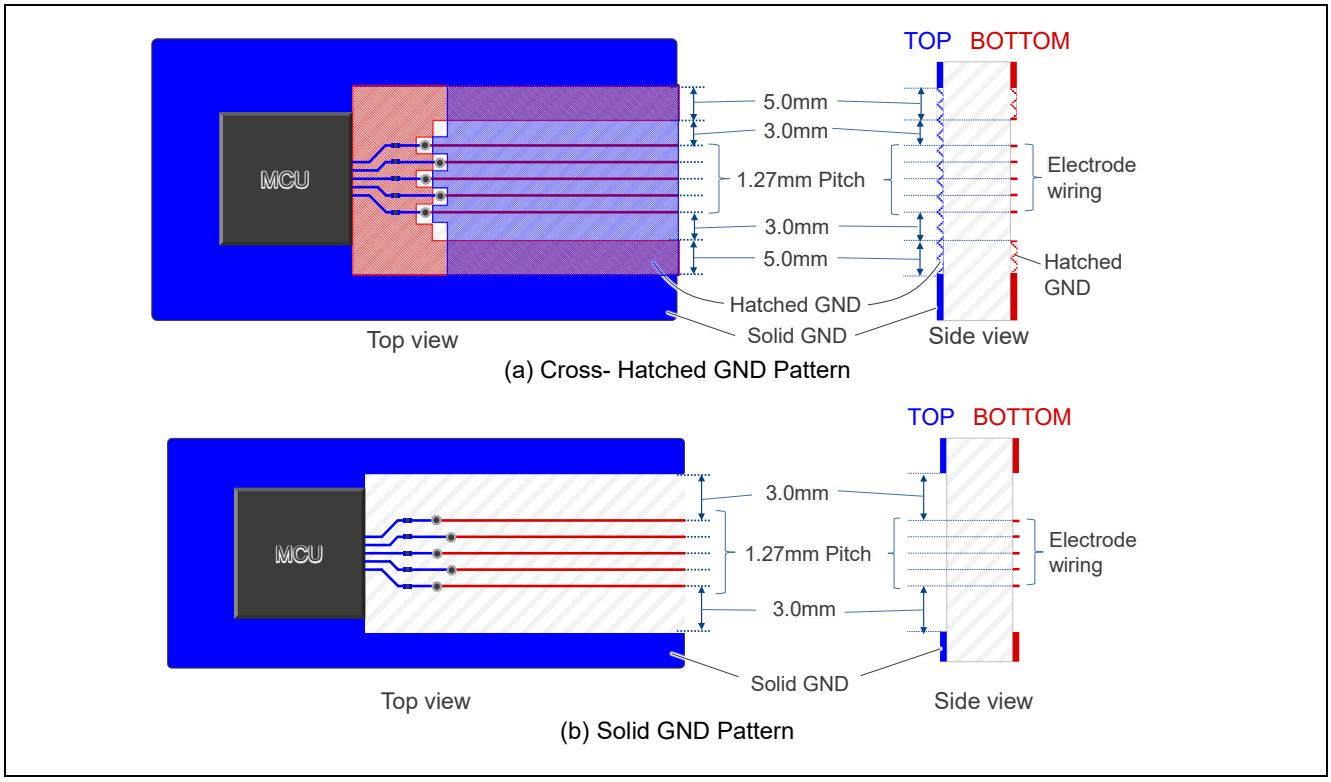


Figure2-9. Double-Layer Board Layout Example (wiring section)

Figure2-10 shows an example of the electrode section of a double-layer board layout.

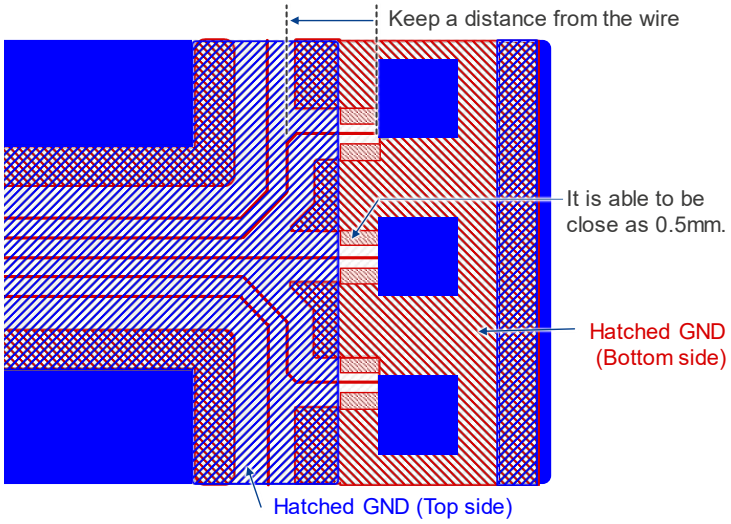


Figure2-10. Double-Layer Board Layout Example (electrode section)

Figure2-11 and Figure2-12 show layout examples for each layer.

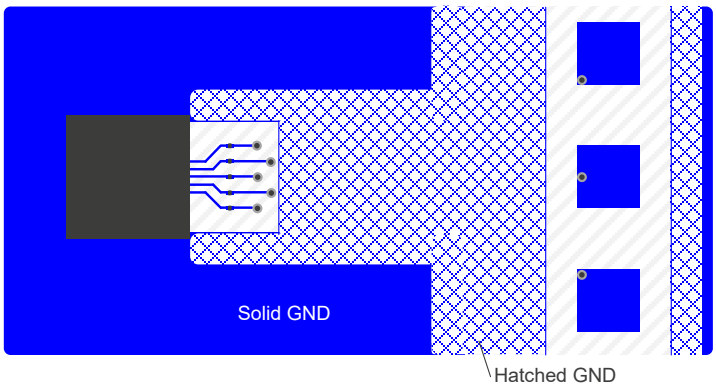


Figure2-11. Top Layer Layout Example

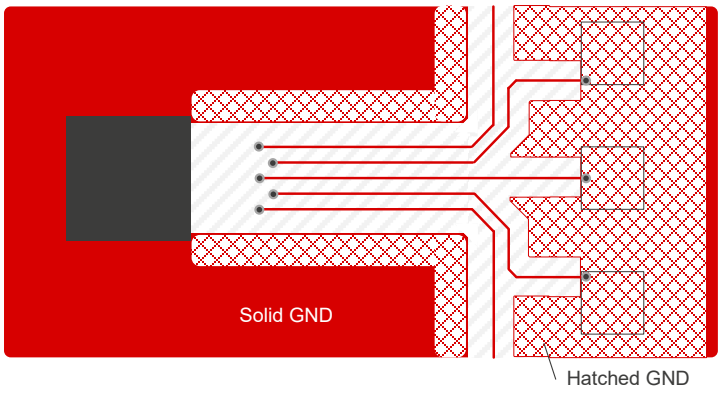


Figure2-12. Bottom Layer Layout Example

Figure2-13 shows an example of high-density wiring. When you have limited board size and need to increase the wiring density, shift the wiring by a half pitch and lay out the wiring on both sides of the board. For 4-layer boards, make sure to place a cross-hatched GND on the inner layers.

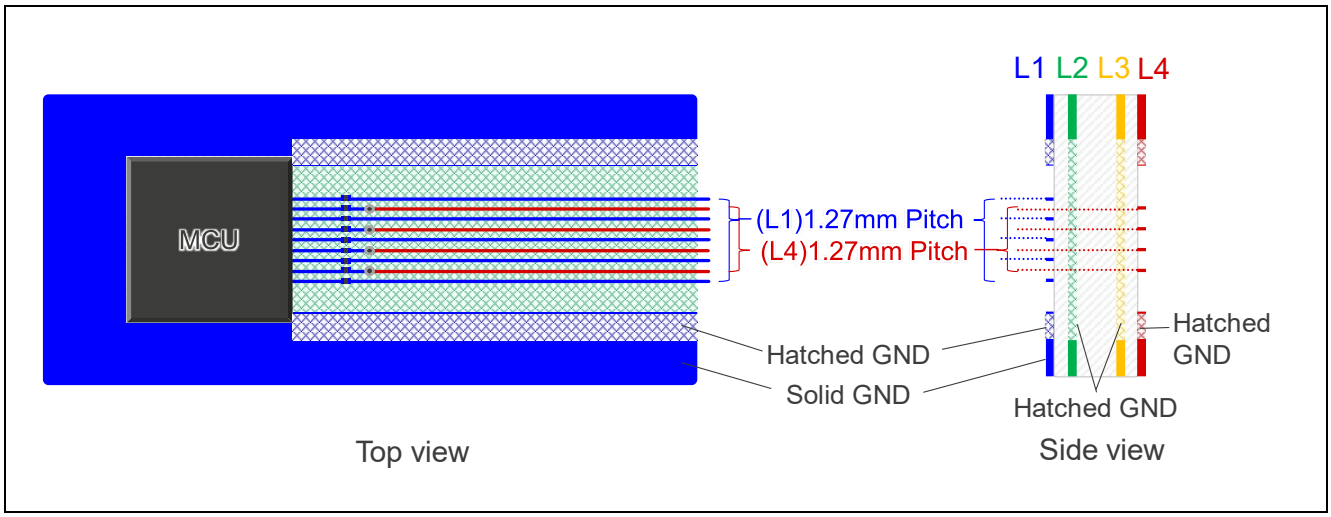


Figure2-13. High-density Wiring

2.5 Anti-Noise Layout Pattern Designs

The electrode circuit configuration allows the circuit to act as an antenna (the MCU pin is open only for capacitive coupling) and makes it vulnerable to electromagnetic field noise. Renesas Touch MCUs employ several anti-noise countermeasures to ensure high noise immunity. However, an MCU alone cannot prevent influence from all noise. Hardware countermeasures are indispensable when using the MCU in a severe noise environment. The following are a few examples of how to protect the system from external noise.

In general, the longer the wiring, the more chances for noise to synchronize and mix with the many noise frequencies. Make sure the wiring between button electrodes and the touch MCU is kept as short as possible.

The best way to prevent malfunctions due to external noise is to shield guard the touch button circumference. CTSU2 supports active shields.

2.5.1 Shield guard countermeasures

2.5.1.1 Pattern design

Figure2-14 shows the cross-hatched pattern dimensions. Shielding the electrode and electrode wiring serves as an effective EMS noise countermeasure. A shield guard can be placed directly under the electrode or electrode wiring on a multi-layer board but the GND plane pattern has a large coupling capacity which will prevent the electrode from detecting capacitance fluctuation when touched. Therefore, a cross-hatched pattern shield guard should be used. The Renesas Capacitive Touch Evaluation System employs a cross-hatched pattern in the dimensions listed below. In addition, the cross-hatched pattern is tilted 45 degrees depending on the wiring direction in order to reduce the capacitive coupling with the electrode wiring.

- Pitch: 1.5mm
- Line width: 0.15mm
- Line space: 1.35mm

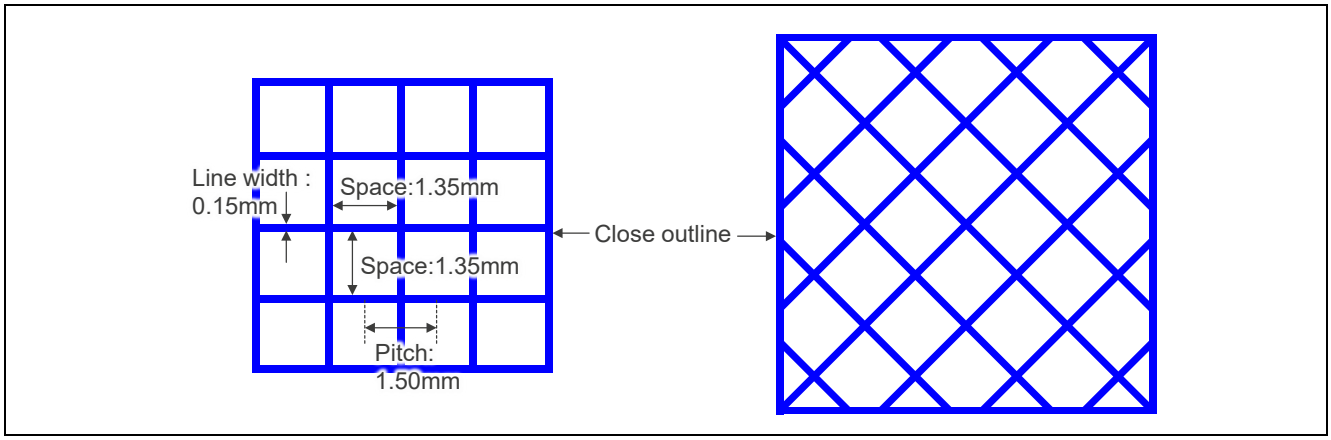


Figure2-14. Cross-hatched Pattern Dimensions

2.5.1.2 GND shield

Placing a GND pattern around the electrodes and electrode wiring generates capacitive coupling which suppresses potential fluctuation due to influence from external noise. Note that if the GND shield is placed too close to the electrode it will cause parasitic capacitance to increase too much, which may block touch detection. When close shielding is necessary due to a severe noise environment, we recommend using a hatched shape that will reduce capacitive coupling. In addition, the longer the wiring must run in parallel, the more the parasitic capacitance increases. Therefore, you may need to adjust the distance between the wiring and the shield.

The following are recommended shape and wiring conditions for the top layer. These recommendations assume the electrode pads are placed on the top layer.

- Distance between electrode and cross-hatched GND shield: 5mm
- Width of cross-hatched GND shield: 5mm or less
- Make sure to connect the cross-hatched GND pattern and GND plane.
- Cover the area directly under the electrode and wiring with the cross-hatched GND pattern.

Figure2-15 and Figure2-16 show an example of a GND shield pattern for a multi-layer board.

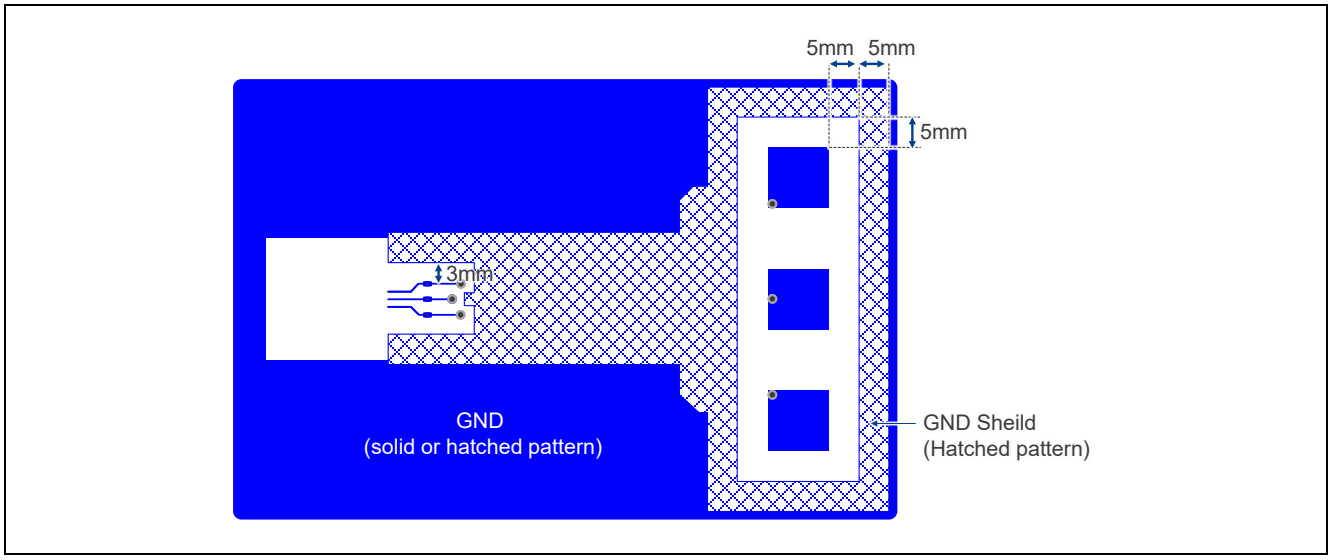


Figure2-15. GND Shield Pattern Example for Multi-layer Board (top layer)

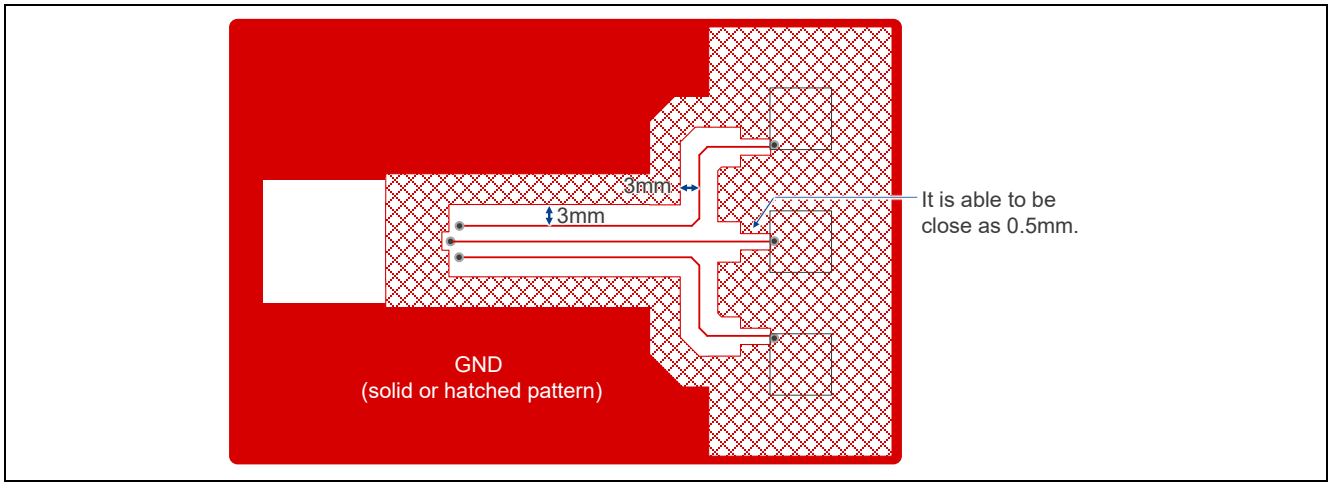


Figure2-16. GND Shield Pattern Example for Multi-layer Board (bottom layer)

2.5.1.3 Active shield (CTSU2 function)

This function is provided for MCUs embedded with CTSU2.

The active shield function drives the shield guard with signals of the same potential and phase as the electrodes. Using the active shield will reduce capacitance coupling between the electrode and shield guard as well reduce noise interference. The active shield is driven by a switched capacitor in the same manner as a normal electrode. Note that the active shield can't be driven when parasitic capacitance is large, which causes a phase shift with the electrode, making it impossible to gain sufficient results.

Figure2-17 shows an example of a shield electrode circuit. An active shield can be thought of as the button electrode that connects to the TS pin. The shield electrode circuit can be designed in the same manner as a normal electrode, but extra attention must be paid to size and pattern design. Since this shield is placed to cover the electrodes, the more electrodes there are, the higher the parasitic capacitance of the shield electrodes, which results in insufficient charging and discharging of the switched capacitor. Reducing the damping resistance value may help improve this problem. If the capacitance of the electrode and active shield differ significantly, also consider subdividing the button and active shield grouping. QE for Capacitive Touch supports up to 8 groupings (configurations). For details concerning the configurations, refer to QE for Capacitive Touch Help File.

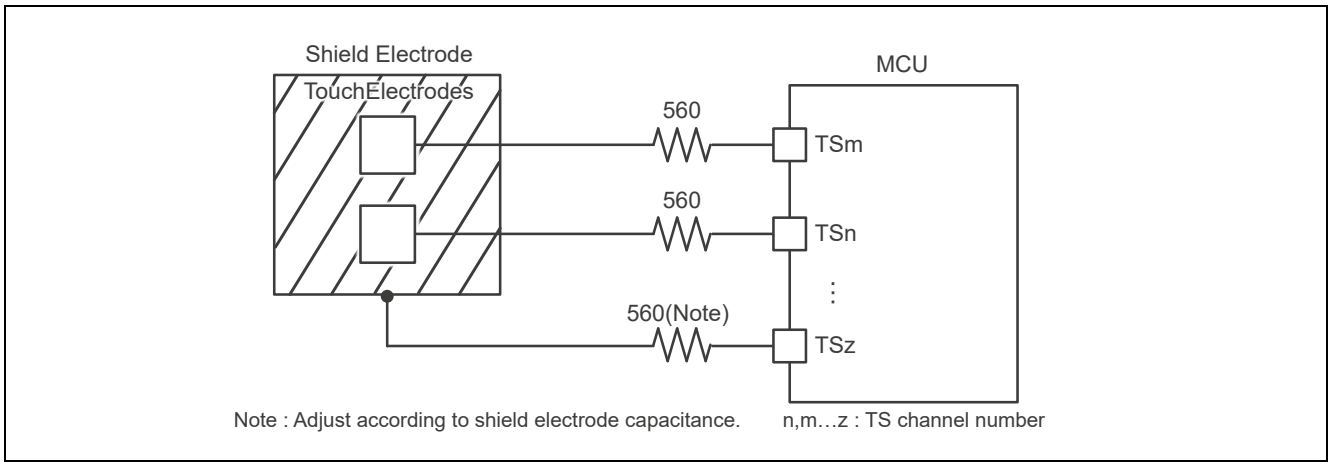


Figure2-17. Shield Electrode Circuit

The following are recommended shape and wiring conditions for the active shield. The recommendations assume the electrode pads are placed on the top layer.

- Distance between touch electrode and active shield electrode: 3mm
- Width of active shield electrode: 3mm
- Distance between active shield electrode and GND plane pattern: 3mm or more
- Cover all of the areas directly under the electrodes and wiring with an active shield electrode.

Figure2-18 and Figure2-19 show an example of the active shield pattern for multiple-layer boards.

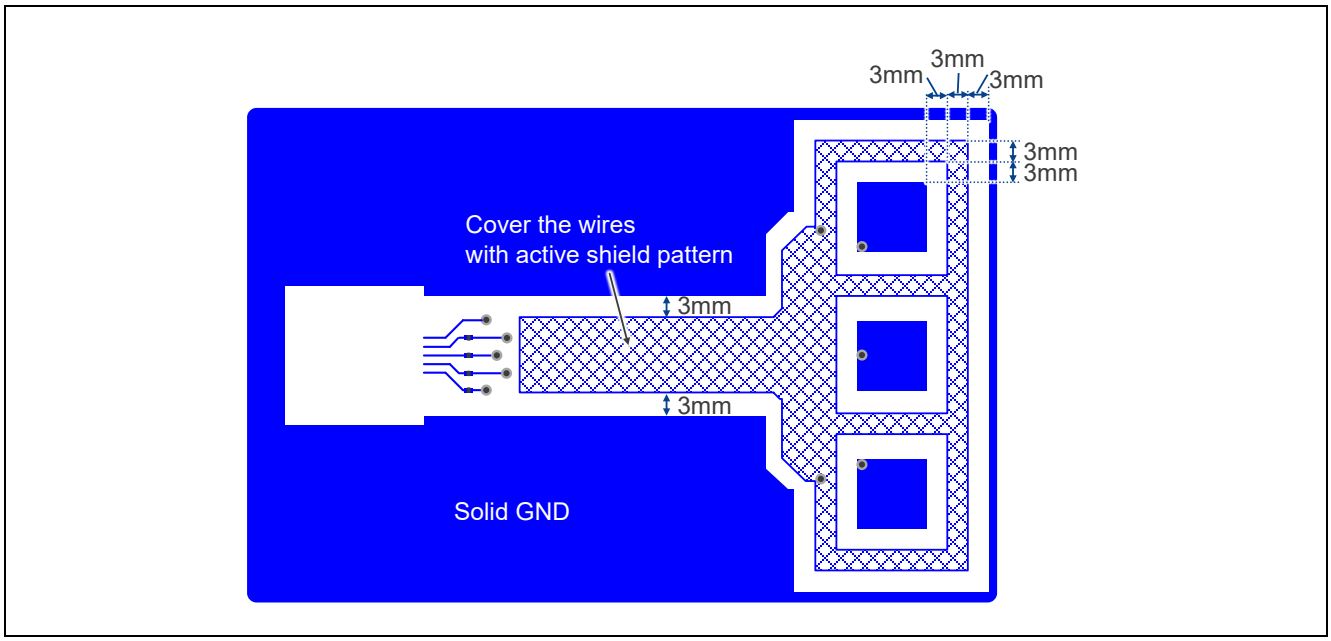


Figure2-18. Example of Active Shield Pattern for Multiple-Layer Board (top layer)

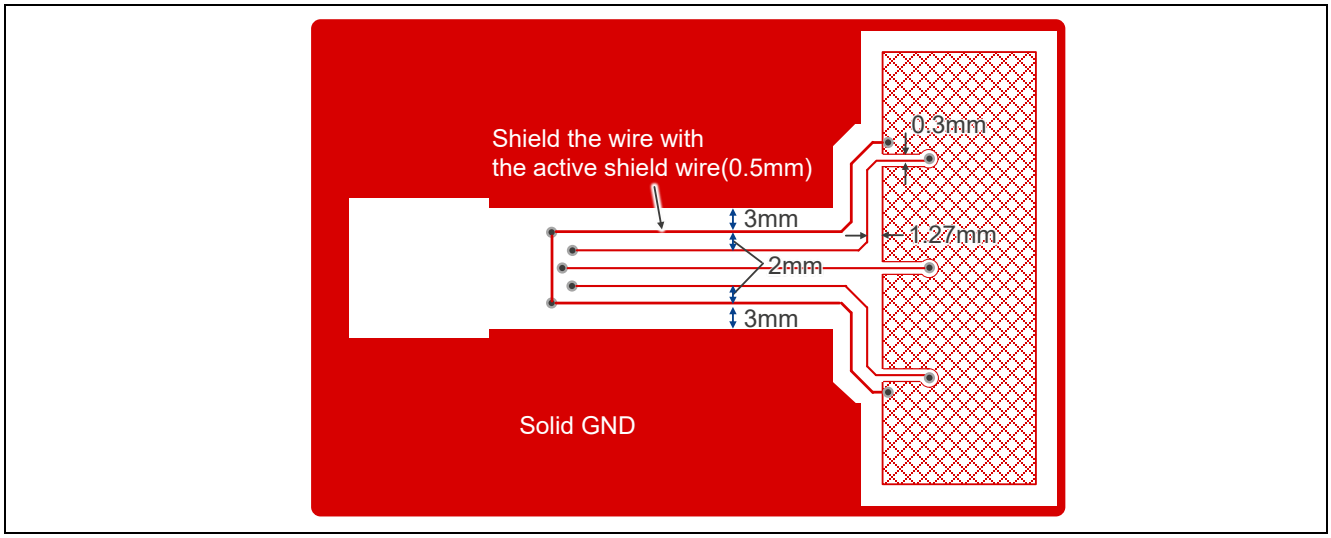


Figure2-19. Example of Active Shield Pattern for Multiple-Layer Board (bottom layer)

2.6 Effect of Panel Thickness

The self-capacitance method detects the capacitance generated when there is contact between the human body and a button electrode. Accordingly, in this kind of touch detection, the larger the touch surface of the button electrode and the longer the distance between the finger or other body part and the electrode, the higher the sensitivity. As the maximum touch surface size of the button electrode is limited (10mm to 15mm), the distance, or panel thickness, is the key factor in adjusting sensitivity.

2.6.1 Relationship of panel thickness and touch sensitivity

Figure2-20 shows the relationship of the amount of capacitance change and sensitivity distance in the self-capacitance method. In this method, the capacitance increases or decreases depending on the distance between the finger and the electrode, allowing touch detection over a broad range (distance). However, this also means that if the threshold has a large margin in comparison to the capacitance, touch detection may occur before the finger actually has contact with the panel. Capacitance may increase and decrease when touched depending on the relative permittivity of the panel material. Keep in mind that materials with a high relative permittivity may exceed the CTSU measurement range even at the same touch distance.

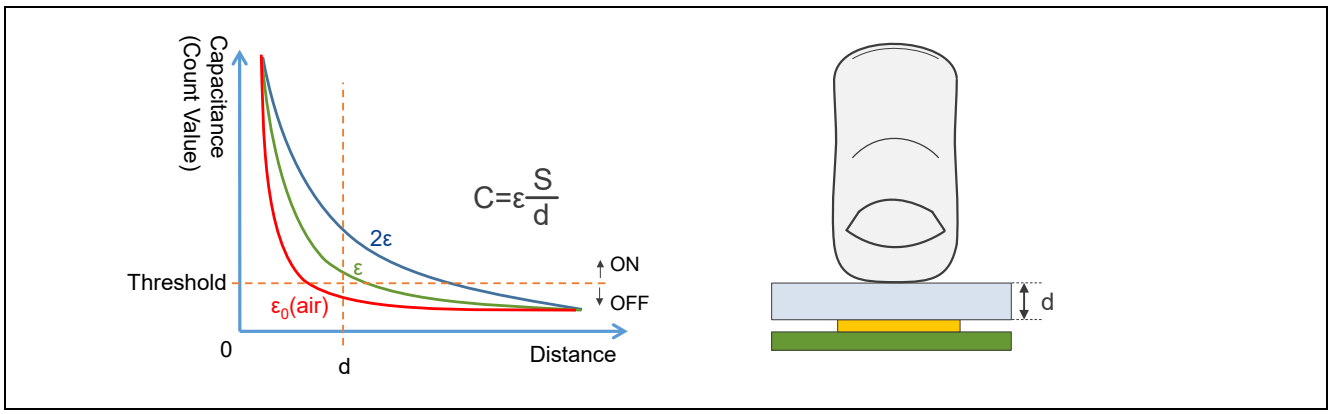


Figure2-20. Relationship of Capacitance Change and Sensitivity Distance

Table 2-1. Relative Permittivity of Each Material

Dielectric Material	ε
Acrylic	2.4-4.5
Glass	4.5-7.5
Nylon Plastic	3.0-5.0
Flexible Vinyl Film	3.2
Air	1.0
Water	80

2.6.2 Relationship of panel thickness and crosstalk

Figure2-21 shows the relationship of the inter-electrode distance and panel thickness in the self-capacitance method. If the button electrodes are placed too close together, they may cause neighboring button electrodes to turn ON erroneously (left side of figure). To prevent false detections (crosstalk), among neighboring button electrodes, the recommended distance between button electrodes is 0.8 times wider than the button size.

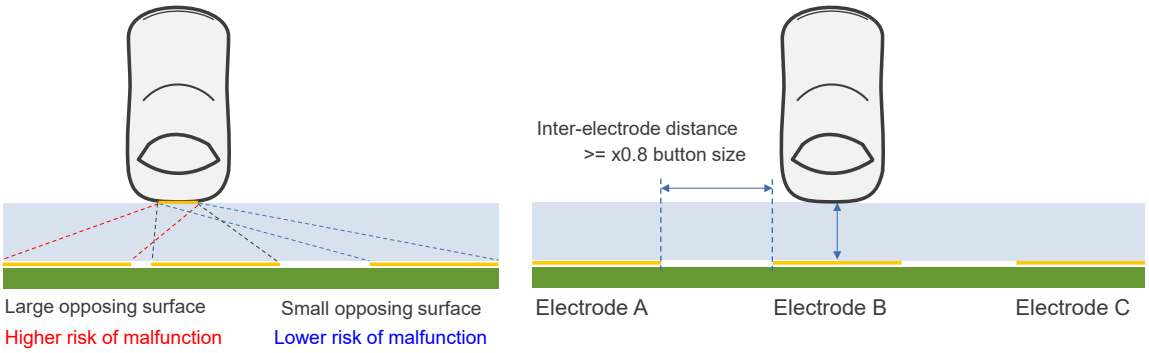


Figure2-21. Relationship of Inter-electrode Distance and Overlay Thickness for Self-capacitance Method

2.7 Electrode Application Examples

2.7.1 Example of slider electrode layout pattern design

Figure2-22 shows the recommended pattern for a slider electrode in the self-capacitance method. This pattern is designed for finger touch and ensures that 3 electrodes respond when the slider is touched anywhere other than the two ends. To change the size of the slider, adjustments must be made by adding or removing electrodes rather than expanding or shrinking the pattern.

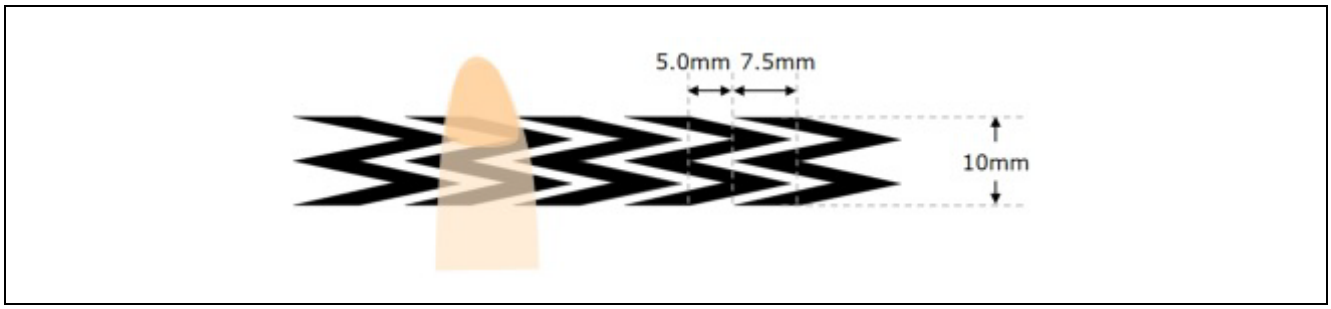


Figure2-22. Recommended Pattern for Slider Electrode for Self-Capacitance Method

2.7.2 Example of wheel layout pattern design

Figure2-23 shows the recommended wheel electrode pattern for the self-capacitance method. This pattern is designed for finger touch and ensures that 3 electrodes respond no matter where the wheel is touched. To change the size of the wheel, adjustments must be made by adding or removing electrodes rather than expanding or shrinking the pattern.

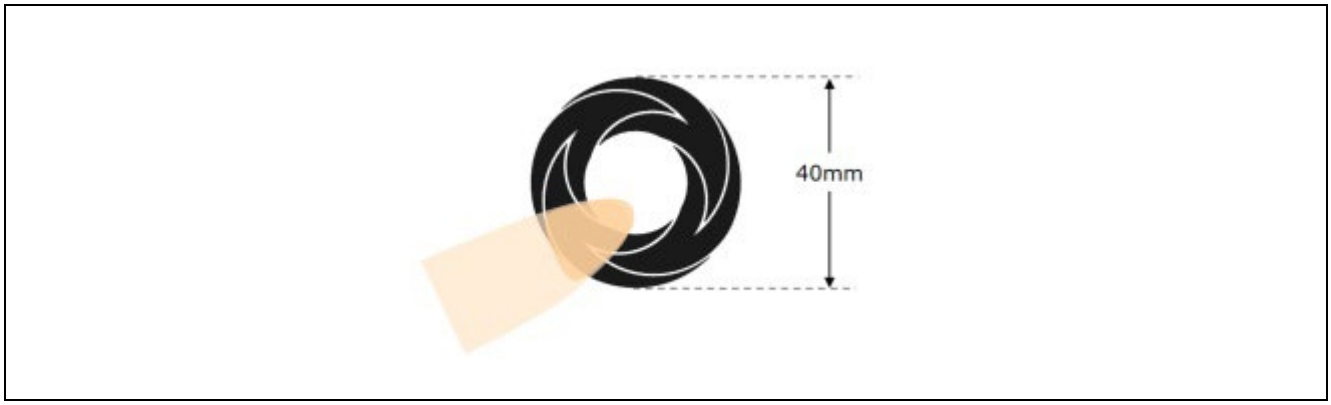


Figure2-23. Recommended Pattern for Wheel Electrode for Self-Capacitance Method

2.7.3 Flexible printed circuit boards

Although any conductive material can be used for the electrode, note that materials with high surface resistance such as carbon may reduce touch sensitivity. Also, materials with high surface resistance may not be consistently sensitive depending on where the finger is placed. If such a material must be used, lay out the wiring as shown in Figure2-24: (b) arrange wiring as close to the center of the electrode or (c) surround the entire electrode with a material that has low surface resistance so the resistance value is constant regardless of where the surface is touched. When using copper or other sufficiently low surface resistant material, the wiring can even be routed from any point on the button electrode itself, as shown in example (a).

On flexible printed circuit (FPC) boards, compared to printed boards, wires tend to be thicker and the space between wiring wider. Although thinner wire width helps suppress parasitic capacitance, the resistance value increases. We recommend designing based on a wire width of approximately 1.0mm with approximately 1.0mm spacing between wires.

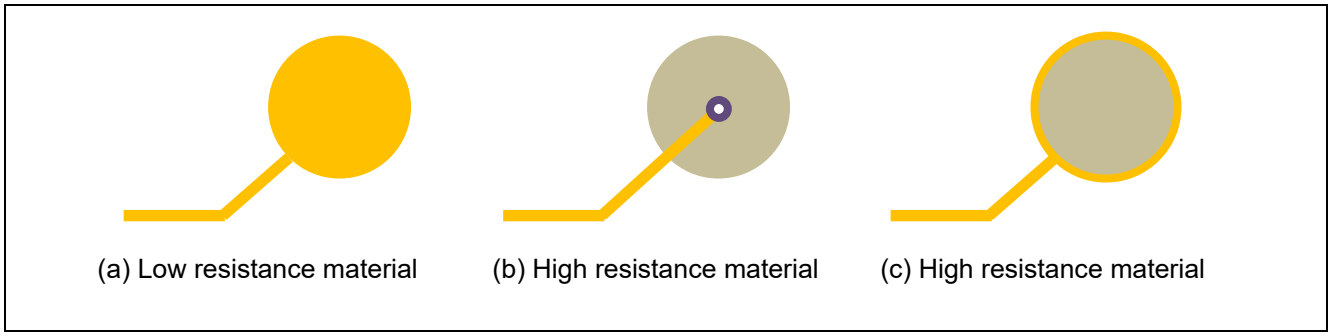


Figure2-24. Button Electrode Wiring Method

2.7.4 LED wiring layout

2.7.4.1 Direct lighting example

Figure2-25 shows the electrode pad and LED wiring for the self-capacitance method. We recommend routing the LED around the outer edge of the electrode pad, as shown to the right of the figure. To reduce noise radiated from the LED circuit, cover the LED wiring with a GND shield and, for multi-layer boards, cover the opposite surface with a GND shield as well.

Note that routing the LED wiring in the electrode pad requires a hole to be made in the electrode, reducing the touch-sensitive surface area and bringing the LED wiring in close proximity to the electrode. This increases the risk of weaker sensitivity due to an increased parasitic capacitance.

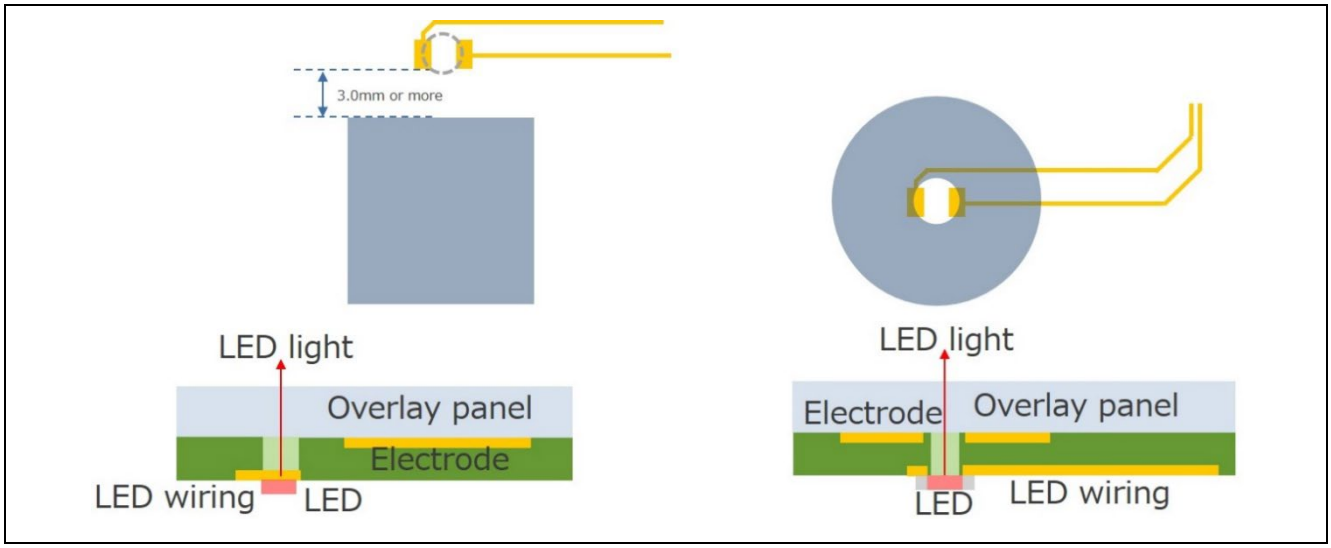


Figure2-25. Electrode Pad and LED Routing Example for Self-capacitance Method

2.7.4.2 Indirect lighting (using light guide plate)

Figure2-26 shows an example of LED routing using an electrode pad and a light guide plate for the self-capacitance method. The LED (the light source) must be a set distance from light-emitting surface to ensure even lighting. Placing multiple LEDs (light sources) in opposing positions helps to eliminate uneven lighting.

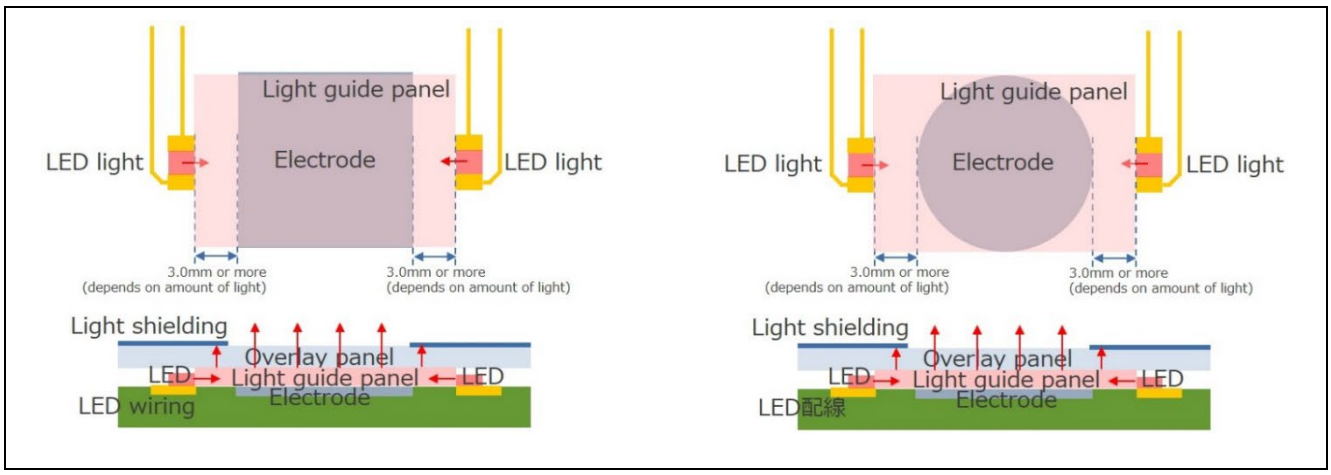


Figure2-26. Example of LED Routing using Electrode Pad Light Guide Plate for Self-capacitance Method

2.7.5 When panel and button electrodes are separated

Figure2-27 shows an example configuration with space between the panel and button electrodes. Although the configuration depends on the size of the button electrode, parasitic capacitance, and other factors, if all conditions are favorable, touch can be detected even with a 2mm air gap between the panel and electrodes. However, when dealing with strict noise immunity requirements, if the air gap is larger than 2mm and touch detection is difficult due to other conditions, you may need to extend the button electrodes to the panel, as shown on the right of the figure.

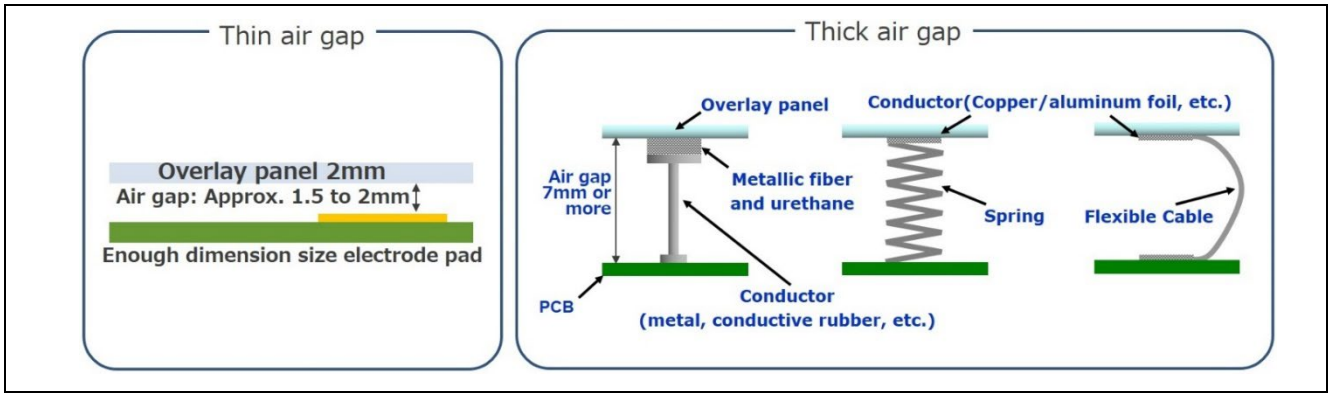


Figure2-27. Example of Air Gap Measure for Auto-capacitance Method

3. Mutual Capacitance Method: Electrode Layout Patterns

3.1 Outline

The mutual-capacitance method boasts button electrodes with superior water-resistance, support based on using matrix structure, and many other functions not available with self-capacitance. However, mutual-capacitance requires complicated button electrode configurations and wire routing, making sensitivity adjustment difficult. The merits and demerits of each method must be taken into account when designing layout patterns. Furthermore, unlike the self-capacitance method, sensitivity is lost when panel thickness falls below a specified level. The designer must carefully consider the button electrode configuration when determining panel thickness.

Always use a multi-layer board of at least two layers for the mutual-capacitance method. This chapter describes a double-layer board as an example.

3.2 Outline of Design Recommendations

This section provides reference design information for creating mutual-capacitance method buttons on a printed board. We recommend placing a cross-hatched pattern GND shield guard around the electrodes. We also recommend using an ESD countermeasure by shielding the outer circumference of the board with a GND plane pattern. The numbers listed here correspond to the numbers in each figure, excluding numbers 8 and 9. Each item is described in detail later.

① Electrode shape: square (combined transmitter electrode TX and receiver electrode RX)

② Electrode size: 10mm or larger

③ Electrode proximity: Electrodes should be placed with ample distance so that they do not react simultaneously to the touch object (finger, etc.), (suggested interval: button size x 0.8 or more)

④ Wire width: The thinnest wire capable through mass production; approx. 0.15mm to 0.20mm for a printed board

⑤ Wiring length: Make the wiring as short as possible. On corners, form a 45-degree angle, not a right angle.

⑥ Wiring spacing:

(A) Make spacing as wide as possible to prevent false detection by neighboring electrodes.
(B) When electrodes are separated: 1.27mm pitch
(C) 20mm or more to prevent coupling capacitance generation between Tx and Rx.

⑦ Cross-hatched GND pattern (shield guard) proximity

Because the pin parasitic capacitance in the recommended button pattern is comparatively small, parasitic capacitance increases the closer the pins are to GND.

A: 4mm or more around electrodes

We also recommend approx. 2-mm wide cross-hatched GND plane pattern between electrodes.

B: 1.27mm or more around wiring

⑧ Tx, Rx parasitic capacitance: 20pF or less

⑨ Electrode + wiring resistance: 2kΩ or less (including damping resistor with reference value of 560Ω)

⑩ Do not place GND pattern directly under the electrodes or wiring.

The active shield function cannot be used for the mutual-capacitance method.

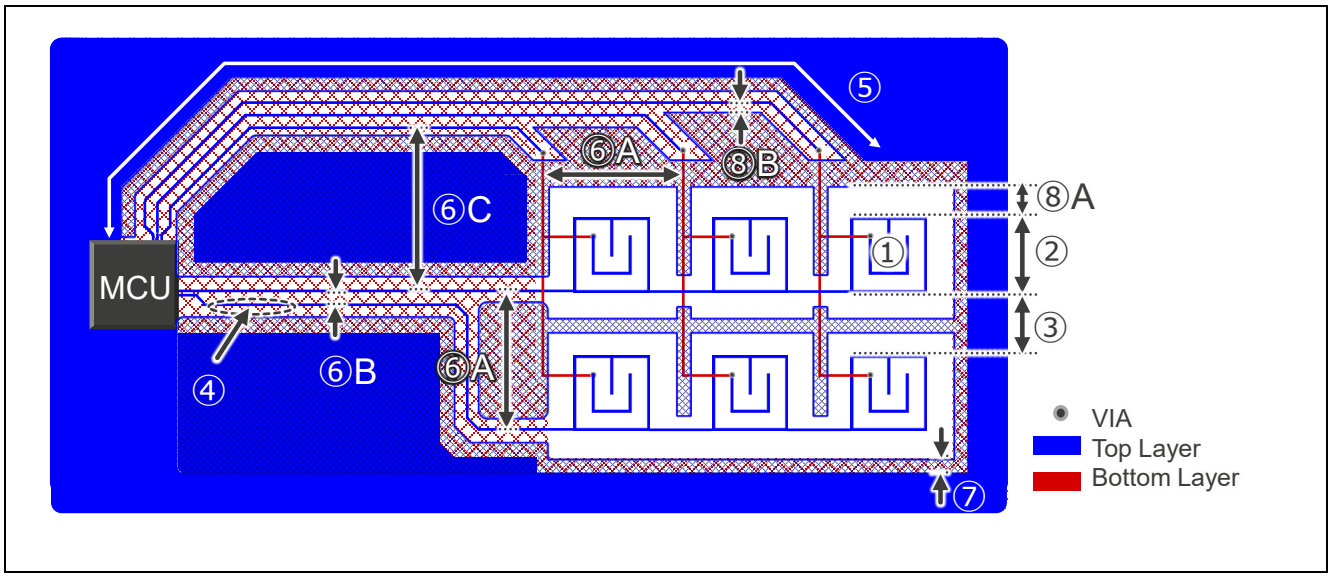


Figure3-1. Example of Button Pattern for Mutual-capacitance Method

3.3 Mutual-capacitance Method Overview

Figure3-2 shows the mutual-capacitance generated in the electrode. The mutual-capacitance method is characterized by parasitic capacitance Cm which is generated between two differing conductors. The mutual-capacitance method button comprises two electrodes, receiver electrode RX and transmitter electrode TX, connected to a capacitive sensor. An electric field is generated when Tx is pulse-driven, and electric charge is also accumulated in Cm. When a finger comes close to the electrode, parasitic capacitance Cf is generated between the finger and the electrode, and Cm and Cf are connected in parallel. Since the driving energy of Tx is constant, the amount of electric charge does not change. Therefore, the charge on Cm and Cf is dissipated and the Cm electric charge decreases. By setting a threshold for the amount of increase in Cf, you can determine whether the touch button is ON or OFF. Note that if the finger actually touches the electrode, it will short and no longer be able to measure capacitance. Normally, there is an overlay panel of a few mm between the electrode and the finger.

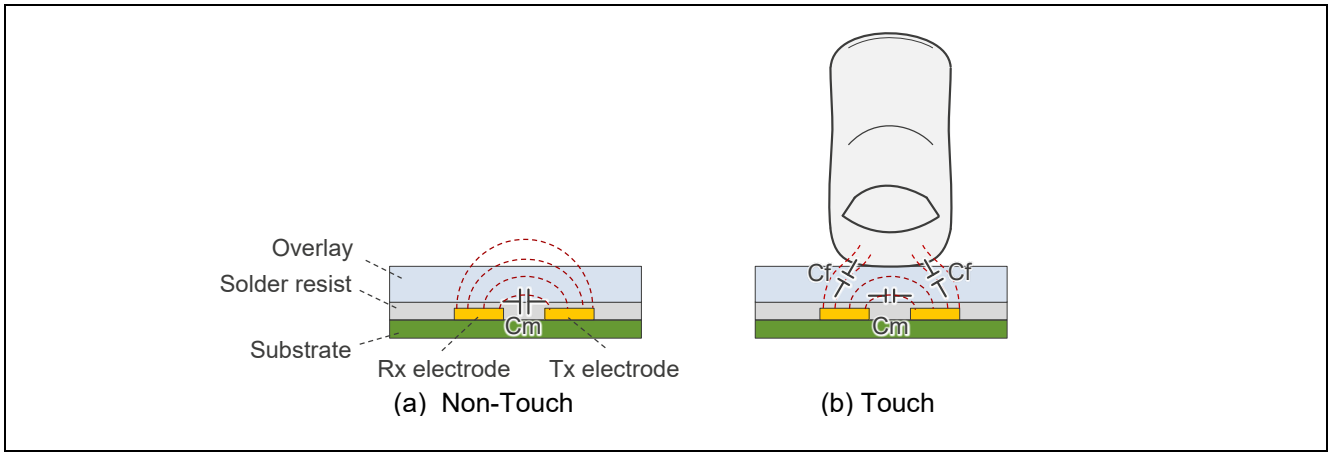


Figure3-2. Image of Mutual-capacitance Electrodes

3.4 Principle of CTSU Mutual-capacitance Method Detection

Figure3-3 shows an overview of the CTSU internal configuration for the mutual-capacitance method. The CTSU outputs a digital count that is negatively proportional to the mutual capacitance of Rx and Tx connected to the electrode, and determines whether the touch button is ON or OFF by software.

In order to measure the capacitance Cm existing on the two connected electrodes, the CTSU obtains Cm by inverting the phase relationship between the pulse output and the switched capacitor, measuring the self capacitance twice, then calculating the difference of the two values by software. For more details on the mutual-capacitance detection principle, refer to the application note “RX113 Group CTSU Basis of Cap Touch Detection.”.

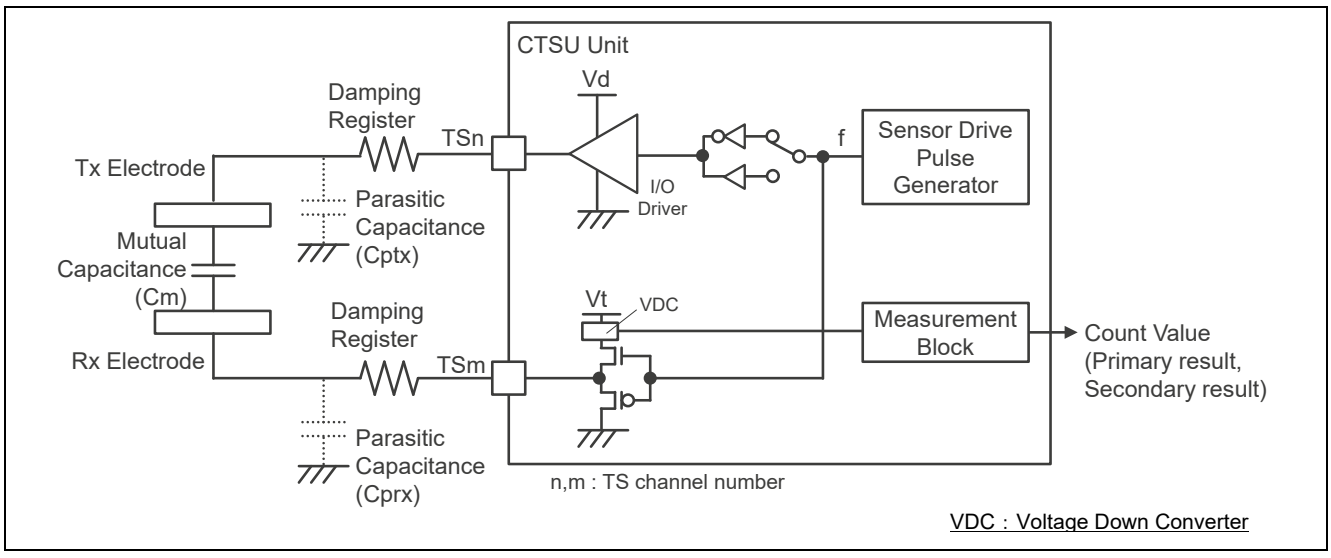


Figure3-3. Internal Configuration Outline for Mutual-Capacitance Method

3.5 Electrode Pattern Designs

Figure3-4 shows an electrode circuit for the mutual-capacitance method. Mutual-capacitance method button electrodes are configured as receiver electrode (Rx) and transmitter electrode (Tx). In the mutual-capacitance method, the total capacitance value for 1 electrode should be 20pF or less, and the total resistance (including protective resistor value) should be 2kΩ or less. The total capacity value for each electrode can be confirmed using QE for Capacitive Touch.

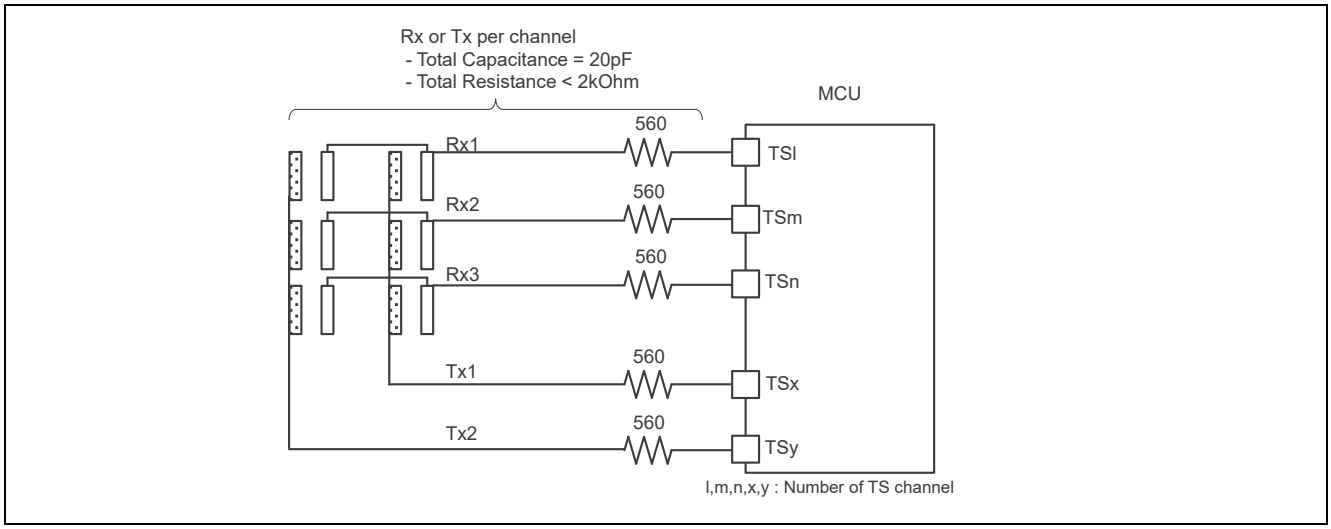


Figure3-4. Electrode Circuit for Mutual-capacitance Method

Figure3-5 shows the recommended electrode pattern for the mutual-capacitance method. The receiver electrode, which is more susceptible to noise, is protected by encompassing the sides of Rx with the sides of Tx. This configuration increases the distance between Tx and Rx opposing sides (called “facing distance” herein) as well as the surface area that comes in contact with the finger. This pattern supports an overlay thickness of 2mm to3mm.

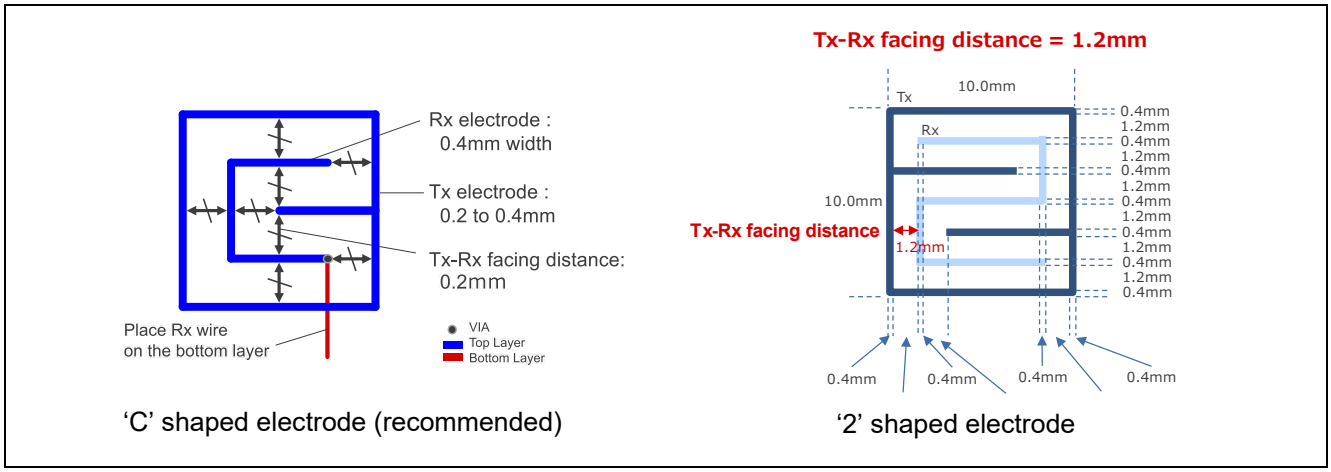


Figure3-5. Mutual Capacitance Method: Recommended Electrode Patterns

Mutual-capacitance method touch measurement measures the electromagnetic field (capacitive coupling) between Tx and Rx and captures the phenomenon of the capacitive coupling decreasing as a fingertip (i.e., part of the human body) in close proximity attracts part of the electromagnetic field. Therefore, the layout pattern must be designed to (1) maximize the capacitive coupling between Rx and Tx, and (2) make the rate of capacitance coupling reduction as large as possible when a finger is in proximity

Figure3-6 shows an image of the Tx/Rx coupling capacitance electromagnetic field for mutual-capacitance method electrodes. A greater Tx/Rx facing distance is required when using a thick overlay panel. However, as most products limit the electrode size, it is often difficult to extend the Tx/Rx distance. As shown in Figure3-5, you may need to use an electrode with a shorter Tx/Rx distance like the Type C electrode, but compared to the Type 2 electrode, the shorter Tx/Rx distance of the Type C electrode means the measured value may also be smaller.

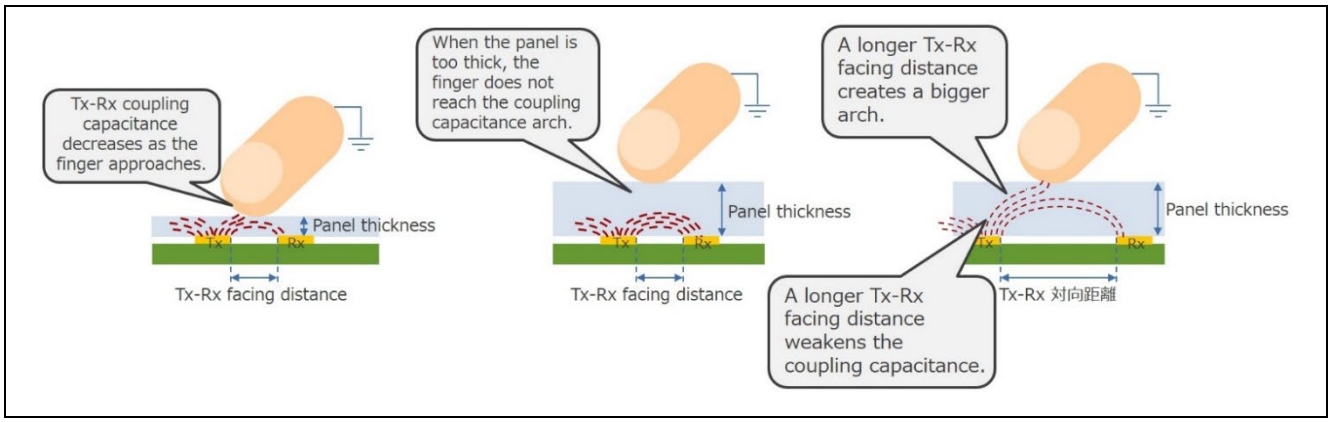


Figure3-6. Image of Electrode Tx-Rx Capacitance Coupling for Mutual Capacitance Method

Figure3-7 shows an image of capacitance coupling based on electrode pad Tx/Rx parallel run distance and Tx/Rx facing distance in the mutual-capacitance method. The longer the parallel run distance of transmitter electrode Tx and receiver electrode Rx, the larger the Tx/Rx coupling capacitance, which results in greater change in the measured value when a touch is detected. When electrode pads are the same size, the longer the Tx/Rx parallel run distance, the more complicated the layout. In addition, a longer Tx/Rx facing distance supports thicker overlay panels and air gaps, but creates a denser electromagnetic field, leading to lower sensor counts.

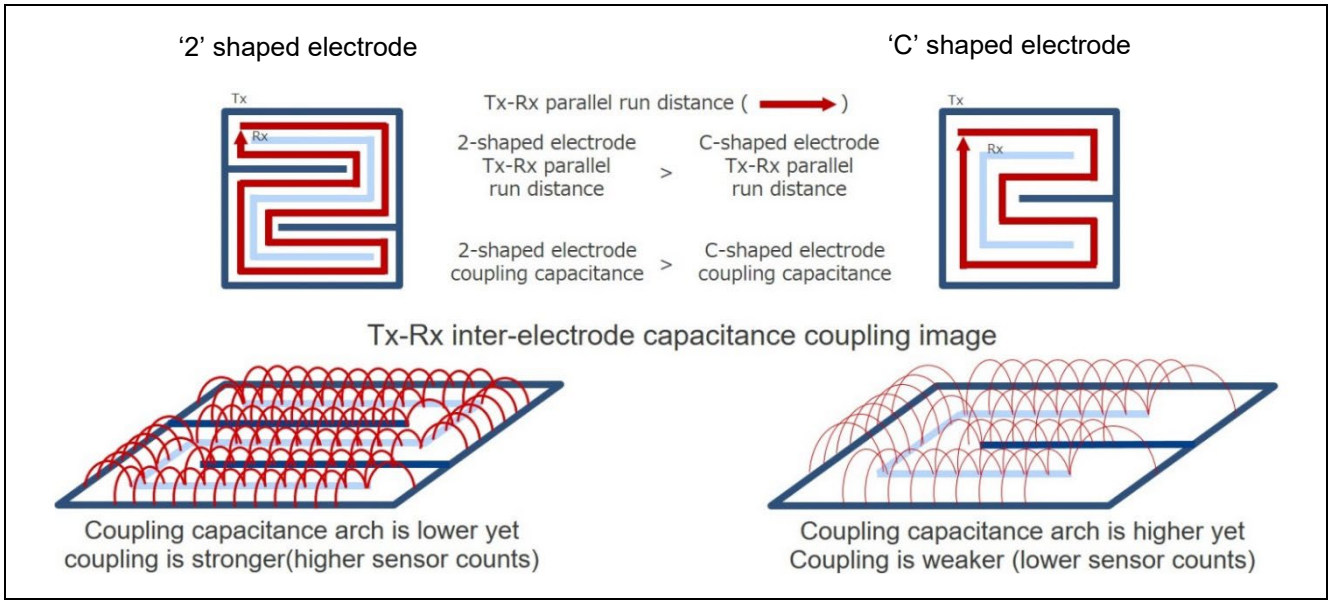


Figure3-7. Image of Capacitance Coupling Based on Electrode Tx/Rx Parallel Run Distance and Facing Distance for Mutual-capacitance Method

3.6 Air Gap

Figure3-8 shows the electrode Tx/Rx coupling capacitance electromagnetic field and air gap (incl. panel thickness) for the mutual-capacitance method. In this method, when the layout design includes an air gap between the electrode and overlay panel, the Tx/Rx facing distance must be as long as possible, in the same manner as when using a thick panel. The facing distance between the transmitter electrode Tx and receiver electrode Rx depends on the panel thickness. The recommended Tx/Rx facing distance is approx. 0.6 times the panel and air gap thickness.

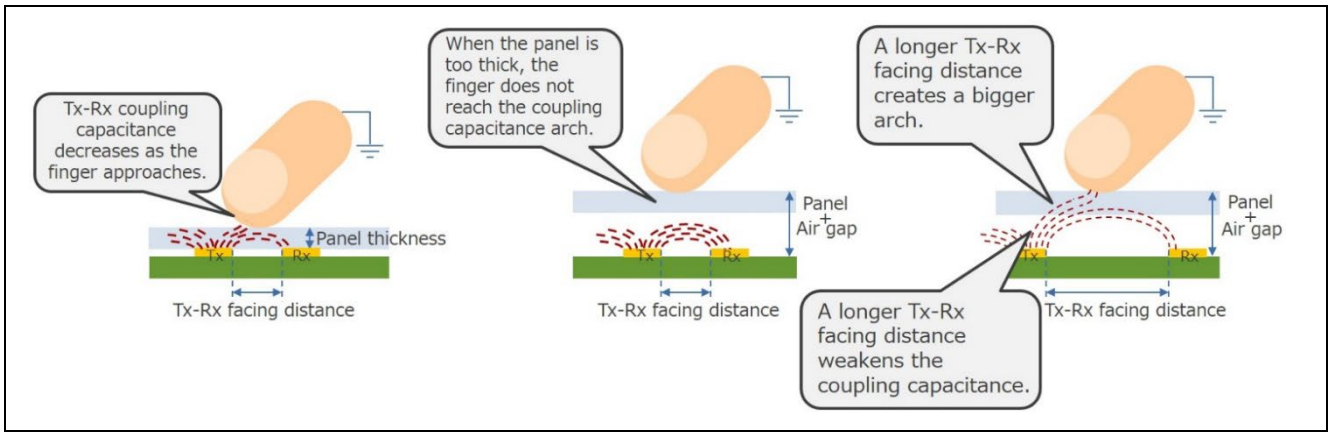


Figure3-8. Tx/Rx Coupling Capacitance Electromagnetic Field and Air Gap (incl. panel thickness) for Mutual Capacitance Method

3.7 Distance from Touch Surface to Electrode

Figure3-9 shows the relationship between the amount of capacitance change and the sensitive electrode. In the mutual capacitance method, no matter how close or far apart the finger (human body) and electrodes are, the decrease in Tx/Rx coupling capacitance will be reduced, so panel thickness and air gap thickness are factors to keep in mind at the design stage. As mentioned earlier, the ideal optimal panel thickness, including the air gap, is 1.7 times the distance between the Tx/Rx electrodes.

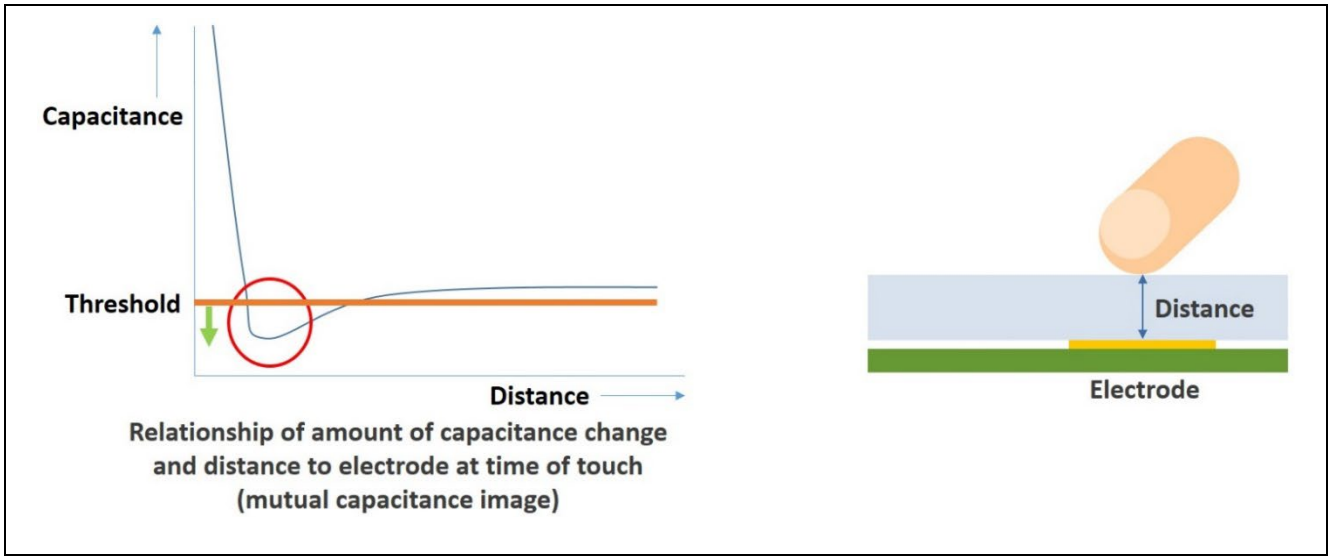


Figure3-9. Relationship of Capacitance Change and Sensitivity Distance for Mutual-capacitance Method

Figure3-10 shows the relationship between inter-electrode distance and panel thickness in the mutual capacitance method. To avoid false detections (crosstalk) between neighboring electrodes, the recommended inter-electrode distance is 2 times or more the panel thickness (including the air gap).

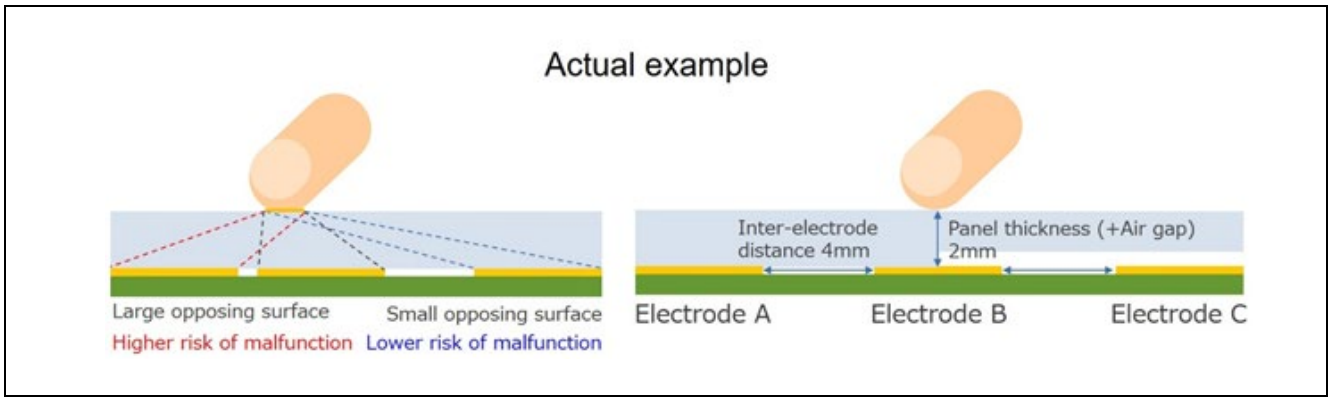


Figure3-10. Relationship of Inter-electrode Distance and Overlay for Mutual-capacitance Method

3.8 Electrode Routing Design

Figure3-11 shows an electrode routing example for the mutual capacitance method. Tx and Rx electrode wiring must be routed with ample distance from neighboring button electrodes and other areas where finger touch is anticipated. This clearance distance will reduce the risk of false detection due to a non-accurate touch, which may occur when a non-electrode pad area is touched. It is important to separate the Tx and Rx electrode wiring so that an unintentional touch does not occur across both traces at the same time. Similarly, if the touch measurement pins (TS) set to Rx and Tx are adjacent, coupling capacitance may occur between the two pins, reducing the relative rate of decreasing capacitance, thus causing a decrease in sensitivity. To prevent capacitive crosstalk, group the Rx and Tx lines separately and keep them as far away as possible

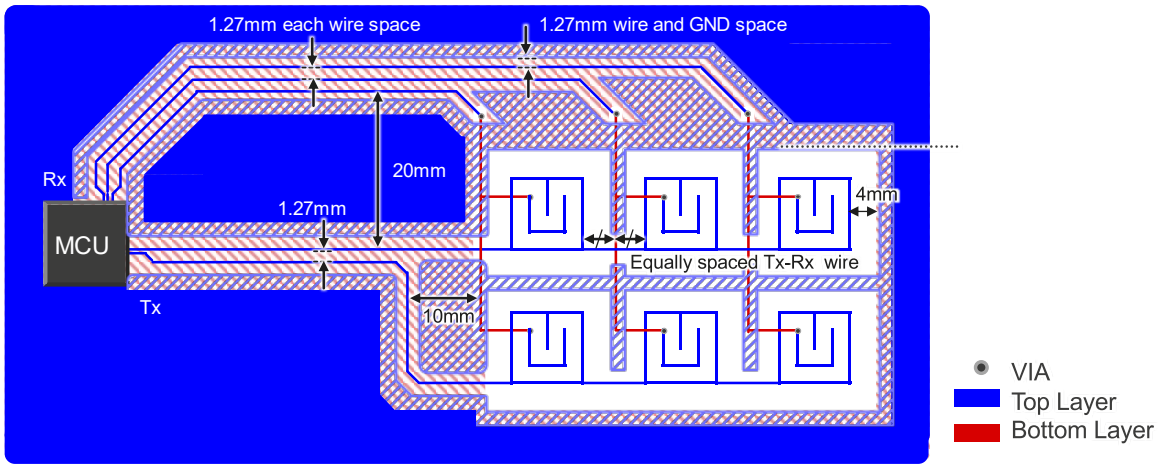


Figure3-11. Example of Electrode Routing for Mutual-capacitance Method

Figure3-12 shows the electrode wiring restrictions that apply in the mutual-capacitance method. Tx and Rx electrode wiring should not be routed in parallel in short range within the wiring area; they must be kept as far apart as possible. If the wiring must cross due to board constraints, do so at a 90º angle as far from the electrode as possible, and then separate the wiring immediately.

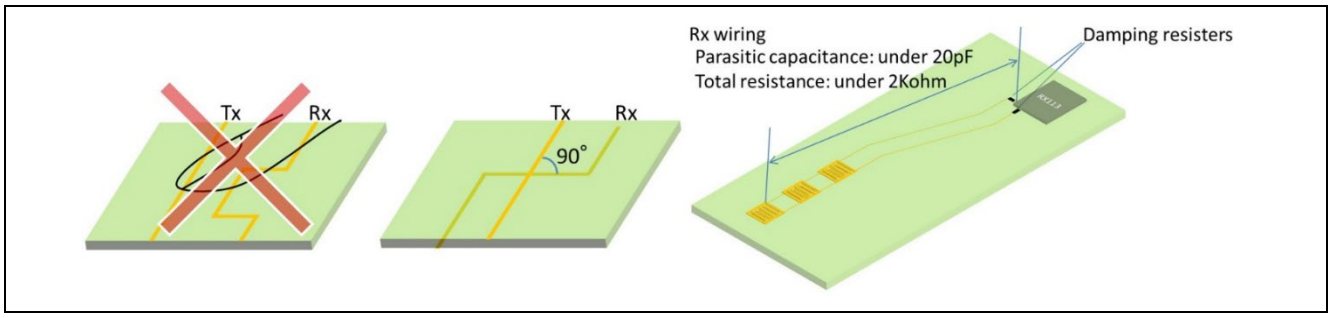


Figure3-12. Electrode Wiring Restrictions for Mutual Capacitance Method

3.9 Anti-noise Layout Pattern Designs

The electrode circuit configuration makes the electrode act as an antenna (the MCU pin is open only for coupling capacitance) and makes it vulnerable to electromagnetic field noise. Renesas Touch MCUs employ several anti-noise countermeasures to ensure high noise immunity. However, an MCU alone cannot prevent influence from all noise. Hardware countermeasures are indispensable when using the MCU in a severe noise environment. This section includes several design examples.

In general, the longer the wiring, the more chances for noise to synchronize and mix with the many noise frequencies. Make sure the wiring between button electrodes and the MCU is kept as short as possible.

The active shield cannot be used for the mutual capacitance method.

3.9.1 Pattern Designs

3.9.2 Shield guard anti-noise countermeasure

A GND pattern is placed around the electrodes and wiring to generate capacitive coupling and suppress potential fluctuations due to the effects of external noise. Placing the GND shield too close to the electrode may cause the parasitic capacitance to increase too much, blocking touch detection. If the noise environment is severe and the shield needs to be brought closer, we recommend using a cross-hatched configuration as the ground pattern to minimize capacitive coupling. The Renesas Capacitive touch Evaluation System employs a cross-hatched pattern in the dimensions listed below. In addition, the cross-hatched pattern is tilted 45 degrees depending on the wiring direction in order to reduce the capacitive coupling with the electrode wiring. Also, the longer the wiring must run in parallel, the more the parasitic capacitance increases. Therefore, you may need to adjust the distance between the wiring and the shield.

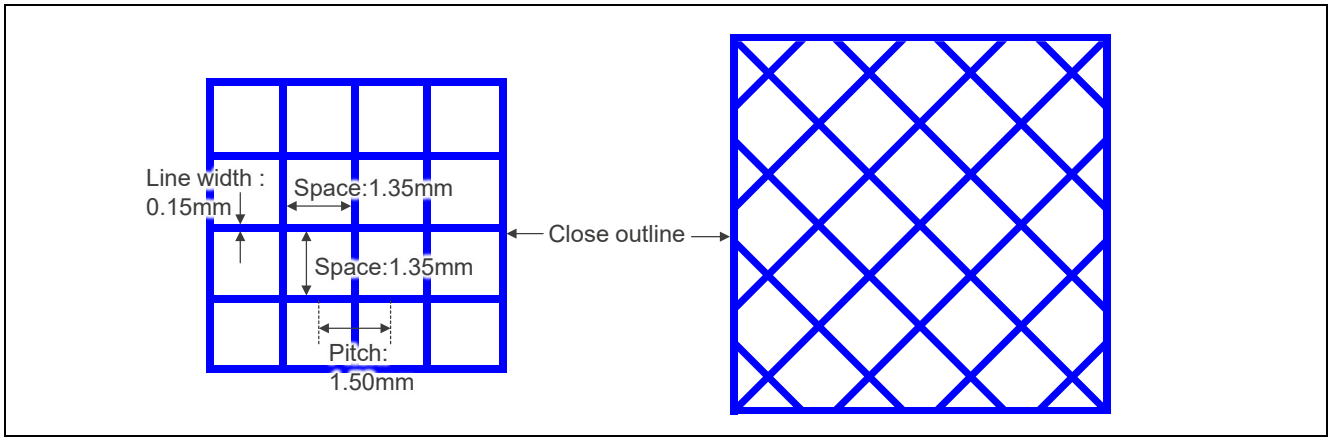


Figure3-13. Cross-hatched Pattern Dimensions

Figure3-14 and Figure3-15 shows an anti-noise layout pattern example for the mutual capacitance method. We recommend using a cross-hatched ground pattern to cover the area around the electrode wiring. When the entire wiring area cannot be covered due to layout limitations, place priority on covering the area around the Rx electrode wiring with the cross-hatched GND pattern. Make sure the distance between the electrode wiring and the cross-hatched GND is 4mm or more.

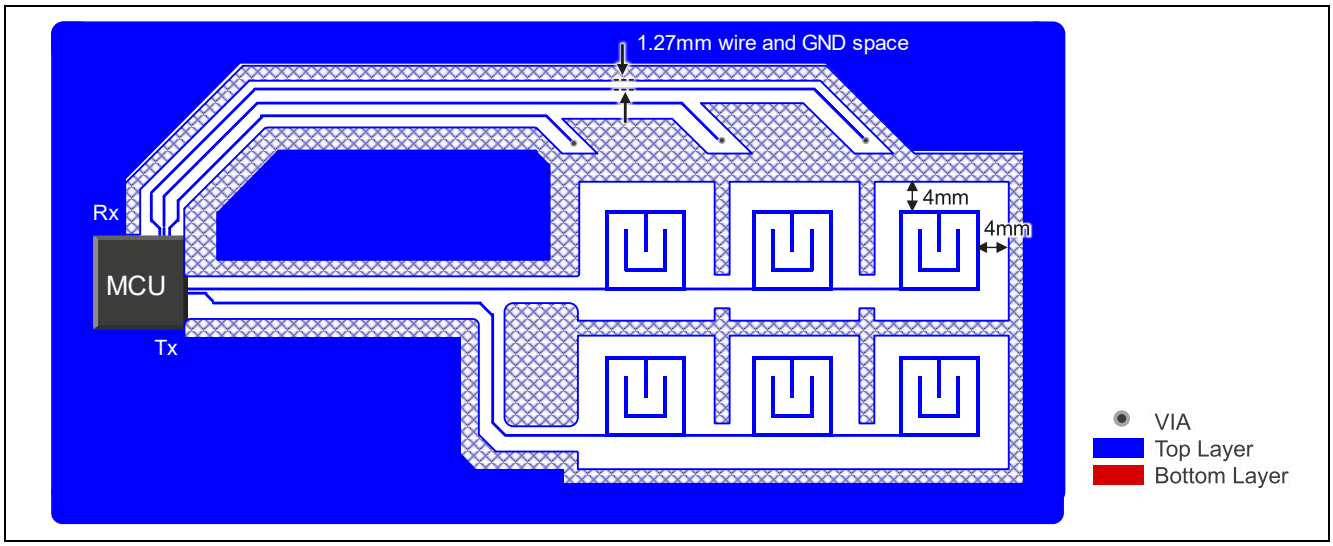


Figure3-14. Anti-noise Countermeasure Layout Pattern Example (top layer)

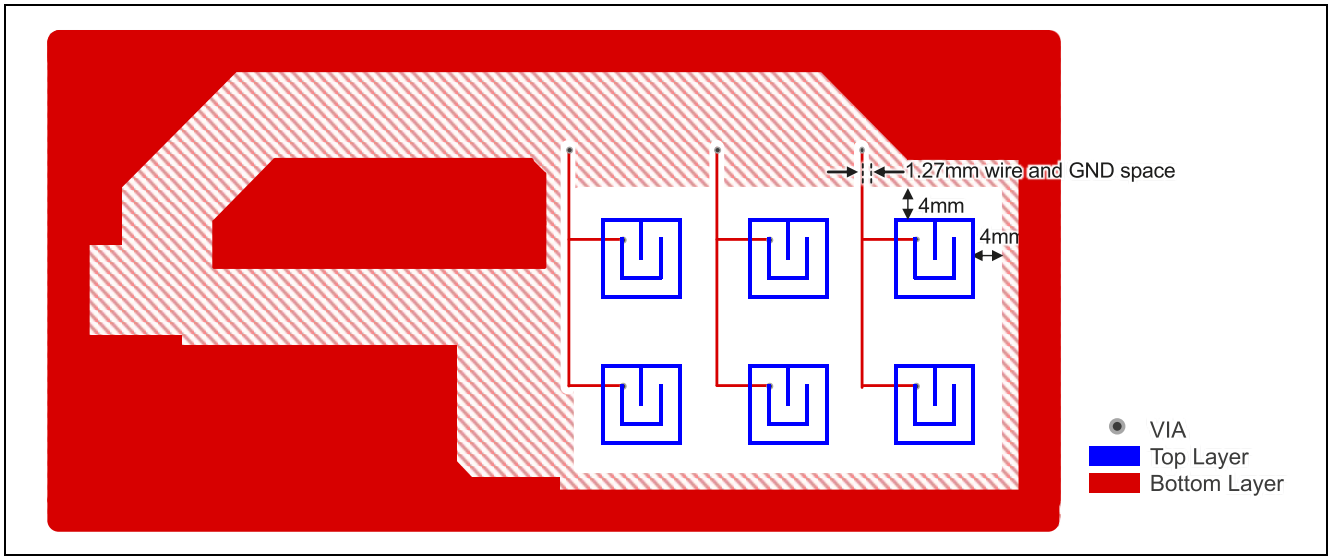


Figure3-15. Anti-noise Countermeasure Layout Pattern Example (bottom layer)

3.10 Design Application Examples

3.10.1 Water-resistant electrode layout pattern design

Figure3-16 depicts cautions regarding water-resistant electrode layout patterns for the mutual capacitance method. If the device is used under flowing water and a water film forms on the electrode surface, when the fingertip touches the water film, the effect is almost as if all electrodes under the water film are touched. This state greatly increases the risk of false detection (crosstalk) between adjacent electrodes in inverse proportion to the resistance value of the flowing water. Using sensing devices in the ocean or in other water containing electrolytes will deteriorate the operating conditions for electrostatic touch. The resistance value of the water film is reduced due to an increasingly thicker water film and a high dielectric constant of the water, which is increased even further by the electrolytes.

Products that require water resistance must be designed with wide spaces between electrode pads as a countermeasure against false detections between adjacent electrodes.

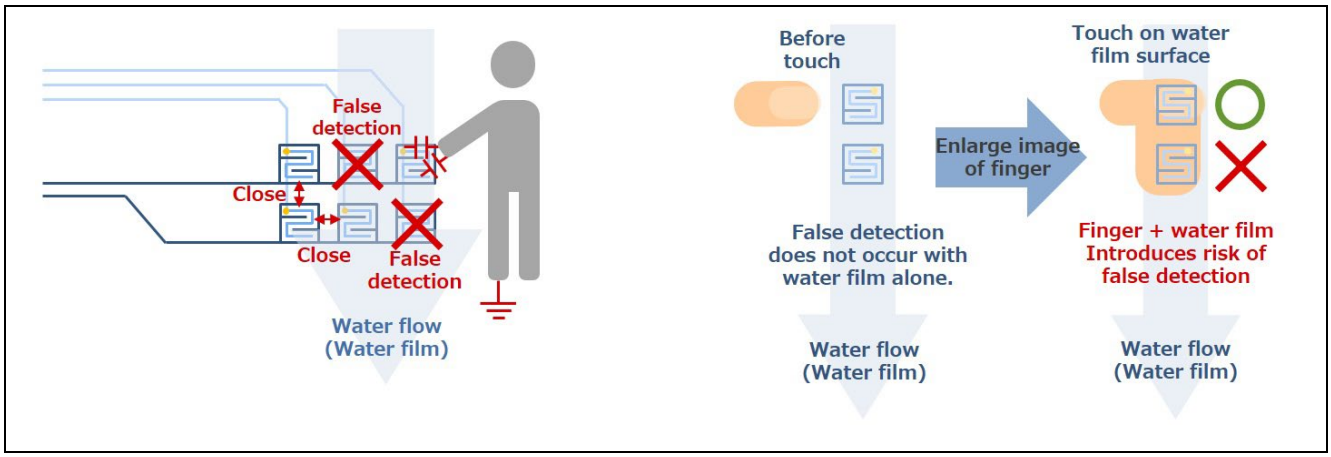


Figure3-16. Cautions for Water-resistant Electrode Layout Pattern in Mutual-capacitance Method

Figure3-17 shows the recommended water-resistant electrode layout for the mutual-capacitance method. Considering that water flows from top to bottom, the best water-resistant layout would be to position all electrodes in a single horizontal line.

Since the Tx wiring, which is not used by the electrode during measurement, outputs low, all Tx can be grouped into one line for water-resistant designs. This will enable the L level output by non-active Tx wiring to bridge with other electrodes via the water film, preventing false detections.

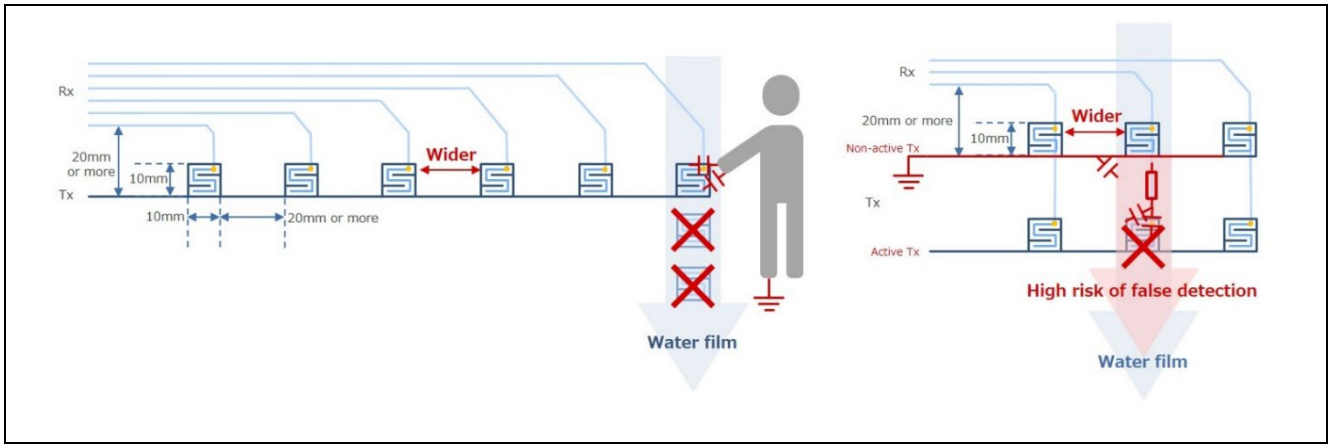


Figure3-17. Recommended Water-resistant Electrode Layout for Mutual-capacitance Method

Figure3-18 shows the relationship between electrode proximity and the panel thickness for the mutual capacitance method. To prevent false detection between adjacent electrodes (crosstalk), the recommended inter-electrode distance is 2 or more times the thickness of the panel overlay (including air gap).

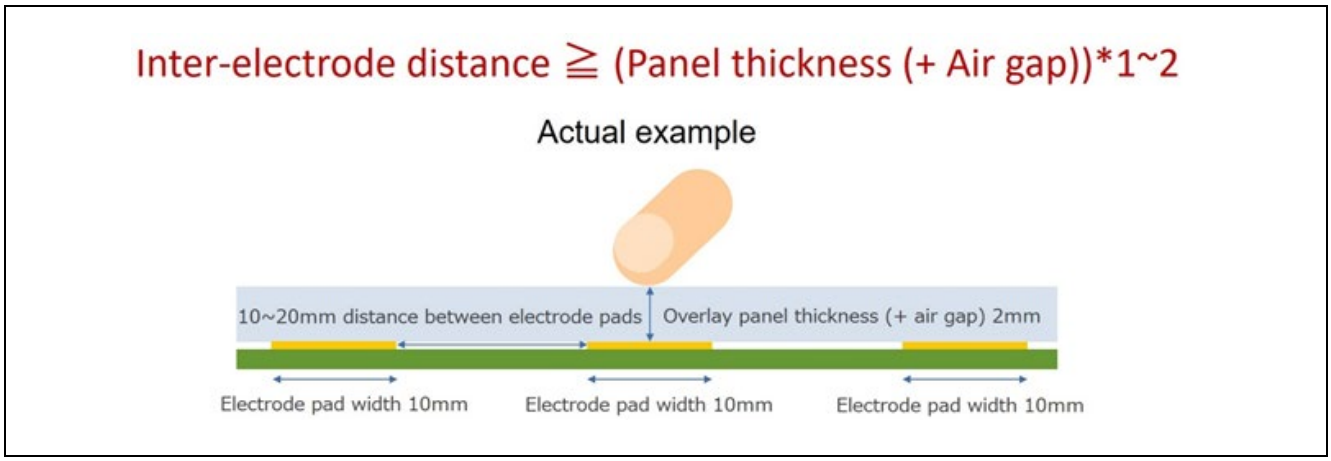


Figure3-18. Relationship of Water-resistant Inter-electrode Distance and Overlay for Mutual-capacitance Method

3.10.2 LED wiring layout

3.10.2.1 Direct lighting example

Figure3-19 shows an example of the electrode pad and LED wiring for the mutual-capacitance method. The ideal routing is to position the LED around the outer edge of the electrode pad, as shown to the right of the figure. In the mutual capacitance method, the Tx/Rx facing area can be increased to improve detection sensitivity. However, this creates difficulty in positioning the LED wiring going into the electrode pad at the Tx and Rx electrodes. The Tx/Rx parallel runs are short and may cause sensitivity deterioration for electrode pads of the same size.

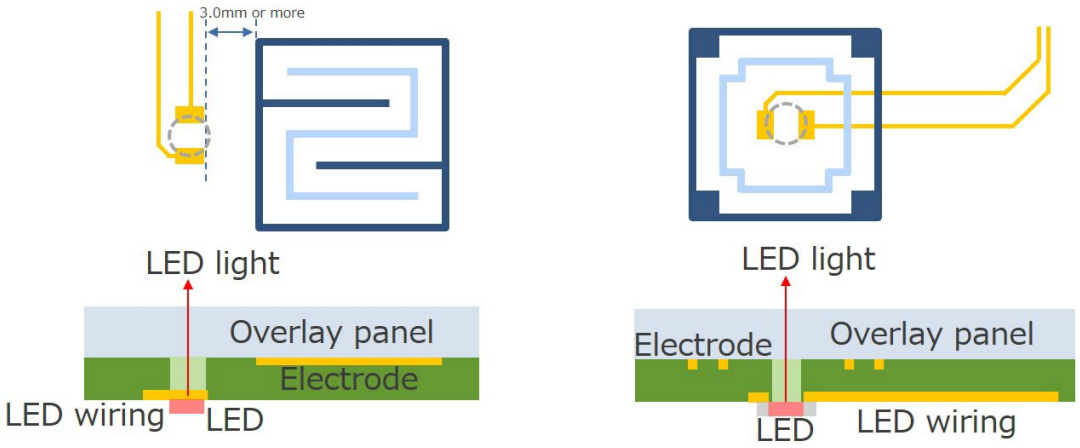


Figure3-19 Electrode Pad and LED Wire Routing for Mutual-capacitance Method

3.10.2.2 Indirect lighting example

Figure3-20 shows an LED routing example using an electrode pad and a light guide plate for the mutual capacitance method. The LED (the light source) must be a set distance from light-emitting surface to ensure even lighting.
Placing multiple LEDs (light sources) in opposing positions helps to eliminate uneven lighting.

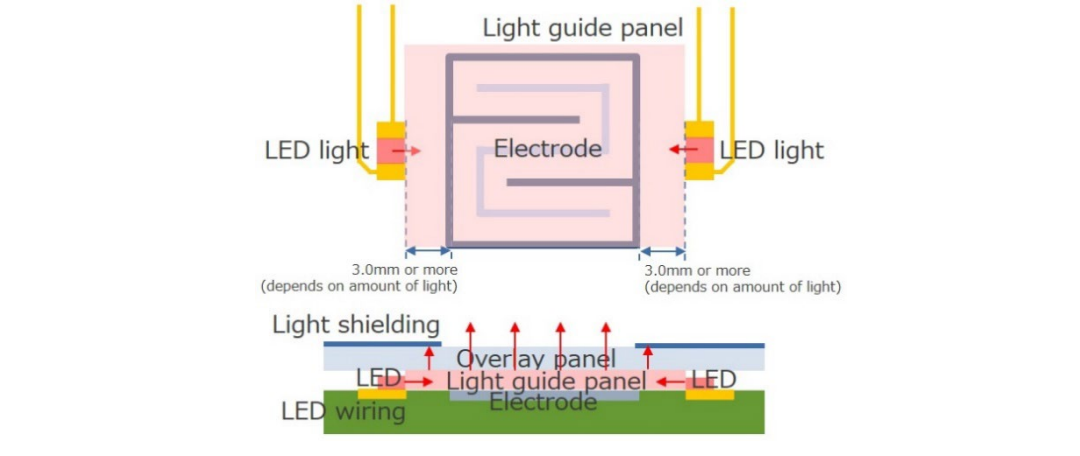


Figure3-20 LED Wire Routing with Electrode Pad and Light Guide Plate for Mutual-capacitance Method

4. Reference Documents

RX113 Group CTSU Basis of Cap Touch Detection（R30AN0218）
(The latest version can be downloaded from the Renesas Electronics website.)

5. Self-capacitance Method Button Patterns and Characteristics Data

The characteristics of capacitive touch buttons vary depending on the combination of various design parameters such as electrode size and wiring pitch. This chapter provides data on how sensitivity is affected when individual design parameters of self-capacitance method buttons are varied. By combining the data for each parameter, you can estimate what risks may occur during board design.

The data provided in this application note does not guarantee the electrical characteristics of each MCU. When designing a board, prototyping and sufficient evaluation should be carried out by the user to determine whether a specific MCU can be used or not.

5.1 Self-capacitance Method Button Sensitivity (SNR)

This chapter defines button sensitivity based on Signal to Noise Ratio (SNR). Figure 5-1 shows Button Sensitivity (SNR) Derivation Method. The SNR is calculated from the count difference value and noise value when the button is touched and not touched. The measured value is the average of an arbitrary number of samples. In this document, the noise value is ±3σ of the standard deviation of an arbitrary number of samples; the worse of the touch or non-touch measurements is adopted. The noise value may increase or decrease depending on the data acquisition time, so evaluate with sufficient sample acquisition time for better accuracy.

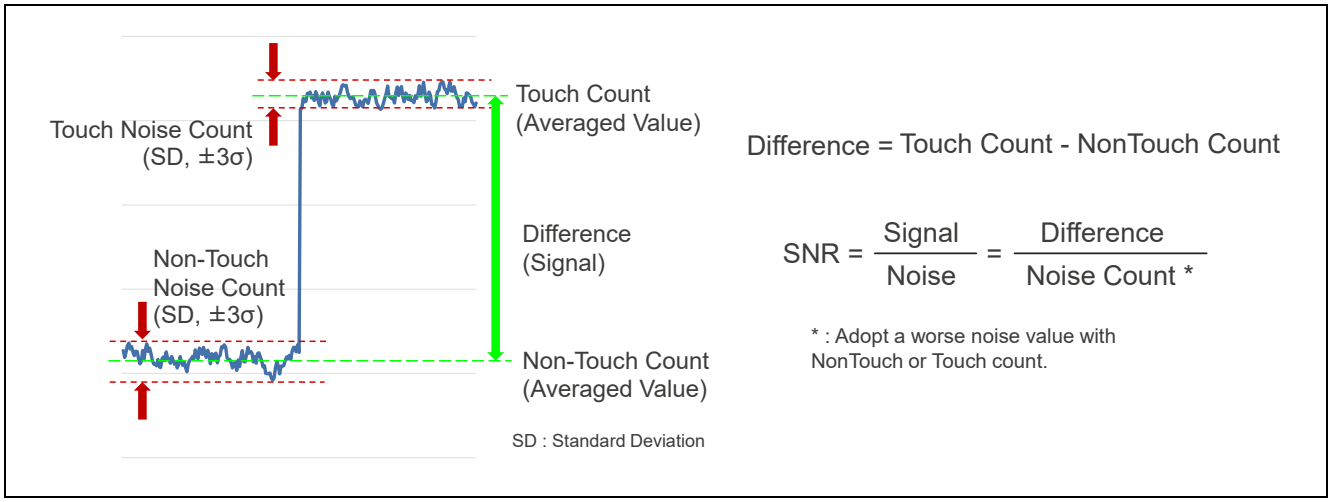


Figure 5-1 Button Sensitivity (SNR) Derivation Method

Table 5-1 lists the measurement results shown in Figure 5-1. When the difference value is 1491 and the noise value is 78 at the time of button touch, the SNR is 19. In this evaluation, the noise value for non-touch is applied because the noise was larger at non-touch.

Table 5-1 Measurement Results of Evaluation Board Pattern Example (REC design values, 1 button)

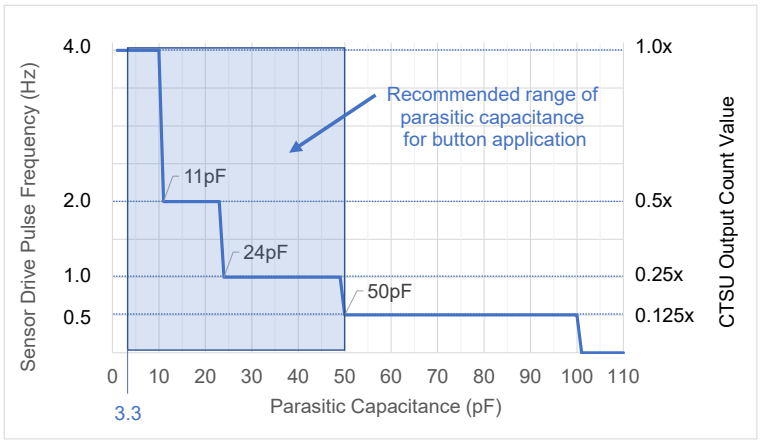
Item	Non-Touch	Touch	Difference
Parasitic capacitance (incl. CPU board)	17.29 pF	17.94 pF	0.65 pF
Parasitic capacitance (evaluation board only)	6.81pF	7.46pF	
Measured value	15379	16870	1420
Noise value	78	62	—
SNR	**19**		

Note: Sensor drive pulse frequency = 2MHz

5.2 Relationship of CTSU Measurement Range and Sensitivity

The sensor drive pulse frequency of the CTSU affects both the capacitance measurement range as well as the SNR. Figure 5-2 shows a Setting Example for Parasitic Capacitance and Sensor Drive Pulse Frequency. The conditions for this example are as follows: the MCU is RA2L1, supply voltage (VCC) is 5.0V, and damping resistance value is R=560 Ohm. Damping resistance value of 560 Ohm is recommended to protect the pins from external noise and limit the output current from pins. The QE for Capacitive Touch auto-tuning function selects the sensor drive pulse frequency from 4.0, 2.0, 1.0, and 0.5 MHz. The setting values differ according to the MCU used.

For self-capacitance method button applications, the recommended range of parasitic capacitance for button electrodes, including MCU pins, is 3.3 pF to 50pF. The recommended range indicates the range which the QE for Capacitive Touch automatic adjustment function can align with the measurement reference value of 15360. If the parasitic capacitance is below the recommended range, it will be outside the CTSU's offset adjustment range, resulting in a measurement reference value lower than 15360, with less margin for environmental and other parasitic capacitance fluctuations. If the range exceeds the recommended range, the drive pulse frequency will be lower, which may result in insufficient SNR.

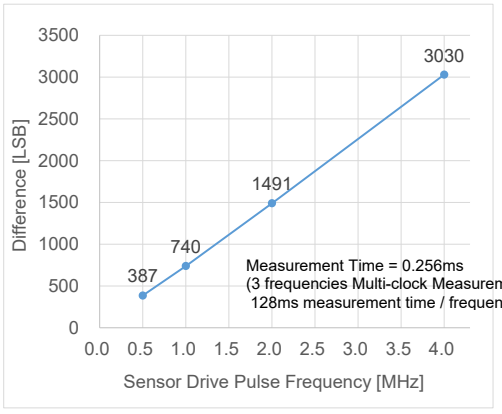


Conditions:
MCU = RA2L1, Vcc = 5.0V,
R = 560Ohm

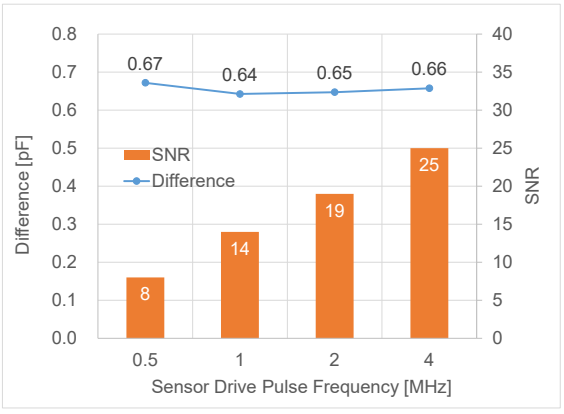
Note:
The frequency range may differ according to the MCU used.

Figure 5-2 Setting Example for Parasitic Capacitance and Sensor Drive Pulse Frequency

Figure 5-3 shows the Relationship of Sensor Drive Pulse Frequency and Sensitivity. The example shows the evaluation results when the sensor drive pulse frequency is varied on the evaluation board with the recommended design pattern shown in Figure 5-5. Figure 5-3 (a) shows the measured difference between touch ON and OFF for each sensor drive pulse frequency, which is proportional to the sensor drive pulse frequency. When the measured value is converted to a capacitance value, such as the detected capacitance (difference) at touch shown in Figure 5-3 (b), a constant value can be detected regardless of the sensor drive pulse frequency. On the other hand, the SNR improves in proportion to the sensor drive pulse frequency. The lower the sensor drive pulse frequency, the higher the amount of noise per count, and the SNR tends to decrease.



(a)Sensor drive pulse frequency and measured values



(b)Detected capacitance and SNR at touch

Figure 5-3 Relationship of Sensor Drive Pulse Frequency and Sensitivity

5.3 Evaluation Conditions

Table 5-2 Hardware Conditions

Item	Specification
CPU board	RA2L1 Cap Touch CPU Board (RTK0EG0018C01001BJ) (RA2L1 Capacitive Touch Evaluation System (RTK0EG0022S01001BJ) accessory)
MCU	RA2L1 (R7FA2L1AB2DFP)
Operating frequency	48MHz
Power supply	5.0V (powered via USB)
Pseudo finger	Φ8.0 x 50mm stainless steel rod

Table 5-3 Software Development Environment

Item	Specification
Integrated development environment	Renesas e² studio Version: 2022-01
Compiler	GCC ARM Embedded 10.3.1.20210824
RA FSP	Version 3.6.0
Development support tool for capacitive method touch sensor	QE for Capacitive Touch V3.0.2
Emulator	Renesas E2 emulator Lite

Table 5-4 Measurement Conditions

Item	Settings
CTSU resistor setting	Use results from automatic adjustment processing of QE for Capacitive Touch (Drive pulse frequency is determined by automatic adjustment; multi-frequency measurement = 3 times, measurement time = 0.128ms x number of multi-frequency measurements)
Measurement period	20ms (generated by hardware timer (AGT))
Data acquisition points	128 points
Data determination method	128 points averaged
TS pin parasitic capacitance measurement method	Use automatic adjustment process log of QE for Capacitive Touch

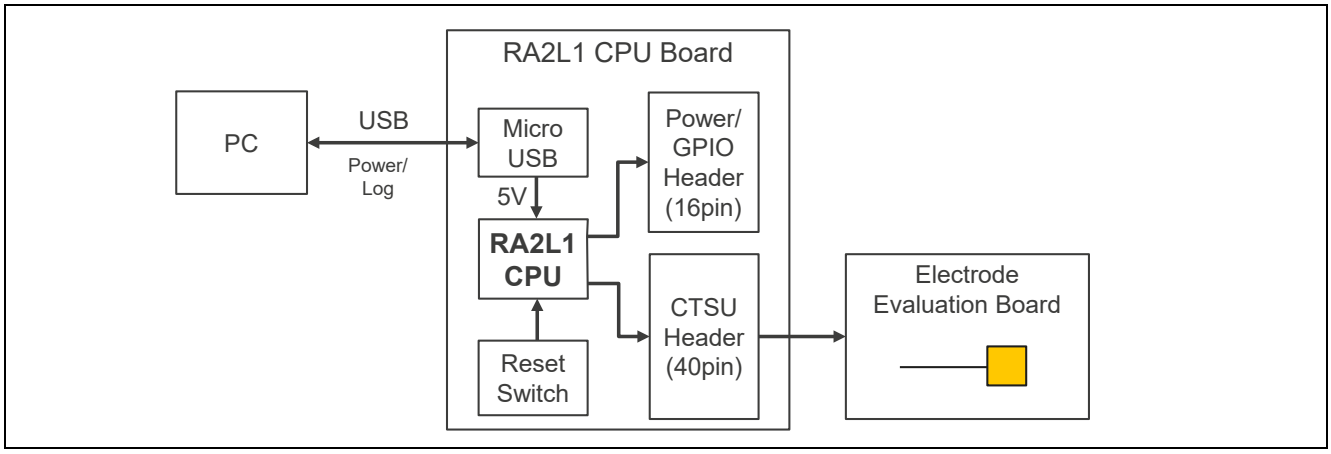
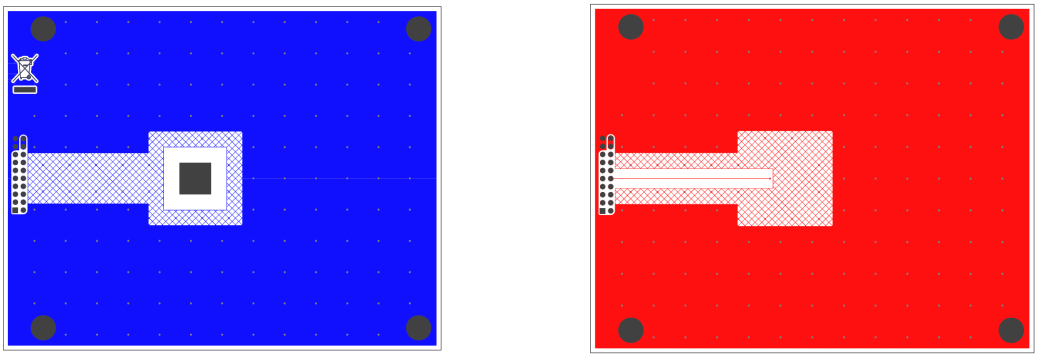


Figure 5-4 Evaluation Board Block Diagram

Table 5-5 shows the Recommended Electrode Design Values. Figure 5-5 shows an Evaluation Board Pattern Example (recommended design values, 1 button); Figure 5-6 shows an Evaluation Board Pattern Example (recommended design values, 3 buttons). The number of buttons is limited depending on the item so that other design parameters are not affected by the parameters that will be changed.

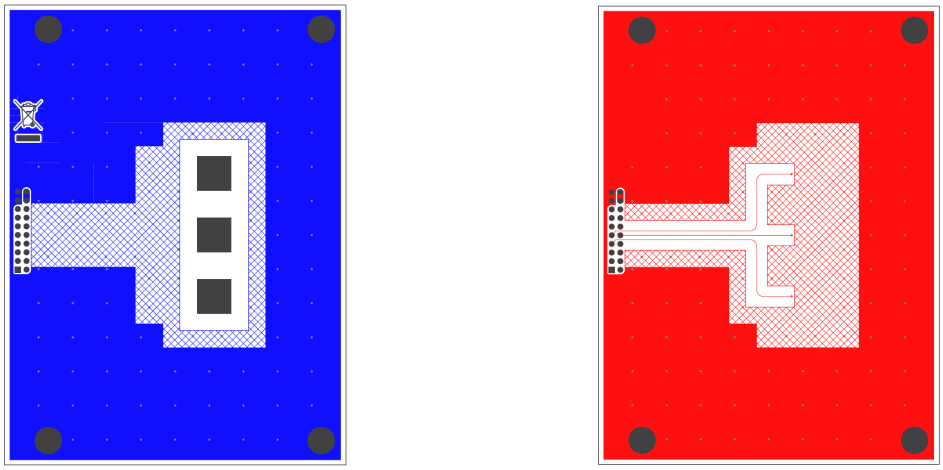
Table 5-5 Recommended Electrode Design Values

Parameter		Specification	Unit	Item in Figure2-1
Electrode (PAD)				
	Shape	Square or rectangle	-	①
	Size	10x10 to 15x15	mm	②
	Electrode proximity	Electrode size x 0.8	mm	③
	Cross-hatched GND pattern width	5.0	mm	⑦
	Distance between cross-hatched GND shield and electrode	5.0	mm	⑧A
Wiring				
	Wire width	0.15 to 0.20	mm	④
	Wire length	Shortest distance	mm	⑤
	Wiring pitch	1.27	mm	⑥
	Cross-hatched GND pattern width	3.0	mm	⑦
	Distance between cross-hatched GND shield and wiring	5.0	mm	⑧B
Damping resistor		560	Ohm	—



(a) Top layer (b) Bottom layer

Figure 5-5 Evaluation Board Pattern Example (recommended design values, 1 button)



(a) Top layer (b) Bottom layer

Figure 5-6 Evaluation Board Pattern Example (recommended design values, 3 buttons)

5.4 Design Parameters and Sensitivity Characteristics

This section provides examples of design parameters and sensitivity characteristics as well as the symbols used as abbreviations in the graphs showing various evaluation results. Table 5-6 lists Symbols Used in Graphs. Table 5-7 lists the Board Specifications used for evaluation.

Table 5-6 Symbols Used in Graphs

Symbol	Description
★	Electrode board with recommended design values
Difference	Difference between button touch and non-touch
L	Wiring length
$f_{0.5}$	Sensor drive pulse frequency = 0.5MHz
$f_{1.0}$	Sensor drive pulse frequency = 1.0MHz
$f_{2.0}$	Sensor drive pulse frequency = 2.0MHz
$f_{4.0}$	Sensor drive pulse frequency = 4.0MHz

Table 5-7 Board Specifications

Item	Specification
Board thickness	1.6mm
Material	FR-4
Number of layers	2 or 4 layers

5.4.1 Electrode Size

Table 5-8 shows the Board Specifications for Electrode Size Variation. For evaluation purposes, only the electrode size was varied; all other design parameters remained fixed.

Table 5-8 Board Specifications for Electrode Size Variation

Design Parameter	Specification	Unit	Notes
Electrode size	**5.0x5.0, 10x10 30x30, 50x50**	**mm**	**Square**
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

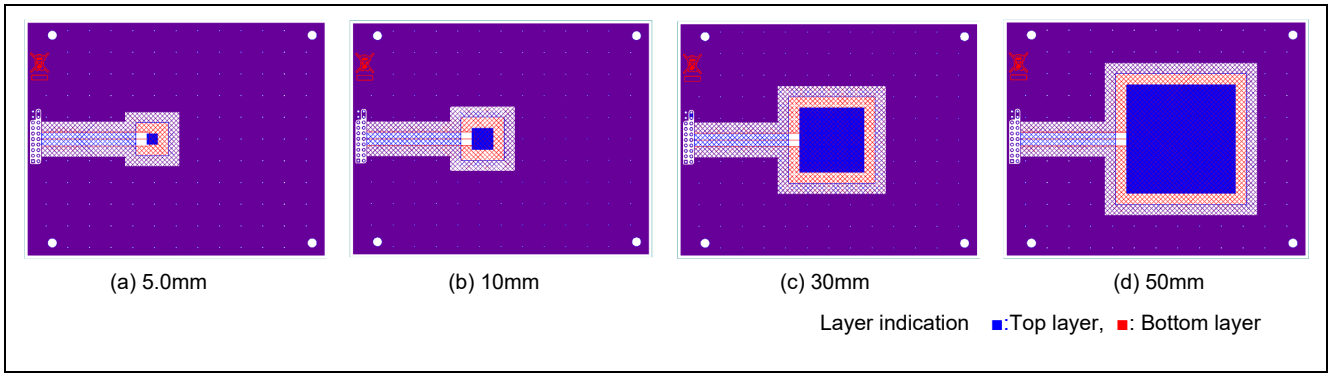
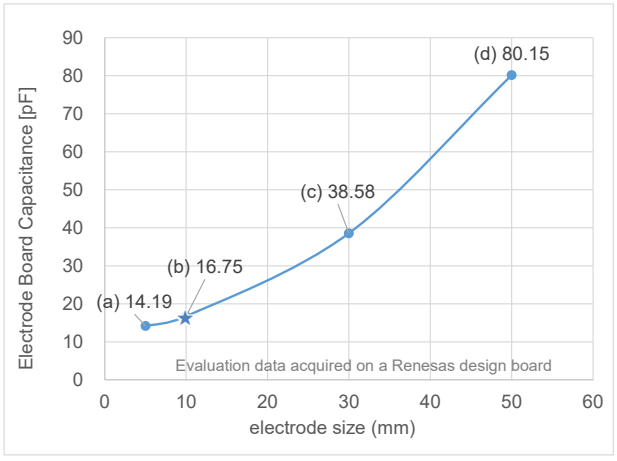


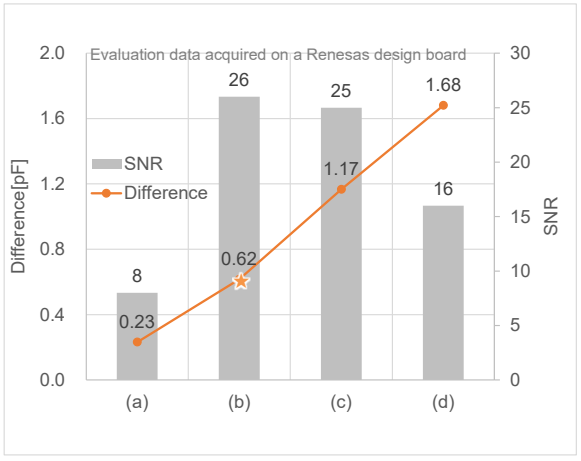
Figure 5-7 Evaluation Board Patterns (electrode sizes)

Figure 5-8 shows Electrode Size and Sensitivity. Parasitic capacitance includes the approximate 10.48 pF parasitic capacitance of the CPU board.

- The parasitic capacitance of the electrode increases in accordance with the area ratio. In actuality, constant amount of parasitic capacitance, such as GND shields and connectors, around the electrode circuit are also added, so the increase in the electrode circuit parasitic capacitance as a whole is smaller than the area ratio.
- CTSU measured capacitance at touch increases in proportion to the electrode size. Parasitic capacitance is generated between the side of the finger and the electrode in addition to the area of the finger that is in direct contact with the electrode.
- SNR at touch decreases as electrode size increases. The sensor drive pulse frequency decreases depending on the total parasitic capacitance of the electrode circuit, which also causes the SNR to decrease.



Parasitic capacitance including CPU board



Detected capacitance difference and SNR

Figure 5-8 Electrode Size and Sensitivity Characteristics

5.4.2 Wiring Length

Table 5-9 lists Board Specifications for Wiring Length Variations, and Table 5-10 lists Combined Shield Conditions. For evaluation purposes, only the wiring length was varied; all other design parameters remained fixed. The effects on sensitivity with different GND patterns are also noted.

Table 5-9 Board Specifications for Wiring Length Variations

Design Parameter	Specification	Unit	Note
Wiring length	**50, 300, 600**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	
GND shield pattern design	Cross-hatched or solid	-	

Note: Recommended design values shown in Table 5-5, except as noted.

Table 5-10 Combined Shield Conditions

Label Name	Cross-hatched pattern	Wiring-Shield Distance	Electrode-Shield Distance
COND1	Cross-hatched/3.0/5.0	3.0mm	5.0mm
COND2	Cross-hatched /0.5/0.5	0.5mm	0.5mm
COND3 Note: GND pattern directly under the electrode is not included.	Solid/0.5/0.5	0.5mm	0.5mm

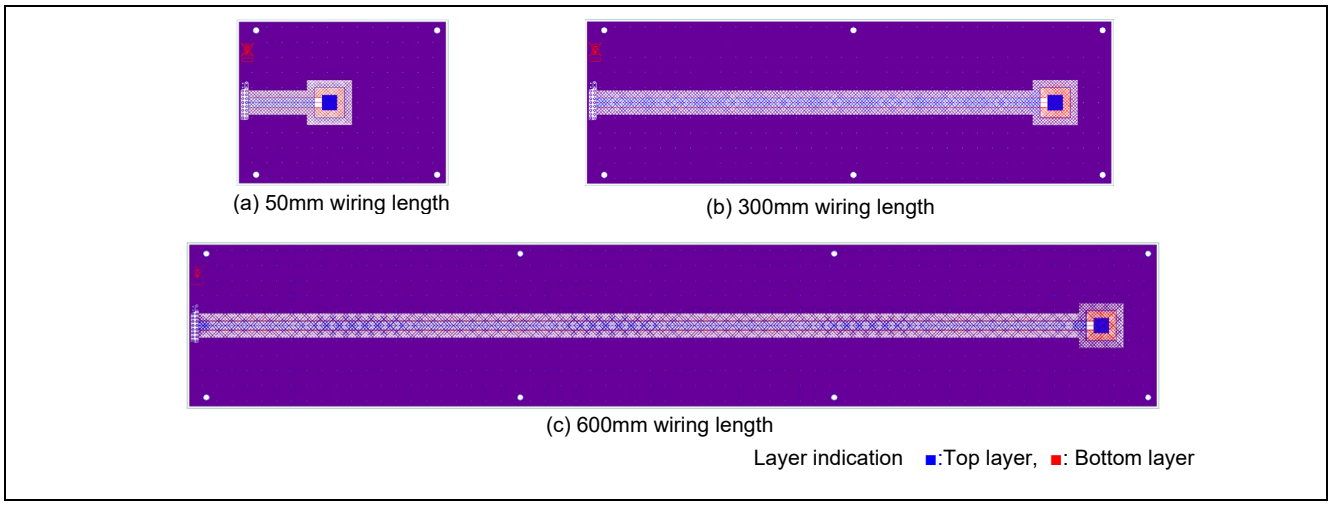


Figure 5-9 Evaluation Board Pattern (COND1)

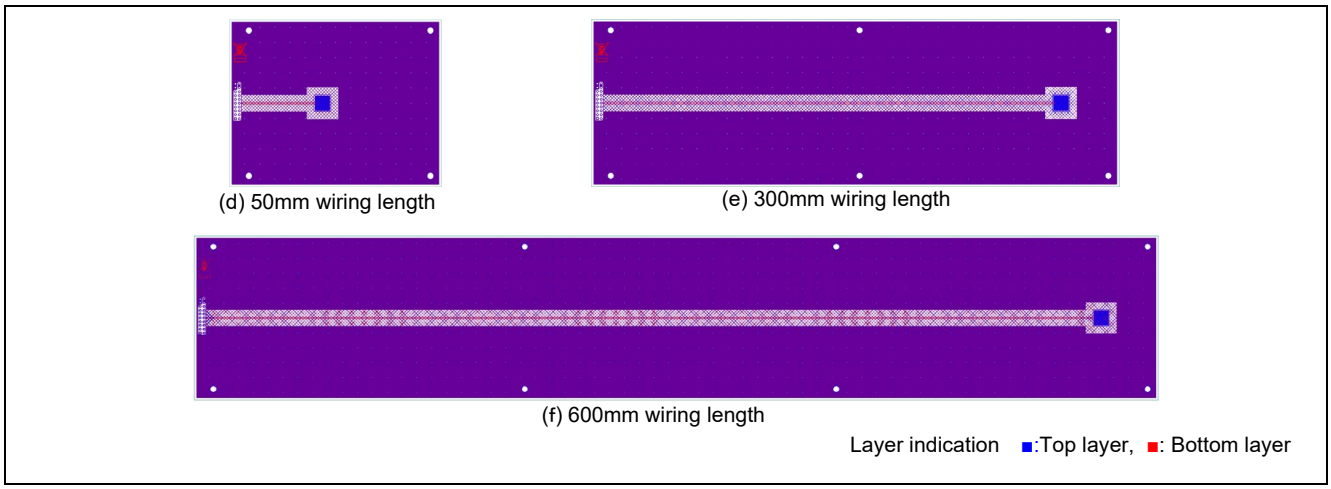


Figure 5-10 Evaluation Board Pattern (COND2)

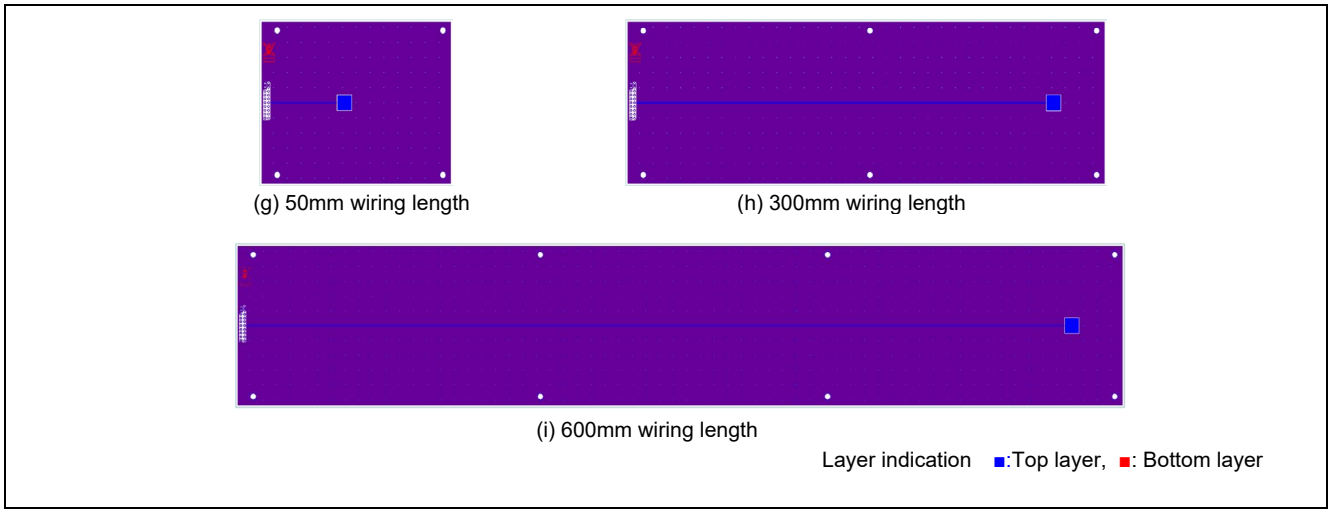


Figure 5-11 Evaluation Board Pattern (COND3)

Figure 5-12 shows Wiring Length and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF. Parasitic capacitance increases in proportion to the wiring length.

- The closer the GND shield is to the electrode and the wiring, the more the parasitic capacitance increases.
- The amount of parasitic capacitance increase at button touch is detected as a constant value regardless of the wiring length.
- The SNR at button touch is lower with longer wiring lengths. As the sensor drive pulse frequency decreases based on the total parasitic capacitance of the electrode circuit, the SNR also decreases.

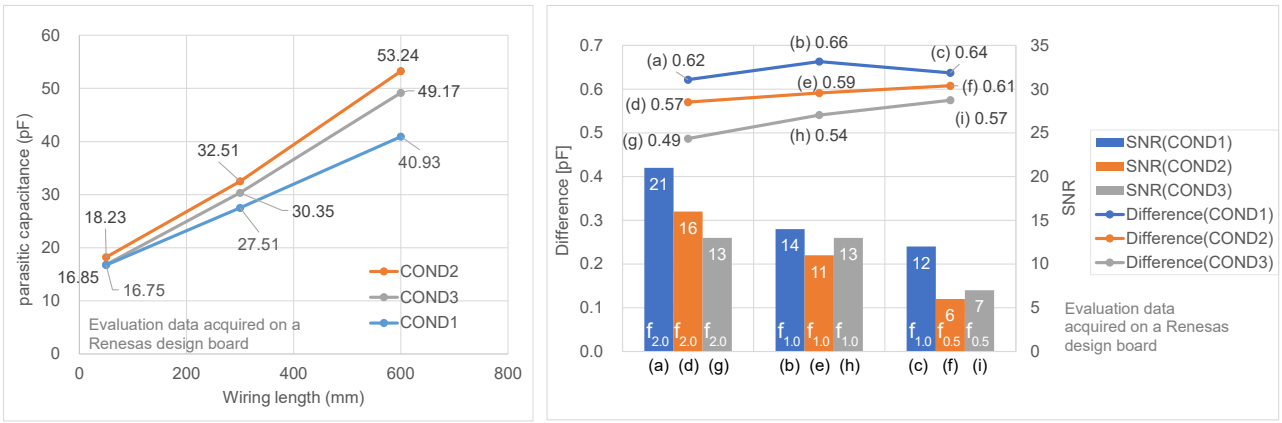


Figure 5-12 Wiring Length and Sensitivity Characteristics

5.4.3 Multiple Button Design

5.4.3.1 Wiring Pitch

Table 5-11 lists the Board Specifications for Wiring Pitch Variations. For evaluation purposes, only the wiring pitch and length was varied; all other design parameters remained fixed.

Table 5-11 Board Specifications for Wiring Pitch Variations

Design Parameter	Specification	Unit	Notes
Wiring pitch	**0.3, 0.5, 1.27, 2.54**	**mm**	
Wiring length	50, 300	mm	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

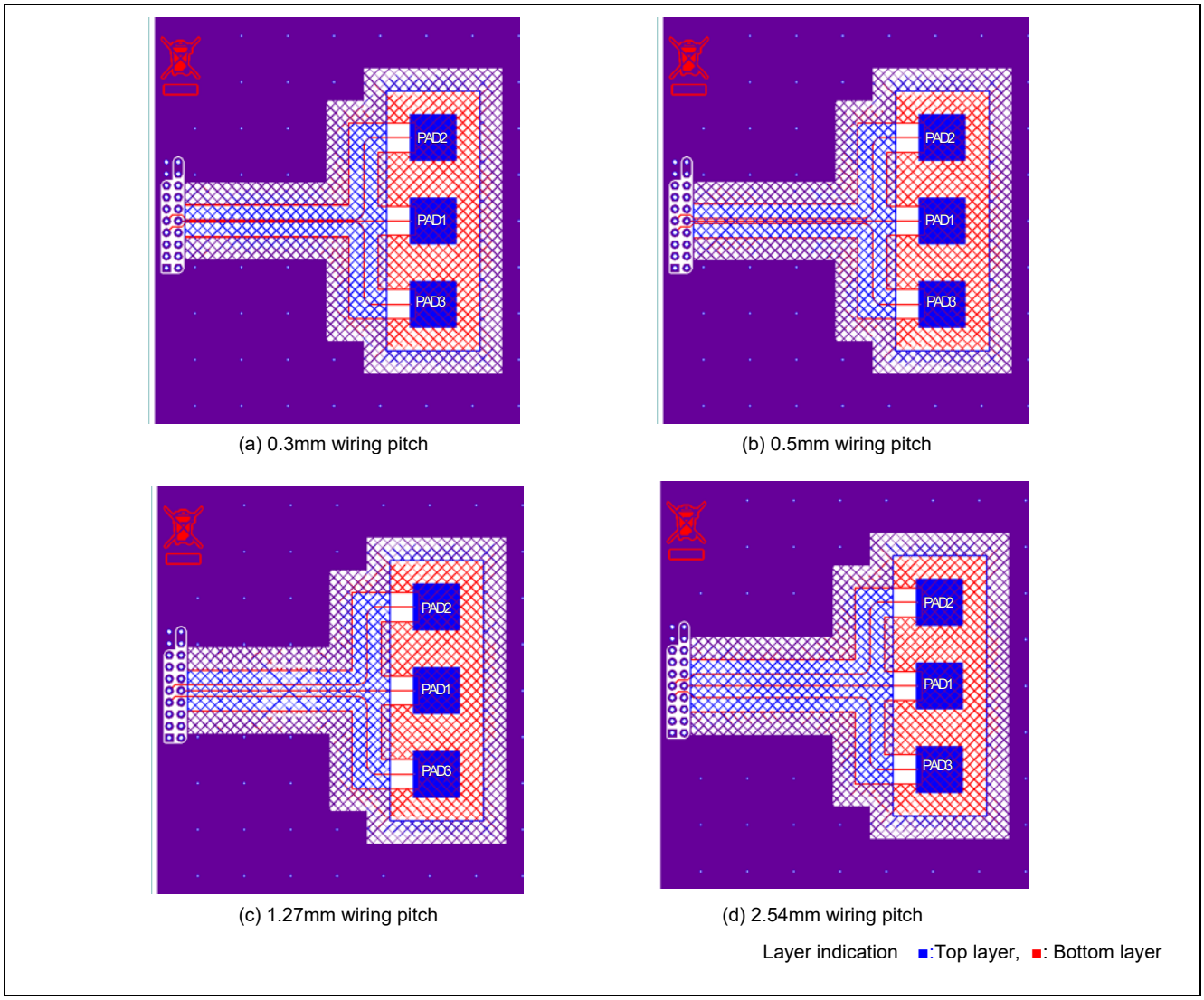
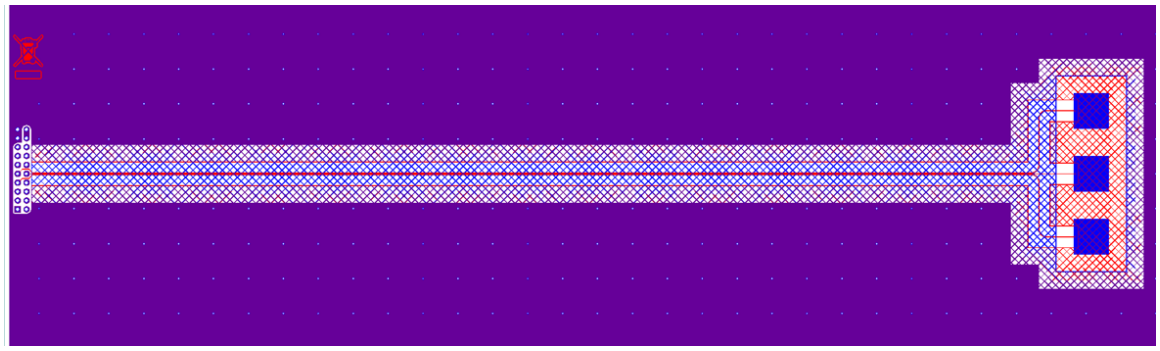
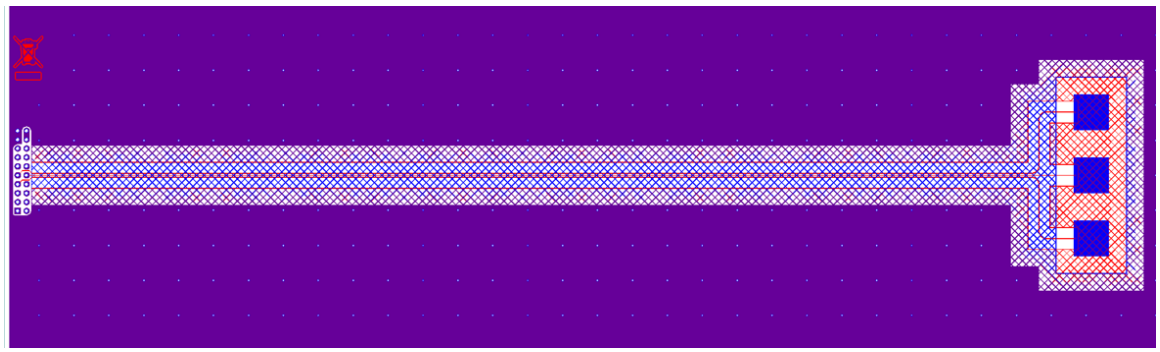


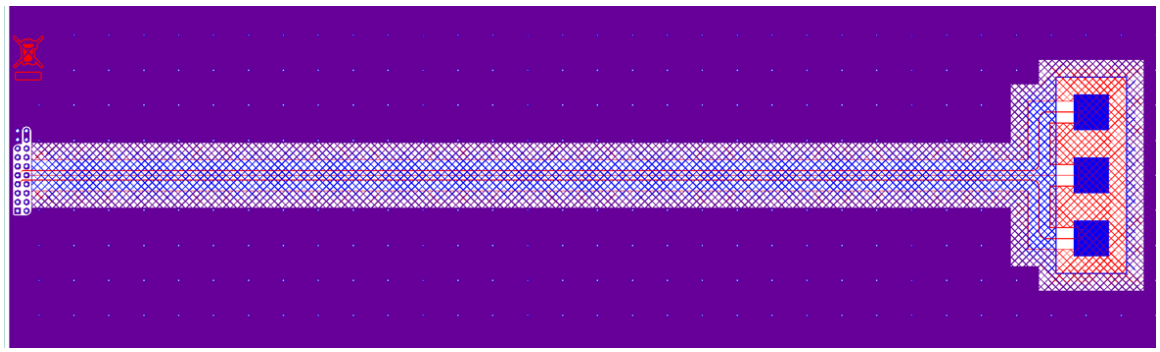
Figure 5-13 Evaluation Board Pattern (wiring length = 50mm)



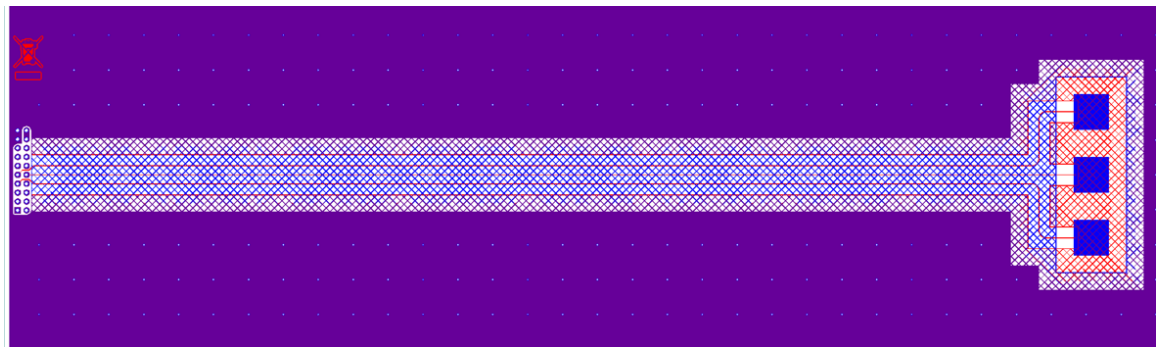
(e) 0.3mm wiring pitch



(f) 0.5mm wiring pitch



(g) 1.27mm wiring pitch



(h) 2.54mm wiring pitch

Layer indication ■:Top layer, ■: Bottom layer

Figure 5-14 Evaluation Board Pattern (wiring length = 300mm)

Figure 5-15 shows Wiring Pitch and Parasitic Capacitance (incl. CPU board) and Figure 5-16 shows Wiring Pitch and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The narrower the wiring pitch, the more the parasitic capacitance increases.
- The amount of parasitic capacitance at button touch is detected as a constant value regardless of the wiring pitch.
- When wiring is on both sides of the electrode, as in PAD1, the SNR at touch is lower because the wiring pitch is narrower. As the sensor drive pulse frequency decreases based on the total parasitic capacitance of the electrode circuit, the SNR also decreases. When wiring is only on one side and it is on the outer side of the wiring group, the SNR is constant regardless of the wiring pitch. The SNR of the wiring on the outer side of the wiring group changes depending on the distance to the GND shield. (SNR (c) is low due to measurement error.)

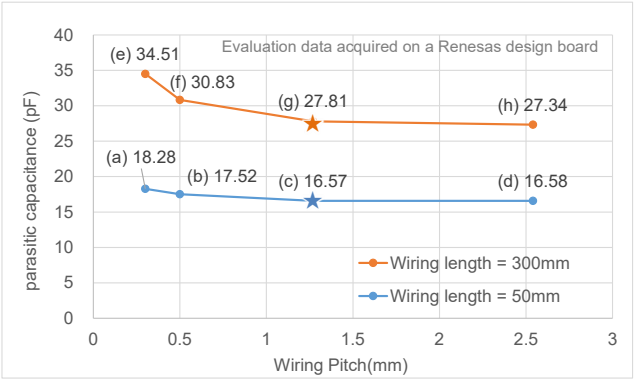
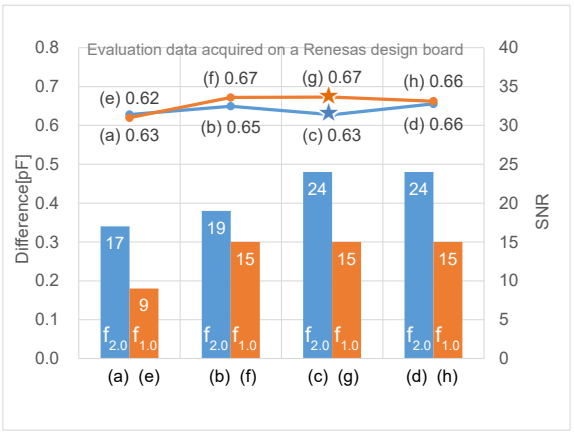
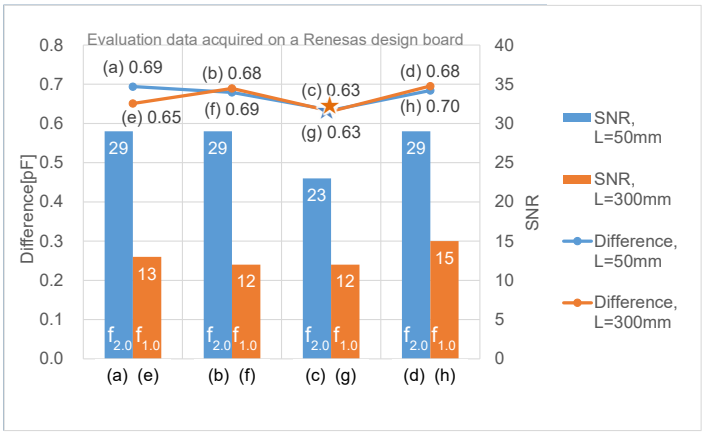


Figure 5-15 Wiring Pitch and Parasitic Capacitance (incl. CPU board)



PAD1 detected capacitance difference and SNR



PAD2 detected capacitance difference and SNR

Figure 5-16 Wiring Pitch and Sensitivity Characteristics

5.4.3.2 Distance between Button Electrodes

The following indicates the sensitivity characteristics based on the distance between button electrodes. For evaluation purposes, only the distance between button electrodes was varied; all other design parameters remained fixed.

Table 5-12 Board Specifications for Variations of Distance Between Button Electrodes

Design Parameter	Specification	Unit	Notes
Distance between button electrodes	**3.0, 8.0, 10.0, 15.0**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

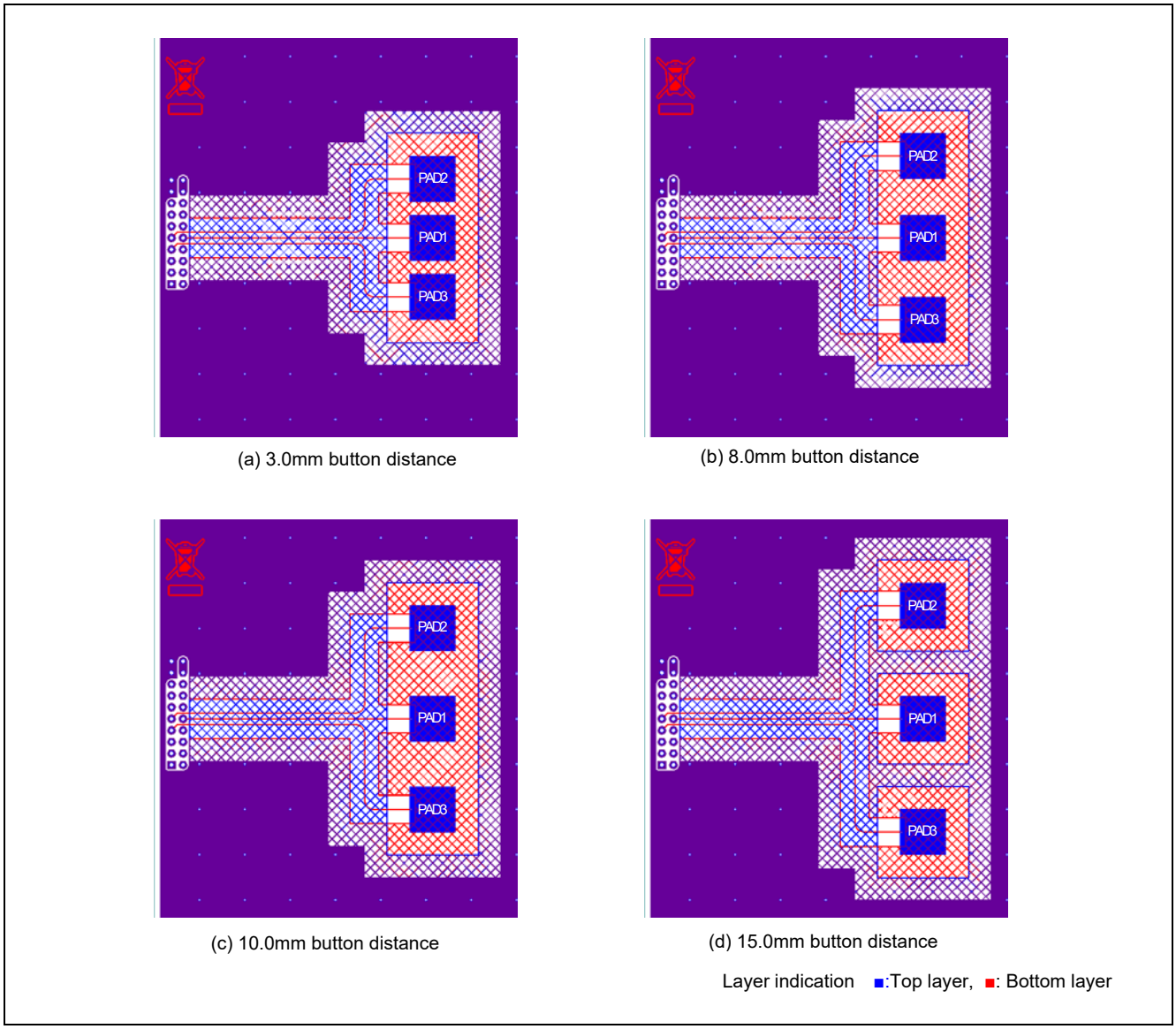
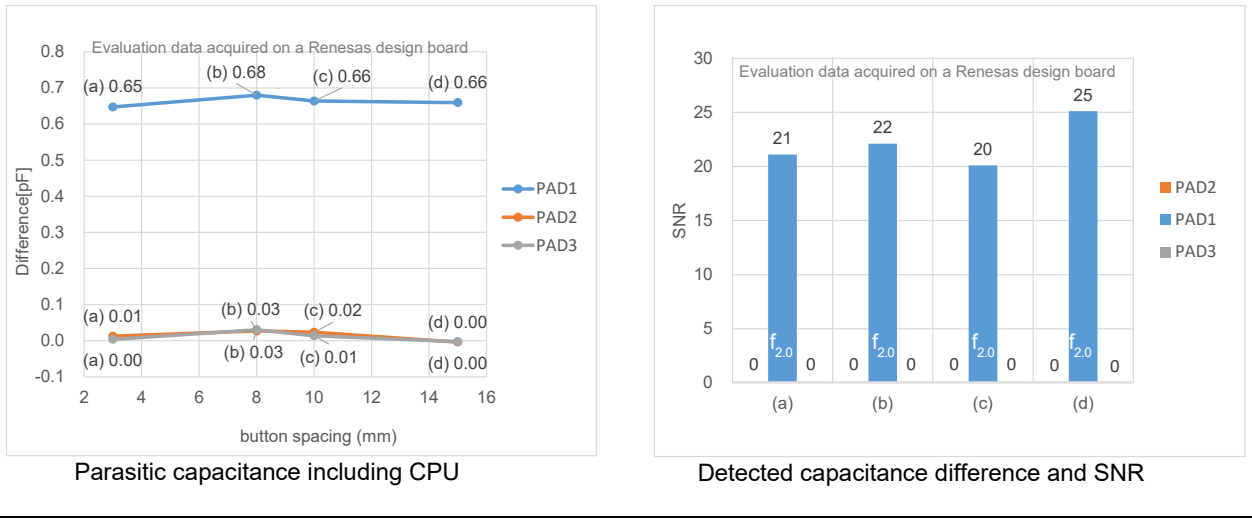


Figure 5-17 Evaluation Board Pattern (distance between button electrodes)

Figure 5-18 shows the Distance Between Button Electrodes and Sensitivity.

- With an overlay thickness of 2.0mm, even a narrow distance between button electrodes of 3.0mm will not cause the SNR of the target button to decrease nor will it cause false detection by neighboring buttons.



Parasitic capacitance including CPU

Detected capacitance difference and SNR

Figure 5-18 Distance Between Button Electrodes and Sensitivity Characteristics

5.4.4 GND Pattern Design

This section focuses on the effect of GND patterns on electrode characteristics. In this document, “shield” refers to a GND pattern that is located on the same layer of the board as the touch electrode and wiring and adjacent to both.

5.4.4.1 Electrode and Shield Distance

Table 5-13 lists Board Specifications for Electrode and Shield Distance Variations. Electrode shield proximity indicates the distance between the electrode and the GND shield. Either a cross-hatched GND pattern or solid GND pattern was used for the shield. For evaluation purposes, only the distance between the electrode and shield, as well as the distance between wiring and shield, were varied; all other design parameters remained fixed.

Table 5-13 Board Specifications for Electrode and Shield Distance Variations

Design Parameter	Specification	Unit	Notes
Shield type	**Hatched GND or solid GND**	**-**	
Distance between electrode and shield	**0.5, 1.0, 3.0, 5.0**	**mm**	
Distance between wiring and shield	3.0	mm	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

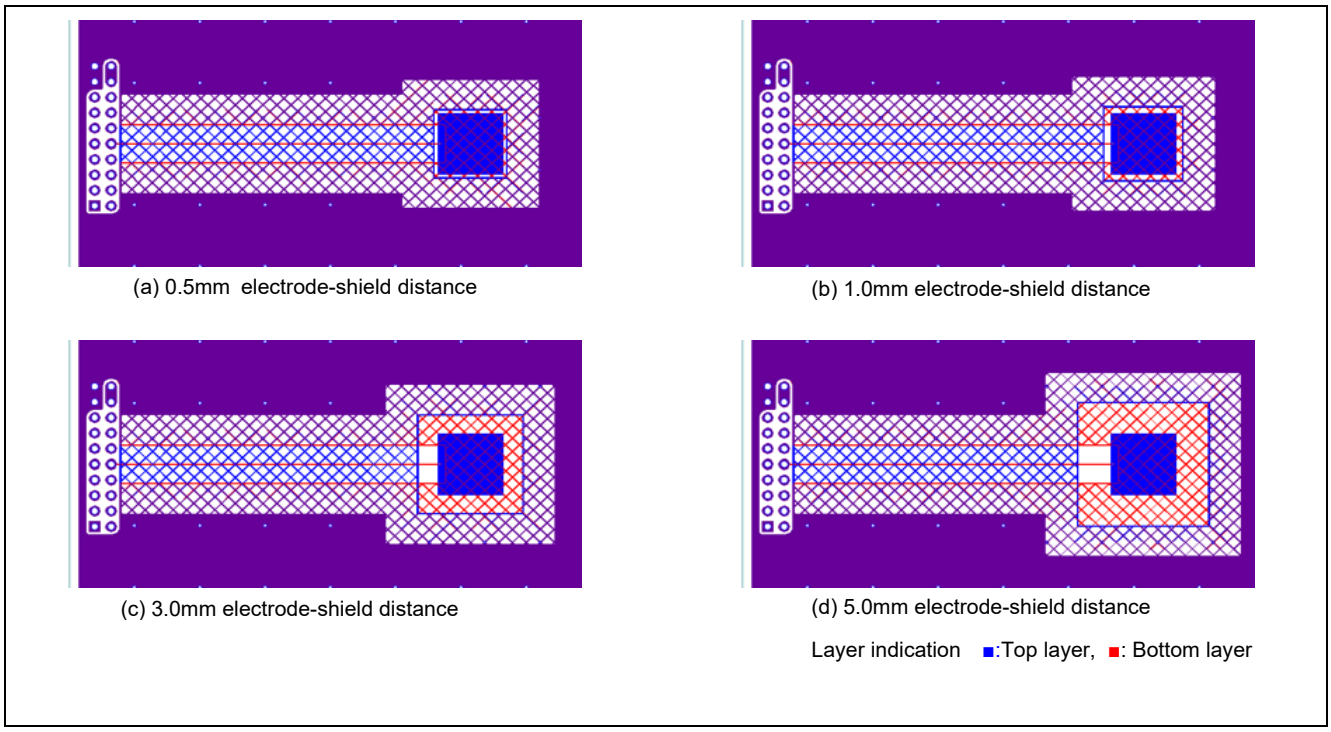


Figure 5-19 Evaluation Board Pattern (cross-hatched GND, only electrode-shield distance varied)

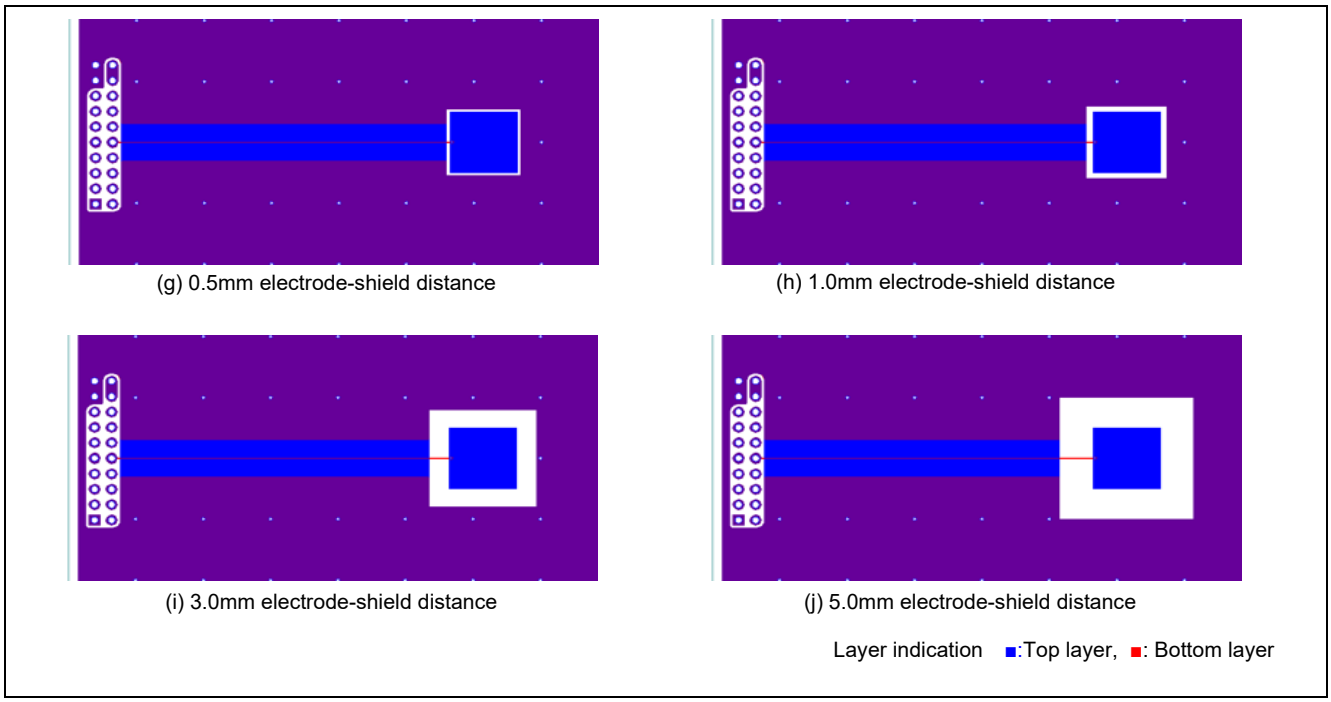


Figure 5-20 Evaluation Board Pattern (only solid GND and electrode-shield distance varied)

Figure 5-21 lists Electrode-Shield Distance and Sensitivity . Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF. Note that the parasitic capacitance of boards using a solid GND shield pattern is smaller than those using a cross-hatched GND pattern due to the lack of solid GND pattern directly under the electrode.

- The shorter the distance between the electrode and the GND shield, the more the parasitic capacitance increases. Cross-hatched GND shields generate a smaller increase in parasitic capacitance than do solid GND shields, even with a shorter distance.
- The shorter the distance between the electrode and the GND shield, the smaller the detected capacitance difference.
- The shorter the distance between the electrode and the GND shield, the more the SNR tends to decrease. In the graphs below, (c) and (e) show larger values due to measurement error.

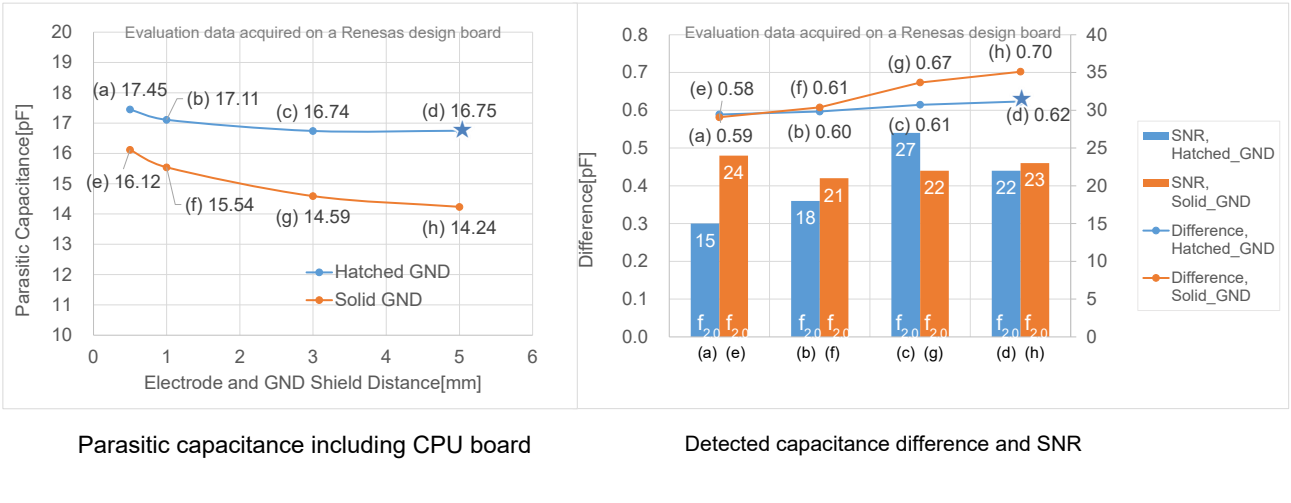


Figure 5-21 Electrode-Shield Distance and Sensitivity Characteristics

5.4.4.2 Distance between Wiring and Shield

Table 5-14 lists Board Specifications for Wiring-Shield Distance Variations. The wiring-shield distance indicates the distance between the wiring and the GND shield. Either a cross-hatched GND pattern or solid GND pattern was used for the shield. For evaluation purposes, only the distance between wiring and shield was varied; all other design parameters remained fixed.

Table 5-14 Board Specifications for Wiring-Shield Distance Variations

Design Parameter	Specification	Unit	Notes
Shield type	**Cross-hatched GND, solid GND**	**-**	
Distance between wiring and shield	**0.5, 1.0, 3.0, 5.0**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

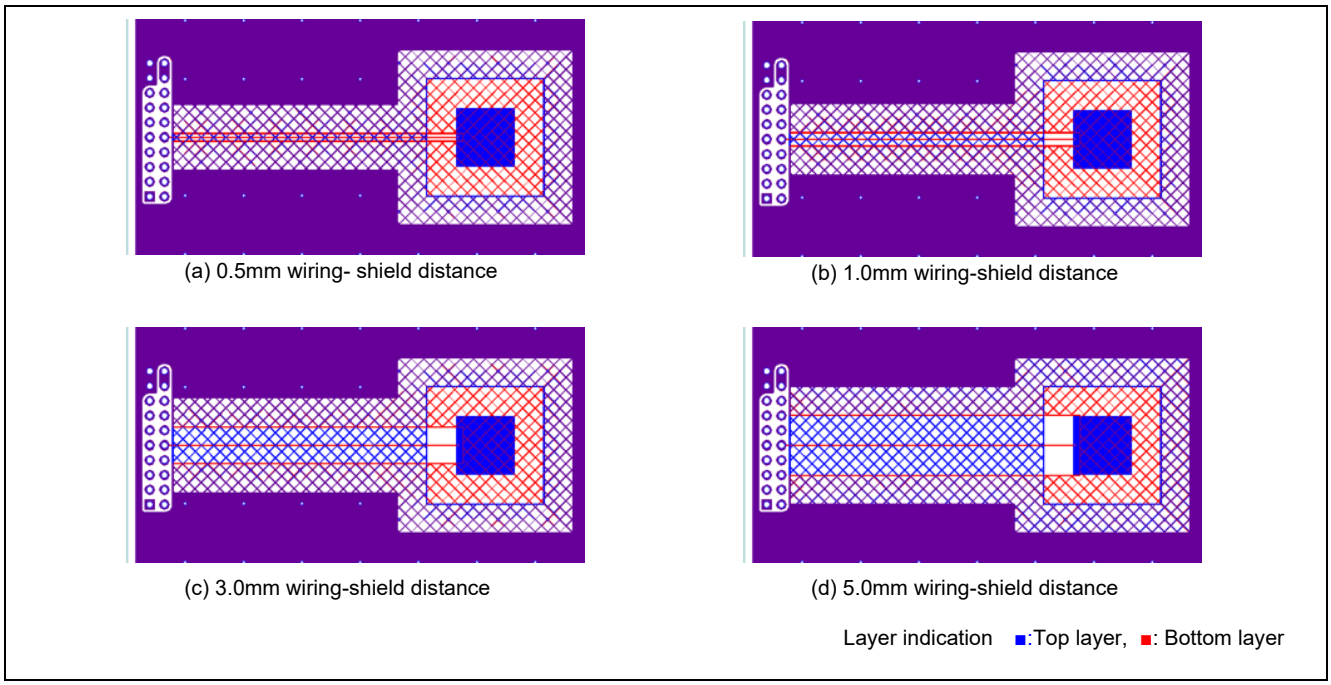


Figure 5-22 Evaluation Board Pattern (cross-hatched GND)

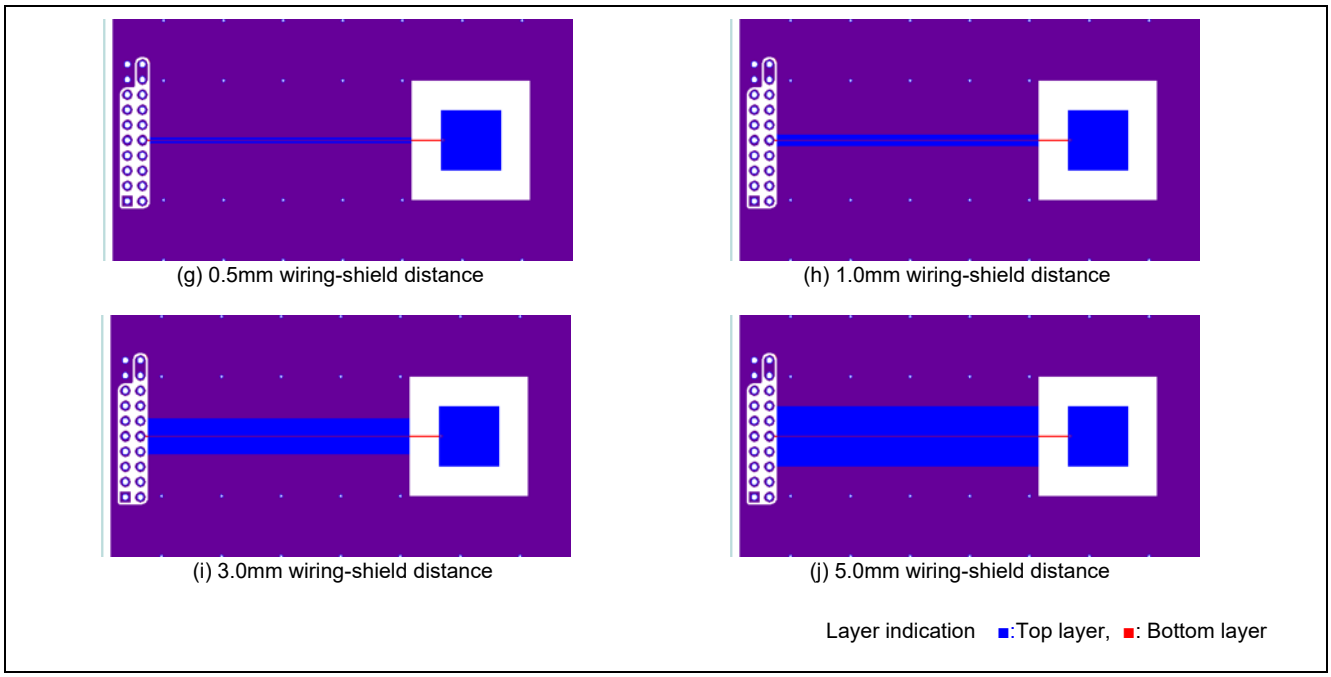
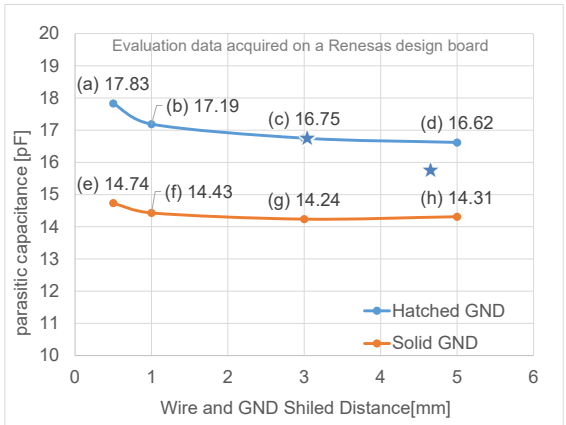


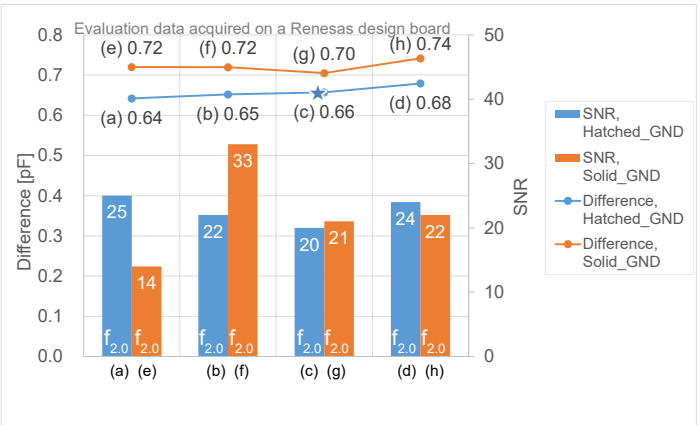
Figure 5-23 Evaluation Board Pattern (solid GND)

Figure 5-24 shows Wiring-Shield Distance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF. Note that the parasitic capacitance of boards using a solid GND shield pattern is smaller than those using a cross-hatched GND pattern due to the lack of solid GND pattern directly under the electrode.

- The shorter the distance between the wiring and the GND shield, the more the parasitic capacitance increases.
- The shorter the distance between the wiring and the GND shield, the smaller the detected capacitance difference.
- The shorter the distance between the wiring and the GND shield, the more the SNR tends to decrease. In the graphs below, (h) shows a larger value due to measurement error.



Parasitic capacitance including CPU board



Detected capacitance difference and SNR

Figure 5-24 Wiring-Shield Distance and Sensitivity Characteristics

5.4.4.3 Effect of Inner Layer GND

Table 5-15 lists Board Specifications With/Without Inner Layer GND. For evaluation purposes, only the inner shield hierarchy on the multi-layered board was varied; all other design parameters remained fixed. The effect on sensitivity due to different shield types is also included. Note that use of a solid patten requires removing the pattern directly under the electrode.

Table 5-15 Board Specifications With/Without Inner Layer GND

Design Parameter	Specification	Unit	Notes
Inner shield layers	**L2, L3, none**	**-**	**L4 can be applied under all conditions**
Shield type	**Cross-hatched GND, solid GND**	**-**	**Solid GND does not include a pattern directly under the electrode**
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

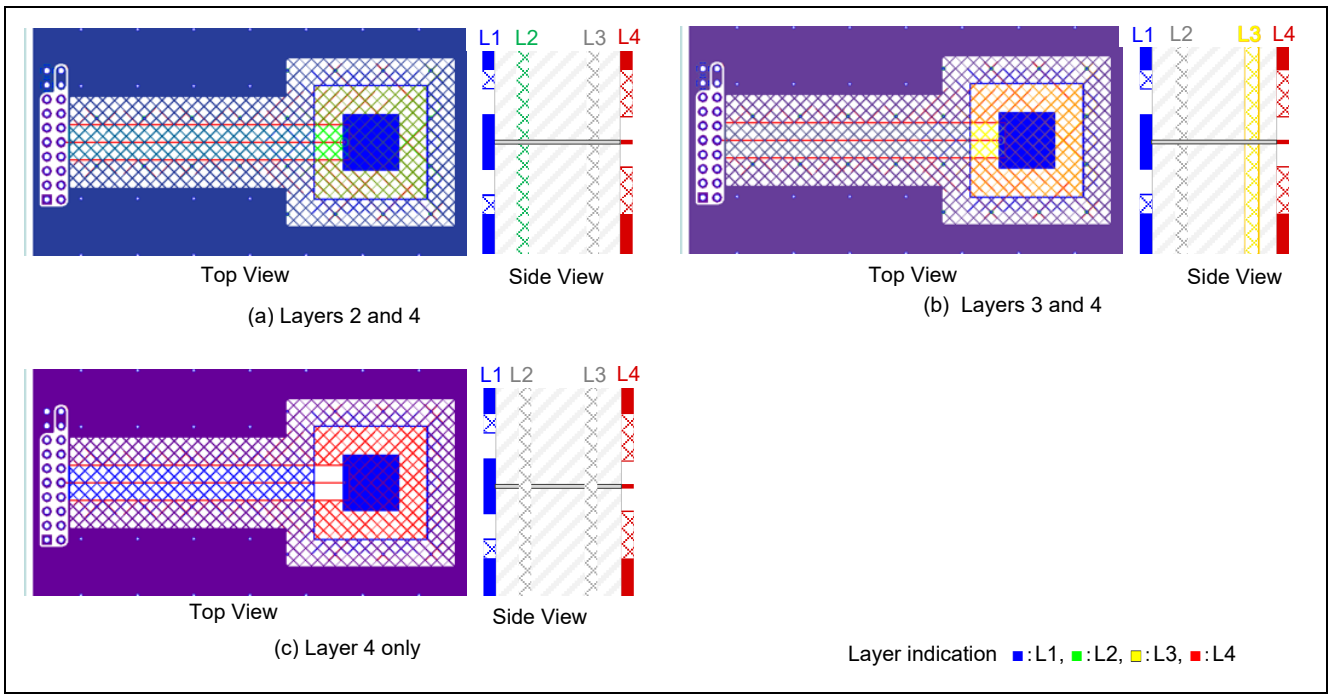


Figure 5-25 Evaluation Board Pattern (cross-hatched GND)

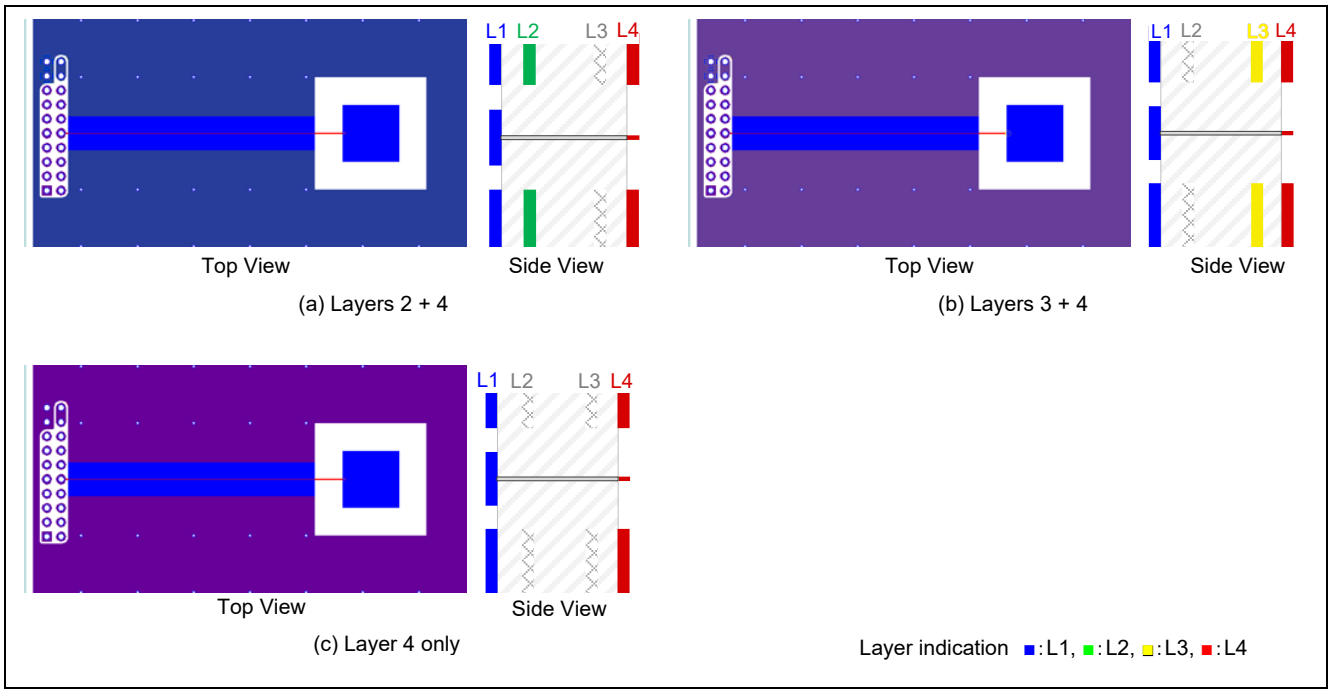
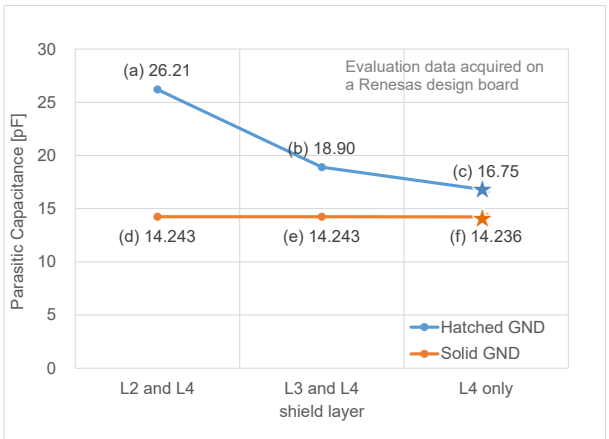


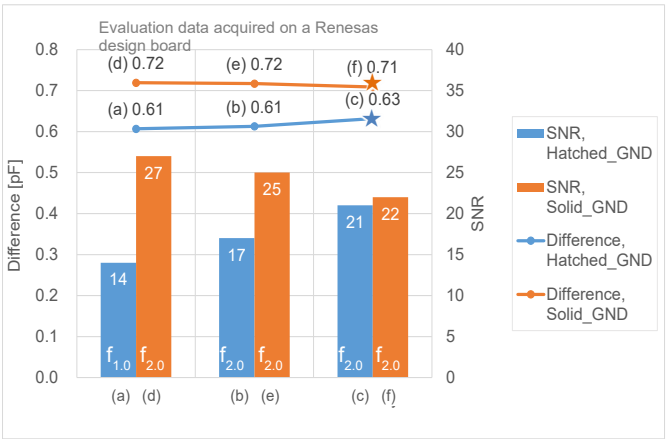
Figure 5-26 Evaluation Board Pattern (solid GND)

Figure 5-27 shows Inner Layer GND and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- When a shield is placed directly under the electrode, the closer the inner layer GND and the electrode are, the more the parasitic capacitance increases. Take caution as parasitic capacitance will increase even when a cross-hatched pattern is placed directly beneath the electrode. There is no increase in parasitic capacitance with a solid pattern because the pattern directly below the electrode is removed.
- The detected capacitance difference is constant, regardless of the shield level.
- The closer the inner layer GND is to the electrode, the lower the SNR. Placing the GND shield on an inner layer increases the total parasitic capacitance and lowers the sensor drive pulse frequency, which tends to lower the SNR.



Parasitic capacitance including CPU board



Detected capacitance difference and SNR

Figure 5-27 Inner Layer GND and Sensitivity Characteristics

5.4.4.4 Cross-hatched Shield Pattern Width

Table 5-16 lists Board Specifications for Cross-hatched Shield Pattern Width Variations. For evaluation purposes, only the cross-hatched shield pattern width and the distance between the cross-hatched shield and electrodes/wiring were varied; all other design parameters remained fixed.

Table 5-16 Board Specifications for Cross-hatched Shield Pattern Width Variations

Design Parameter	Specification	Unit	Notes
Cross-hatched shield pattern width (electrode periphery and wiring periphery)	**1.0, 3.0, 5.0, 10.0**	**mm**	
Distance between electrode and shield	**0.5, 1.0, 5.0**	**mm**	
Distance between wiring and shield	**0.5, 1.0, 3.0**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	
Combined shield conditions (wiring-shield distance/ electrode-shield distance)			
COND1	3.0/5.0	mm	Recommended design values
COND2	1.0/1.0	mm	
COND3	0.5/0.5	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

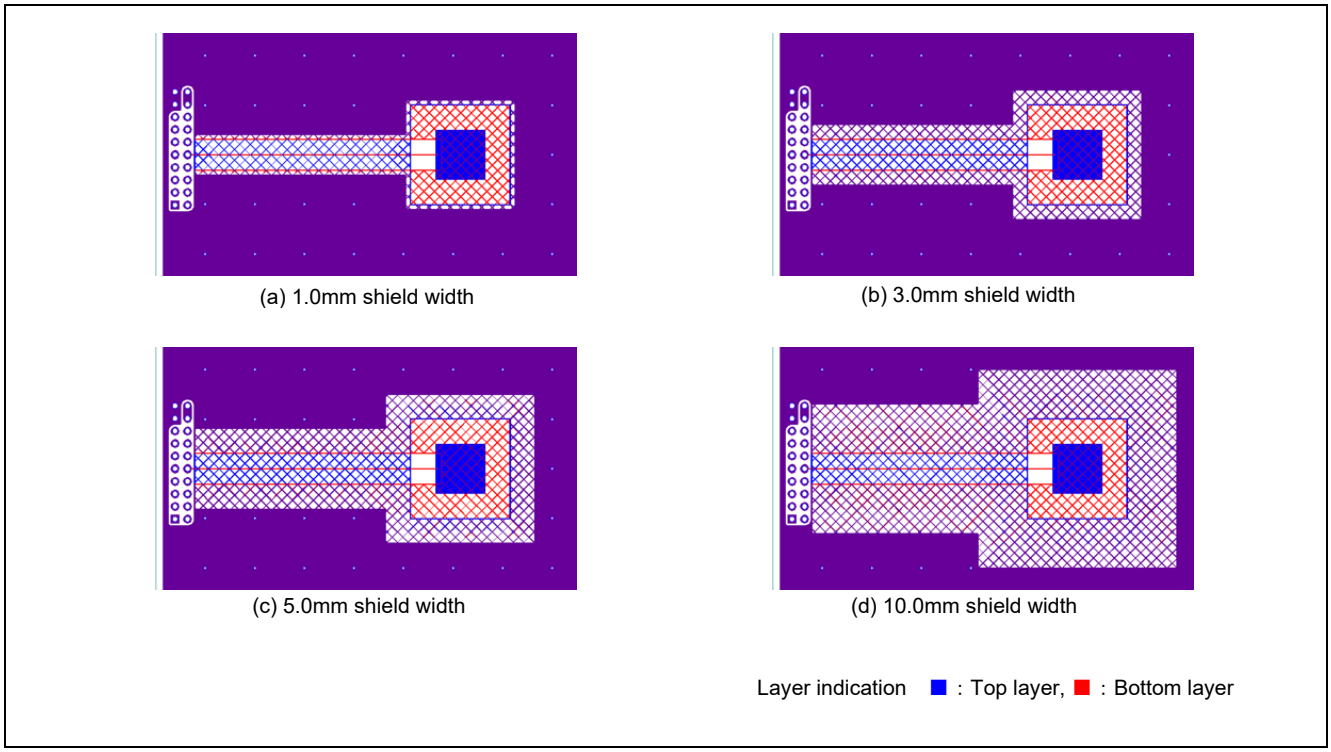
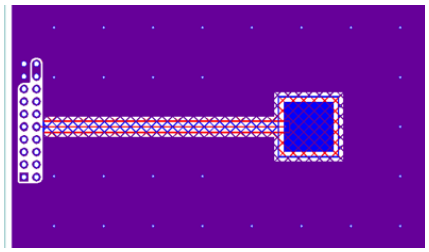
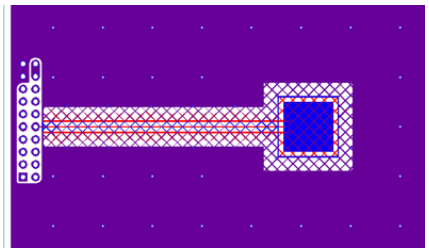


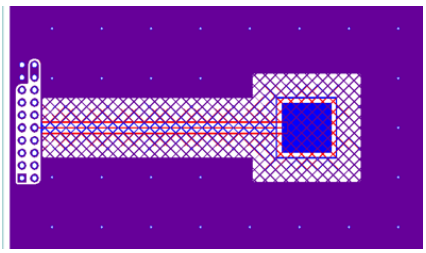
Figure 5-28 Evaluation Board Pattern (Distance between electrode/wiring and cross-hatched shield = recommended value)



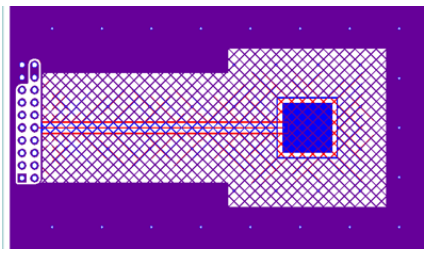
(e) 1.0mm shield width



(f) 3.0mm shield width



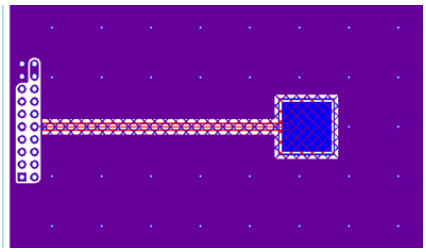
(g) 5.0mm shield width



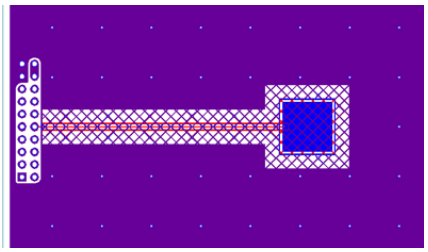
(h) 10.0mm shield width

Layer indication ■ : Top layer, ■ : Bottom layer

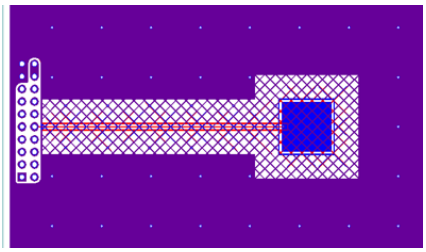
Figure 5-29 Evaluation Board Pattern (Distance between electrode/wiring and cross-hatched shield = 1.0mm)



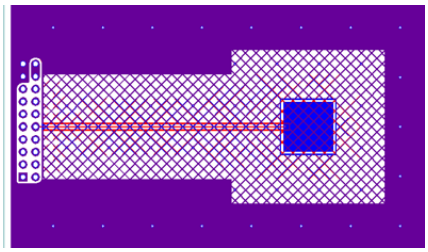
(i) 1.0mm shield width



(j)3.0 mm shield width



(k) 5.0mm shield width h



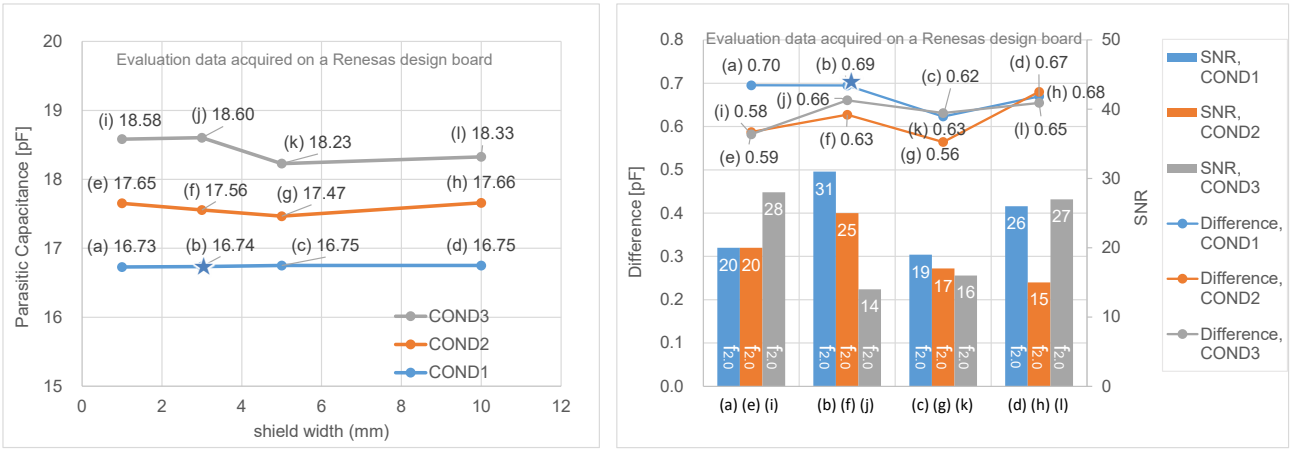
(l)10.0 mm shield width

Layer indication ■ : Top layer, ■ : Bottom layer

Figure 5-30 Evaluation Board Pattern (Distance between electrode/wiring and cross-hatched shield = 0.5mm)

Figure 5-31 shows Cross-hatched Shield Width and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- COND1 (recommended design): Parasitic capacitance is constant regardless of the cross-hatched GND pattern width. Although a solid GND is placed on around the cross-hatched shield, it should have no effect if there is sufficient distance between the shield and the electrode and wiring. In COND2 and COND3, as the cross-hatched shield width is narrowed, the distance between the solid GND and the electrode and wiring decreases, causing the parasitic capacitance to increase.



Parasitic capacitance including CPU board

Detected capacitance difference and SNR

Figure 5-31 Cross-hatched Shield Width and Sensitivity Characteristics

5.4.4.5 Cross-hatched Shield Pattern Aperture Ratio

Table 5-17 lists Board Specifications for Cross-hatched Pattern Aperture Ratio. For evaluation purposes, only the inner shield hierarchy and the shield type on the multi-layered board was varied; all other design parameters remained fixed.

Table 5-17 Board Specifications for Cross-hatched Pattern Aperture Ratio Variations

Design Parameter	Specification	Unit	Notes
Shield aperture ratio	**30、81、90**	**%**	
Inner Shield layers	**Only the bottom layer (layer 4), layer 3 and 4**	**-**	
Shield type	Cross-hatched **GND**	**-**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

Figure 5-32 shows the Cross-hatched Pattern Dimensions.

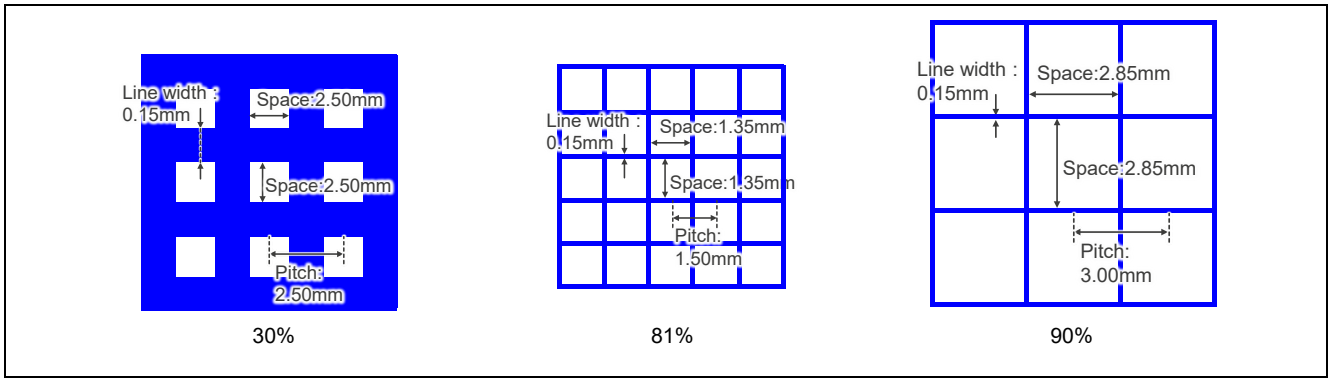


Figure 5-32 Cross-hatched Pattern Dimensions

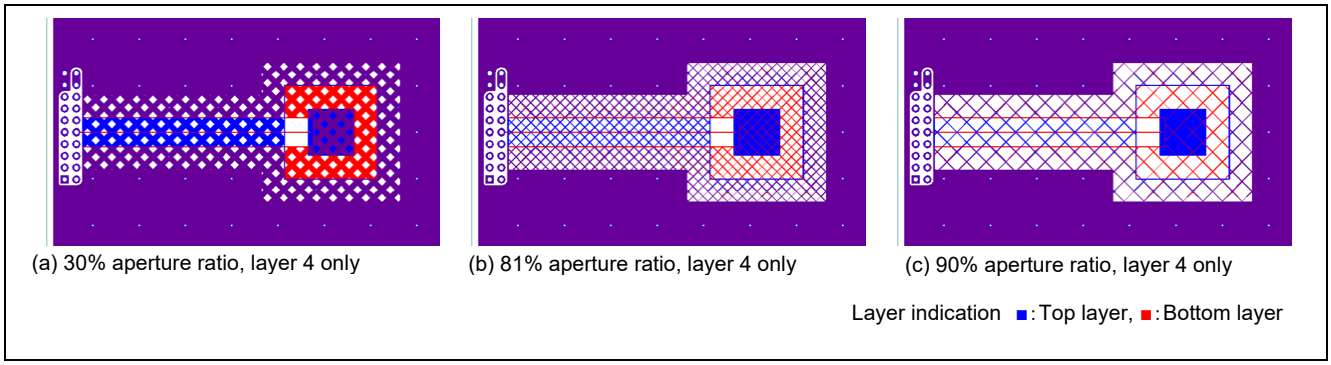


Figure 5-33 Evaluation Board Patterns (double-sided board, GND shield)

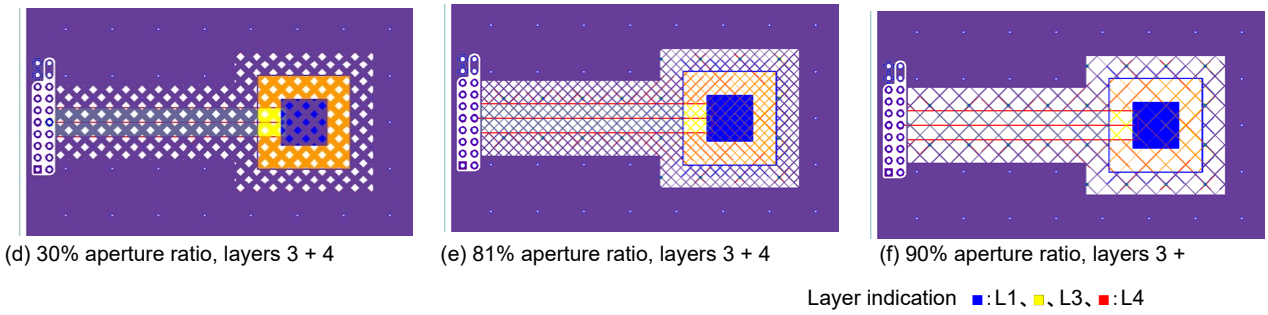
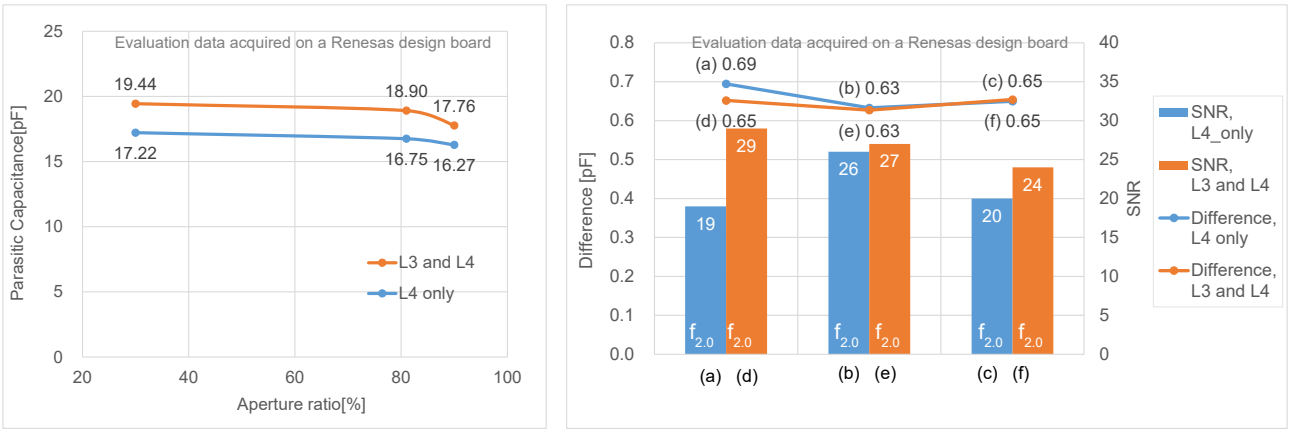


Figure 5-34 Evaluation Board Patterns (4-layered board, GND shield)

Figure 5-35 shows Cross-hatched Shield Aperture Ratio and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The smaller the cross-hatched GND aperture ratio, the larger the facing area opposite the electrode, which cause the parasitic capacitance to increase. In addition, when a GND shield layer is added to an inner layer, the facing distance decreases, causing the parasitic capacitance to increase proportionately.
- The detected capacitance difference at touch is constant, regardless of the aperture ratio.



Parasitic capacitance including CPU board

Detected capacitance difference and SNR

Figure 5-35 Cross-hatched Shield Aperture Ratio and Sensitivity Characteristics

5.4.5 Active Shield Design

5.4.5.1 Active Shield Area

Table 5-18 lists Table 5-18Board Specifications for Active Shield Electrode Capacitance Confirmation According to Number of Buttons. For evaluation purposes, only the number of button electrodes was varied; all other design parameters remained fixed.

Table 5-18 Board Specifications for Active Shield Electrode Capacitance Confirmation According to Number of Buttons

Design Parameter	Specification	Unit	Notes
Number of button electrodes	**1, 3, 5**	**electrode**	
Shield type	Active shield	-	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

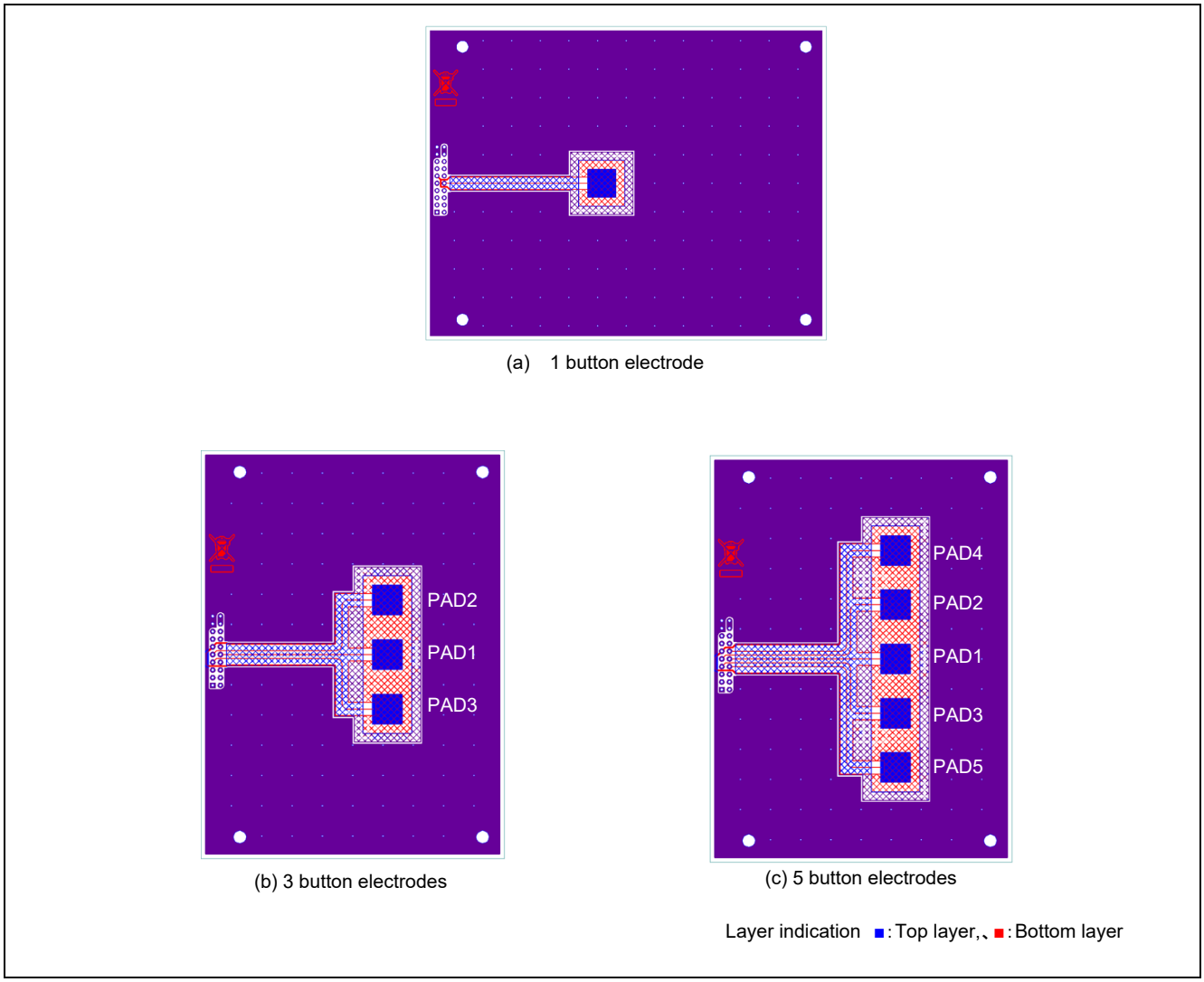


Figure 5-36 Evaluation Board Pattern (active shield electrode capacitance confirmation board)

Figure 5-37 shows Active Shield Capacitance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The evaluation board equipped with an active shield has less parasitic capacitance than the evaluation board with a cross-hatched GND shield, and the parasitic capacitance is mainly detected in the area of the CPU board. The CPU board remains as parasitic capacitance because it does not have an active shield.
- The parasitic capacitance of button PAD1 decreases in proportion to the total number of buttons. This improvement is due to the parasitic capacitance reduction effect of the active shield as well as the increased shield area, which increases the distance between the button and the peripheral solid GND.
- Since the active shield area increases as the number of button is increased, the parasitic capacitance from the active shield pin also increases.
- On the board used in this evaluation, the parasitic capacitance of the active shield tends to be larger than that of the button itself. The automatic adjustment function of QE for Capacitive Touch selects the drive pulse frequency to match the pin with the largest parasitic capacitance from the button or active shield configuration (method). When designing your application, keep in mind that the parasitic capacitance of the active shield pin may go over 50pF, depending on the number and size of buttons.
-

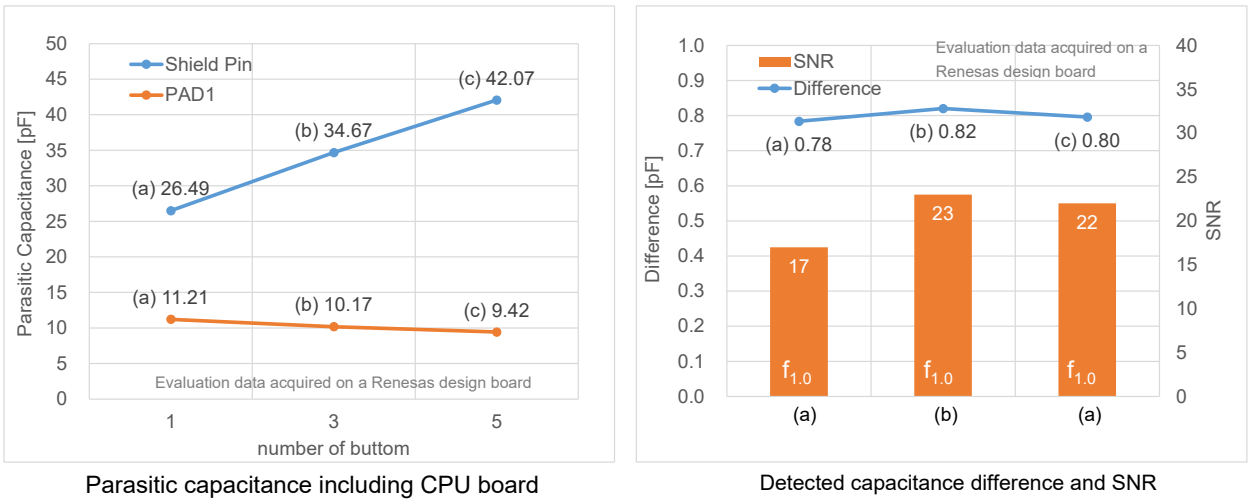


Figure 5-37 Active Shield Capacitance and Sensitivity Characteristics

5.4.5.2 Distance Between Electrode and Active Shield

Table 5-19 lists Board Specifications for Electrode-Active Shield Distance Variations. For evaluation purposes, only the distance between the electrode and the active shield was varied; all other design parameters remained fixed.

Table 5-19 Board Specifications for Electrode-Active Shield Distance Variations

Design Parameter	Specification	Unit	Notes
Distance between electrode and active shield	**0.5, 1.0, 3.0, 5.0**	**mm**	
Distance between wiring and active shield	**0.5, 3.0, 5.0**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

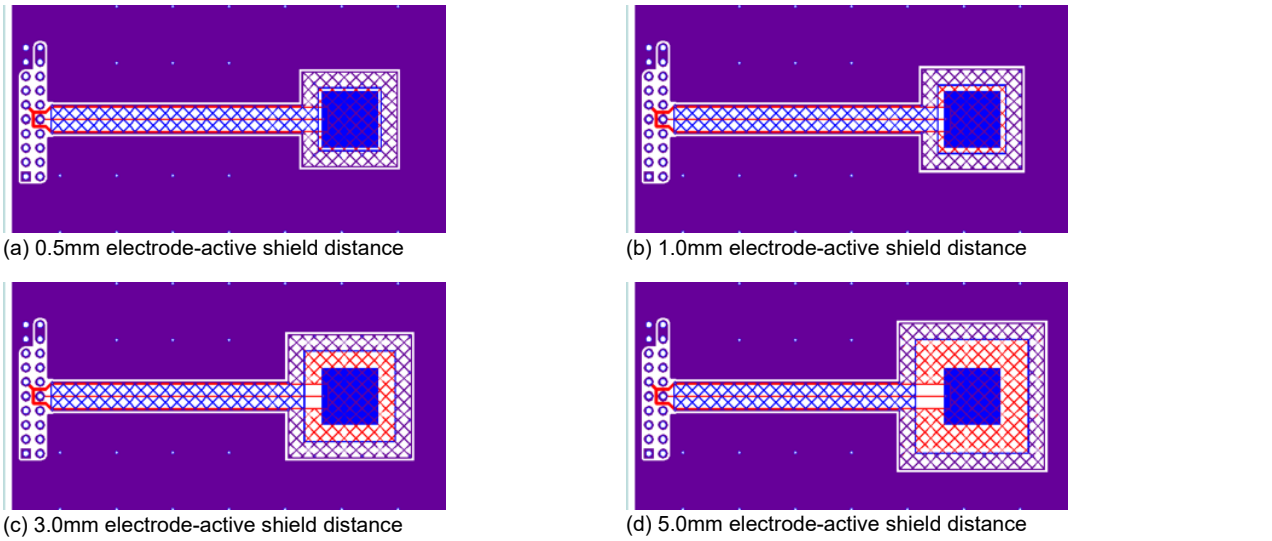
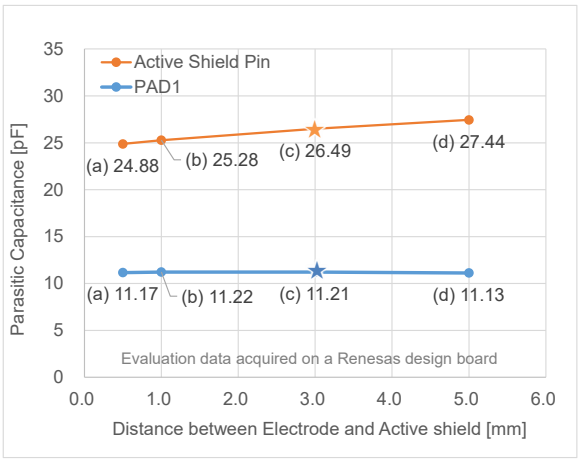


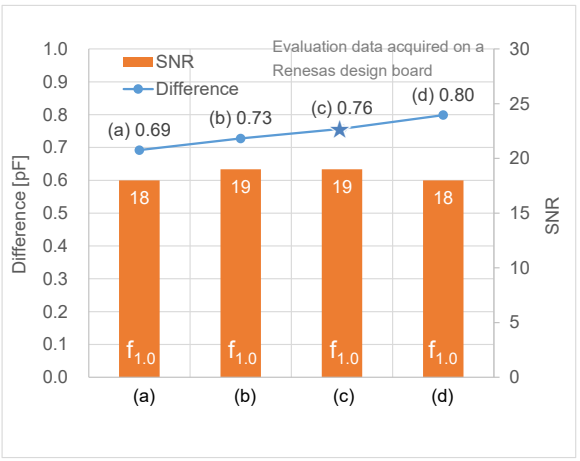
Figure 5-38 Evaluation Board Pattern

Figure 5-39 shows Electrode-Active Shield Distance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The parasitic capacitance of the button electrode is constant regardless of the distance between the electrode and the active shield. The parasitic capacitance of the active shield pin is dependent on the area of the shield.
- The SNR does not fluctuate due to the distance between the electrode and the active shield. Because the active shield reduces the effect of the distance between solid GND pattern on the outer periphery and the electrodes, the capacitance detection difference improves in proportion to the distance between the electrode and active shield.



Parasitic capacitance including CPU board



Detected capacitance difference and SNR

Figure 5-39 Electrode-Active Shield Distance and Sensitivity Characteristics

5.4.5.3 Distance between Wiring and Active Shield

Table 5-20 lists Board Specifications for Wiring-Active Shield Distance Variations. For evaluation purposes, only the distance between the wiring and active shield was varied; all other design parameters remained fixed.

Table 5-20 Board Specifications for Wiring-Active Shield Distance Variations

Design Parameter	Specification	Unit	Notes
Difference between wiring and active shield	**0.5, 1.0, 3.0, 5.0**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

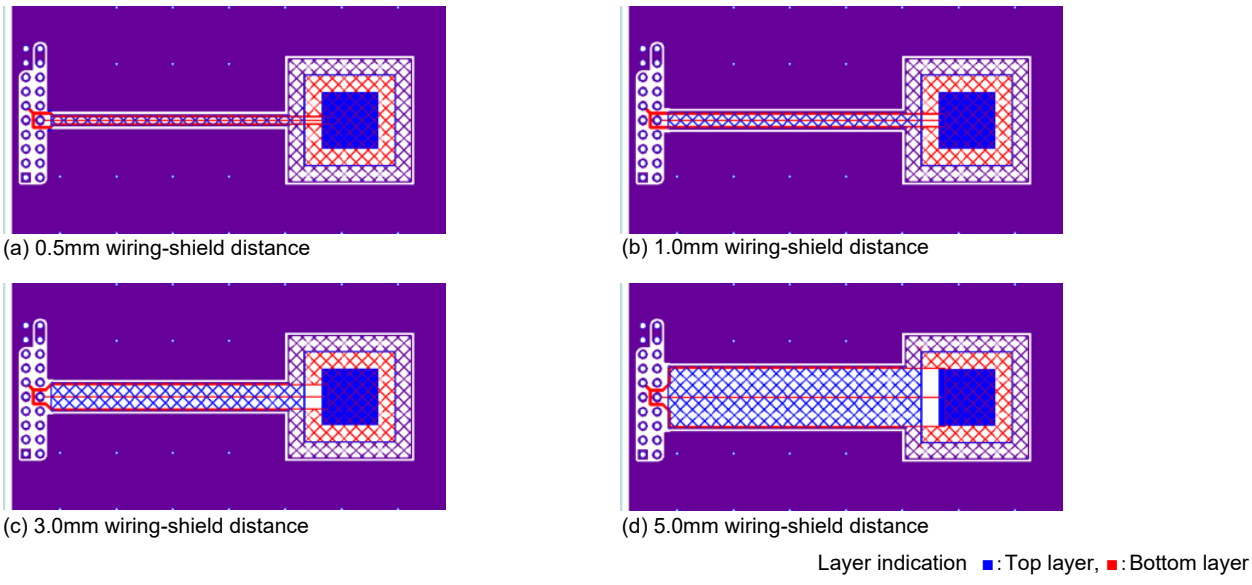
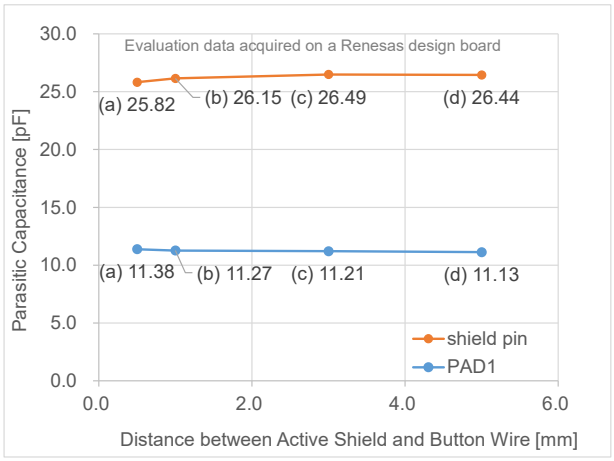


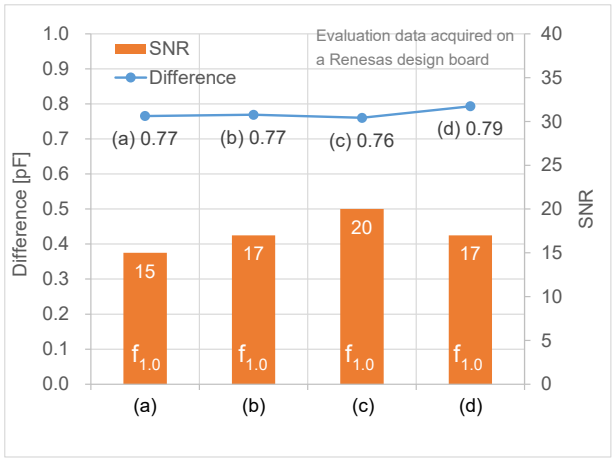
Figure 5-40 Evaluation Board Pattern (wiring-active shield distance)

Figure 5-41 shows Wiring-Active Shield Distance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The parasitic capacitance of the button electrode is constant regardless of the distance between the wiring and the active shield. The parasitic capacitance of the active shield pin is dependent on the area of the shield.
- The SNR does not fluctuate due to the distance between the wiring and the active shield. The capacitance detection value is constant, and the capacitance detection difference is not affected by the distance between the wiring and the active shield.



Parasitic capacitance including CPU board



Detected capacitance difference and SNR

Figure 5-41 Wiring-Active Shield Distance and Sensitivity Characteristics

5.4.5.4 Distance Between Active Shield and Solid GND

Table 5-21 lists Board Specifications for Active Shield-Solid GND Distance Variations. For evaluation purposes, only the distance between the active shield and the solid GND was varied; all other design parameters remained fixed.

Table 5-21 Board Specifications for Active Shield-Solid GND Distance Variations

Design Parameter	Specification	Unit	Notes
Distance between active shield and solid GND	**0.5、1.0、5.0、10.0**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

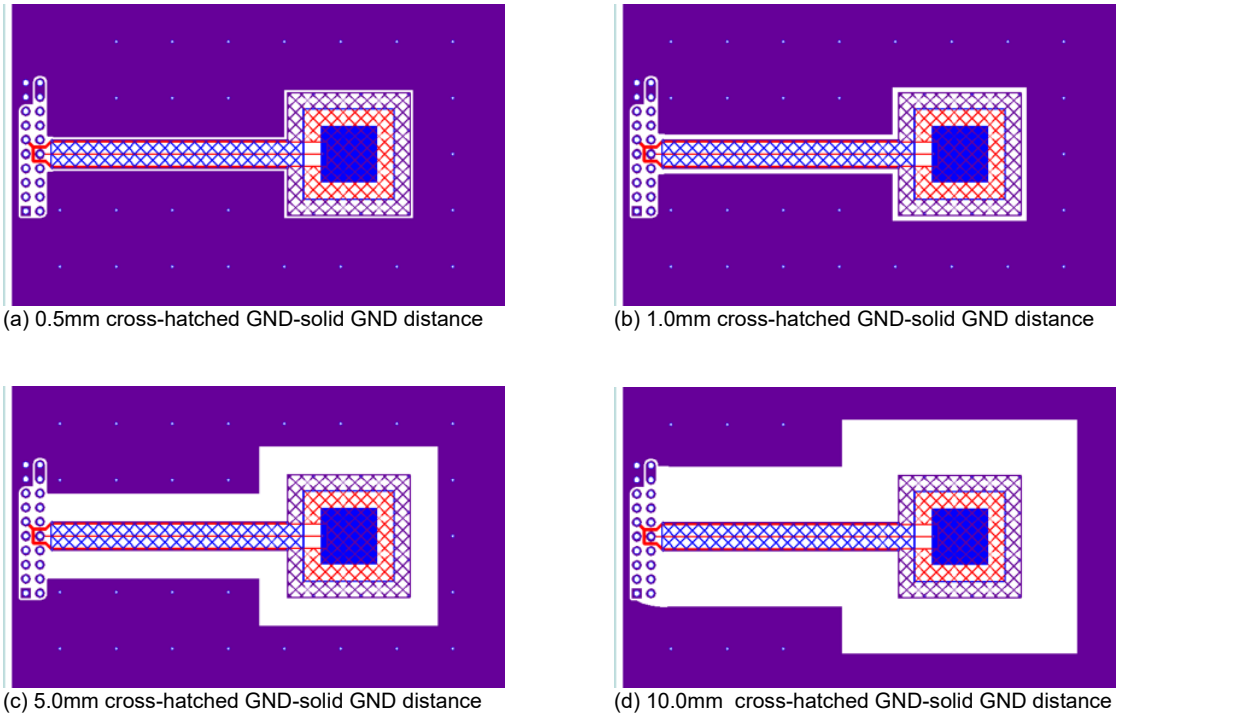
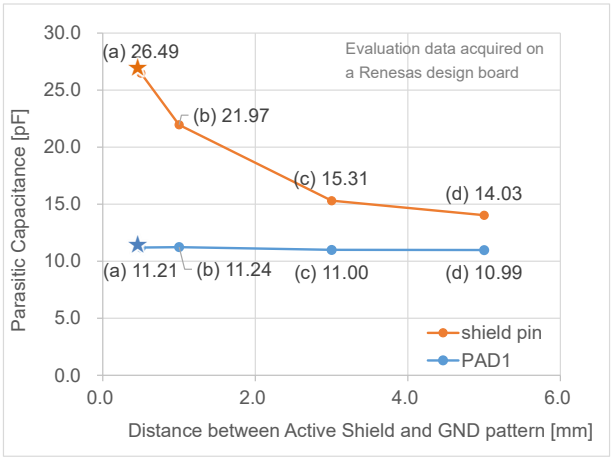


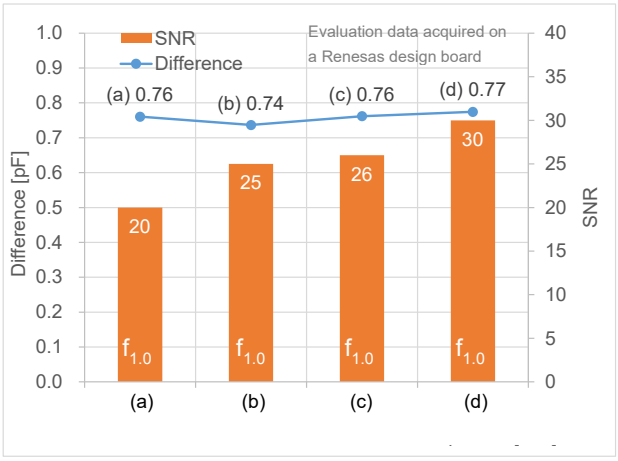
Figure 5-42 Evaluation Board Pattern (active shield-solid GND distance and sensitivity characteristics)

Figure 5-43 shows Active Shield-Solid GND Distance and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The parasitic capacitance of the button is constant regardless of the distance between the active shield and the solid GND. The recommended design values ensure plenty of distance between the active shield and solid GND so that the button's parasitic capacitance is not affected. The shorter the distance between the active shield and the solid GND, the more the parasitic capacitance of the active shield pin increases.
- Because the drive pulse frequency is selected according to the pin with the largest parasitic capacitance, the SNR may decrease based on the board design.



Parasitic capacitance including CPU board



Detected capacitance difference and SNR

Figure 5-43 Active Shield-Solid GND Distance and Sensitivity Characteristics

5.4.5.5 Active Shield Pattern Width

Table 5-22 lists Board Specifications for Active Shield Pattern Width Variations. For evaluation purposes, only the distance between electrode and active shield and the distance between the related wiring and the active shield were varied; all other design parameters remained fixed.

Table 5-22 Board Specifications for Active Shield Pattern Width Variations

Design Parameter	Specification	Unit	Notes
Active shield width	**1.0, 3.0, 5.0, 10.0**	**mm**	
Distance between electrode and active shield	**0.5, 3.0, 5.0**	**mm**	
Distance between wiring and active shield	**0.5, 3.0, 5.0**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	
Combined shield conditions (wiring-shield distance/ electrode-shield distance)			
Combination 1 (COND1)	3.0/3.0	mm	Recommended design values
Combination 2 (COND2)	0.5/0.5	mm	
Combination 3 (COND3)	5.0/5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

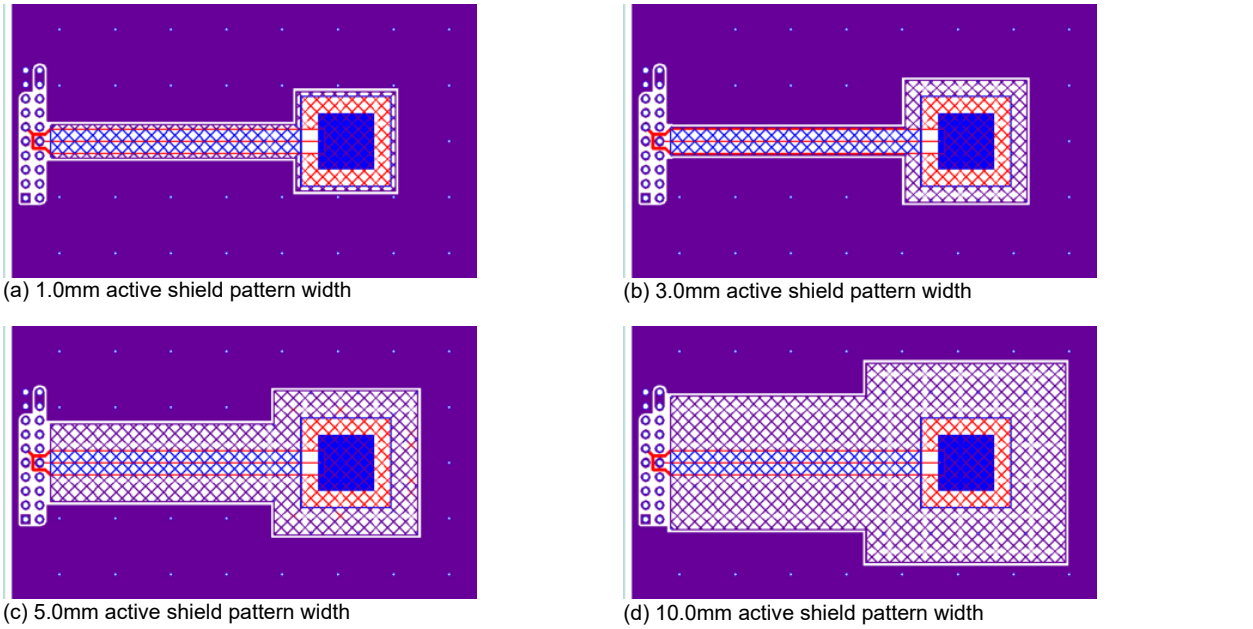
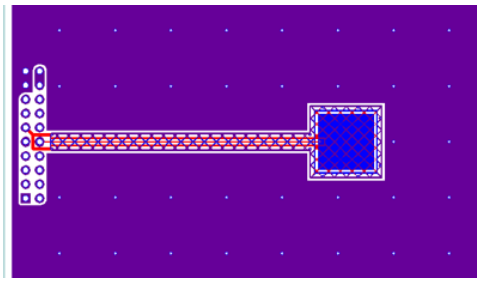
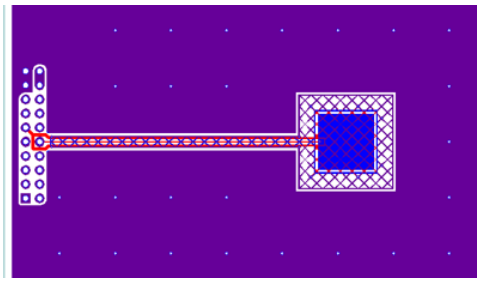


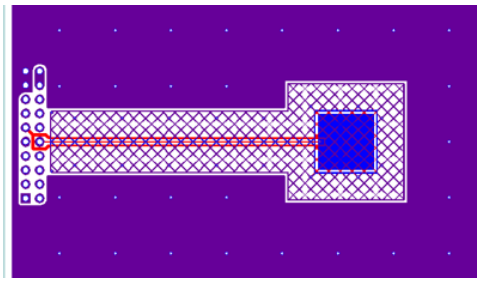
Figure 5-44 Evaluation Board Pattern (electrode/wiring and active shield distance: 3.0mm)



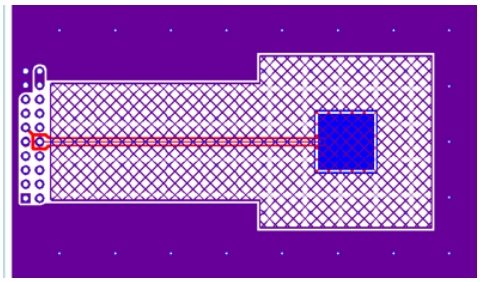
(a) 1.0mm active shield pattern width



(b) 3.0mm active shield pattern width



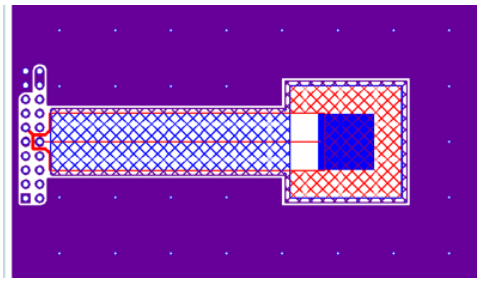
(c) 5.0mm active shield pattern width



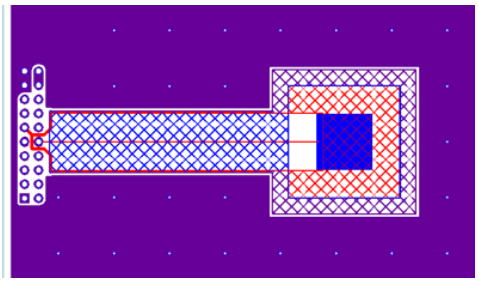
(d) 10.0mm active shield pattern width

Layer indication ■: Top layer, ■: Bottom layer

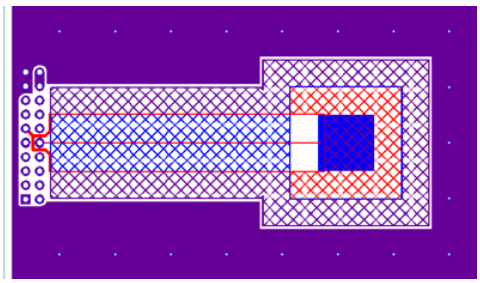
Figure 5-45 Evaluation Board Pattern (electrode/wiring and active shield distance: 0.5mm)



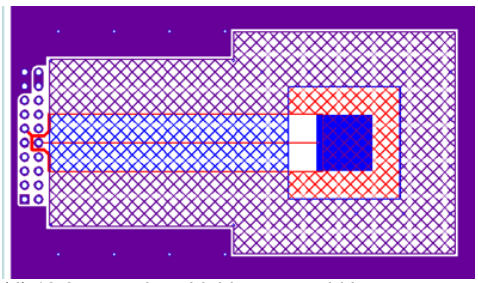
(a) 1.0mm active shield pattern width



(b) 3.0mm active shield pattern width



(c) 5.0mm active shield pattern width



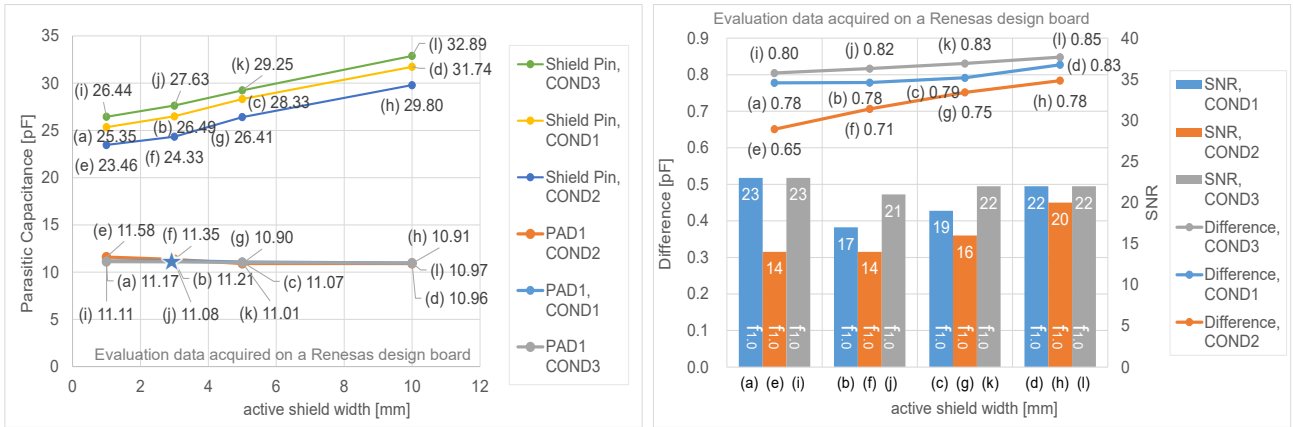
(d) 10.0mm active shield pattern width

Layer indication ■: Top layer, ■: Bottom layer

Figure 5-46 Evaluation Board Pattern (electrode/wiring and active shield distance: 5.0mm)

Figure 5-47 shows Active Shield Pattern Width and Sensitivity. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The parasitic capacitance of the button has a slight tendency to increase when the active shield width is narrow. The shorter distance between the electrode and the solid GND pattern, the more the parasitic capacitance is affected. The active shield pin parasitic capacitance also increases due to the increase in area caused by the shield width.
- The SNR does not change due to the active shield width, but if parasitic capacitance increases due to the board design, SNR may decrease due to lower drive pulse frequency.
- The shorter the distance between the active shield and the electrode and wiring, the more the capacitance detection tends to decrease.
  The shorter the distance between the electrode and the solid GND pattern on the periphery of the active shield, the stronger the capacitive coupling of the electrode, making it difficult for capacitance changes to occur when the electrode is touched.



Parasitic capacitance including CPU board

Detected capacitance difference and SNR

Figure 5-47 Active Shield Pattern Width and Sensitivity Characteristics

5.4.5.6 Damping Resistance Value of Active Shield Pin

Table 5-23 lists the Conditions for Evaluating Damping Resistance Value and Sensitivity Characteristics of Active Shield Pin. For evaluation purposes, only the number of button electrodes was varied; all other design parameters remained fixed.

Table 5-23 Conditions for Evaluating Damping Resistance Value and Sensitivity Characteristics of Active Shield Pin

Design Parameter	Specification	Unit	Notes
Damping resistance value	**10, 560, 1000**	Ω	
Shield type	Active shield	-	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

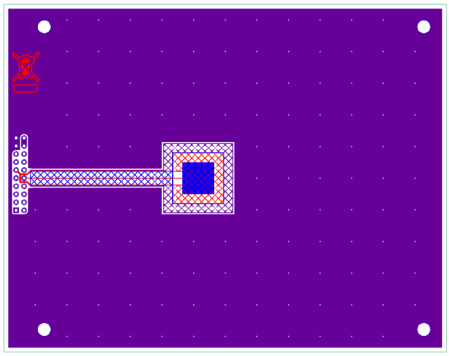


Figure 5-48 Evaluation Board Pattern

Figure 5-49 shows the Damping Resistance Value and Sensitivity of Active Shield Pin.

- When changing the damping resistance value of the active shield pin for the same electrode pattern, the button capacitance and SNR remain constant, regardless of the damping resistance of the active shield.
- Since the role of the damping resistor is to attenuate external noise, reducing the resistance value may result in unstable measurement values due to external noise or run the risk of stopping CTSU operations due to TSCAP voltage errors, etc. Always be sure to evaluate the resistance value thoroughly, especially if it is smaller than the recommended value of 560 Ohm.

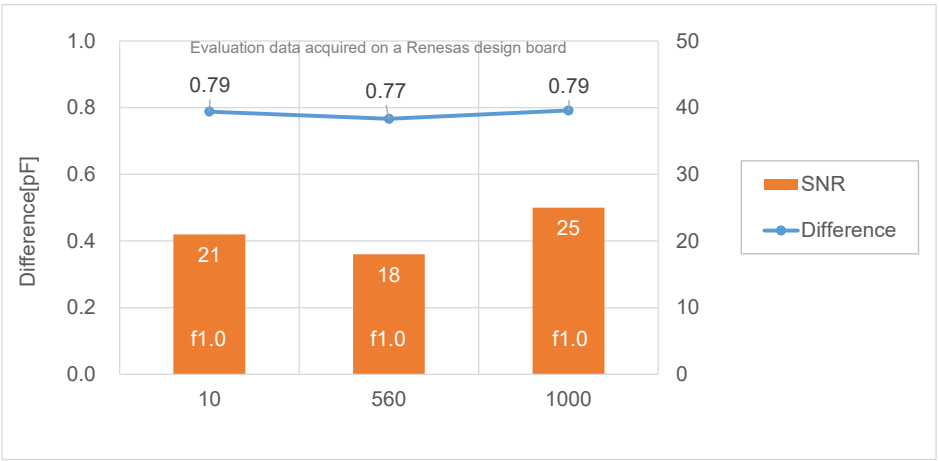


Figure 5-49 Damping Resistance Value and Sensitivity of Active Shield Pin Characteristics

5.4.6 Parameters Unrelated to Board Design

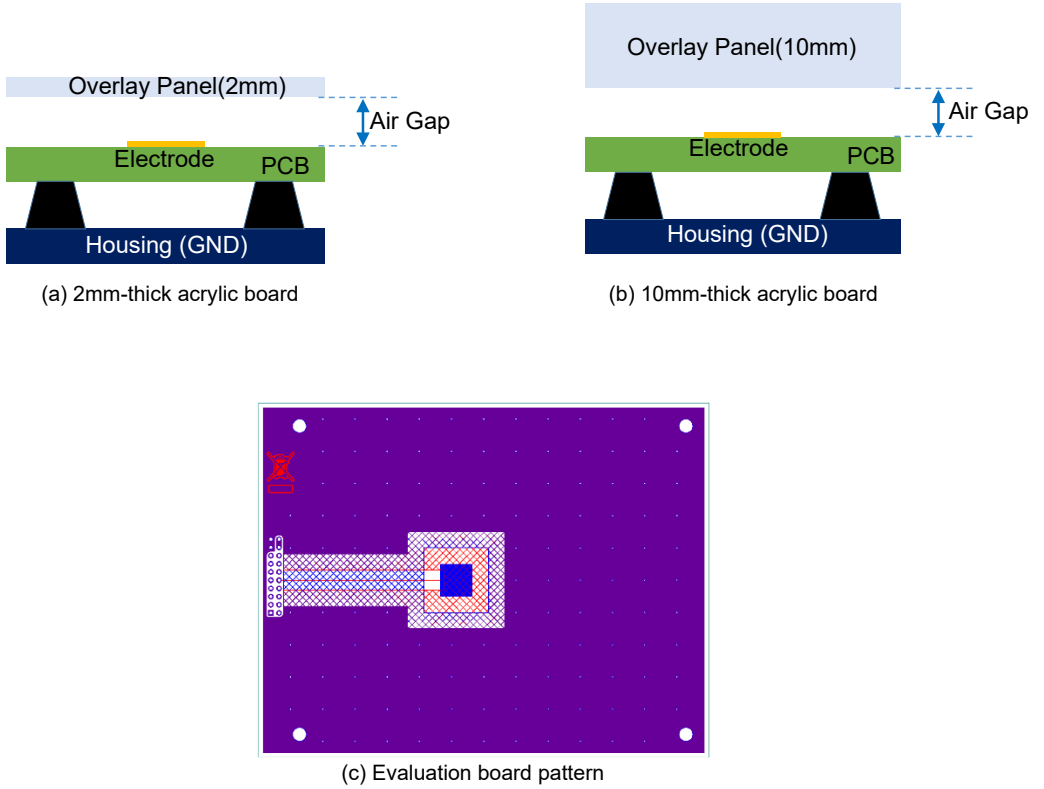
5.4.6.1 Overlay Design and Sensitivity Characteristics

Table 5-24 lists Board Specifications for Overlay Thickness and Air Gap Layer Variations. For evaluation purposes, all other design parameters remained fixed.

Table 5-24 Board Specifications for Overlay Thickness and Air Gap Layer Variations

Design Parameter	Specification	Unit	Notes
Overlay thickness	**2.0, 10.0**	**mm**	Acrylic
Air gap	**0, 1.0, 3.0, 5.0**	**mm**	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.



(a) 2mm-thick acrylic board

(b) 10mm-thick acrylic board

(c) Evaluation board pattern

Figure 5-50 Evaluation condition

Figure 5-51 shows Overlay Air Gap and Parasitic Capacitance.Figure 5-52 shows Overlay Air Gap and Sensitivity Characteristics Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The thicker the overlay, the more the parasitic capacitance increases, but the difference in detected capacitance decreases, resulting in a lower SNR.
- The wider the air gap, the lower the detected capacitance difference of the board and the lower the SNR.
- For capacitive touch, the electrode and finger are the equivalent of the electrodes of a capacitor, so the thicker the overlay panel, the lower the SNR. Also, because the dielectric constant is lower for the air gap than for the acrylic overlay, the wider the air gap, the lower the detected capacitance and SNR.
-

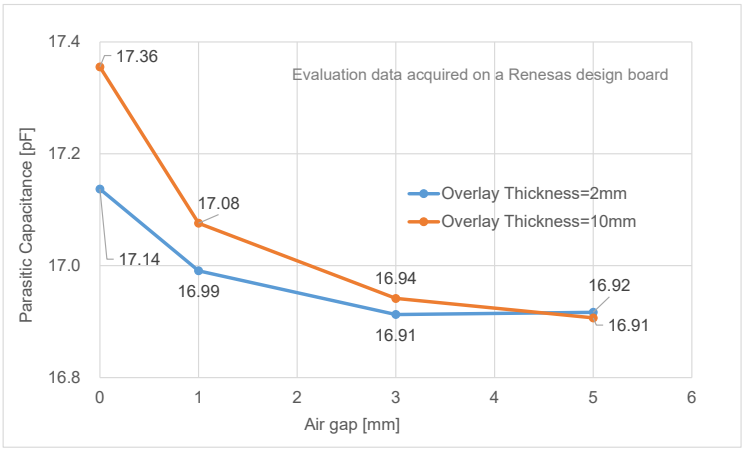
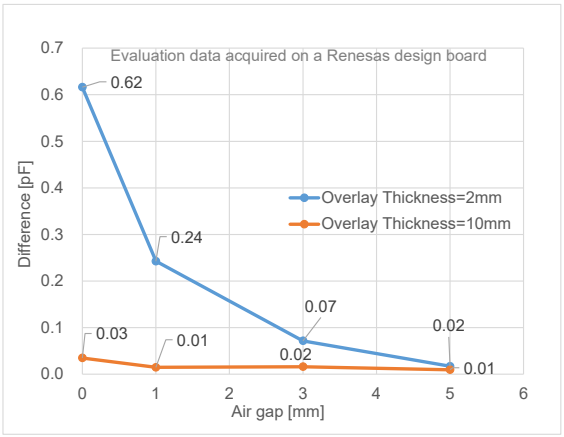
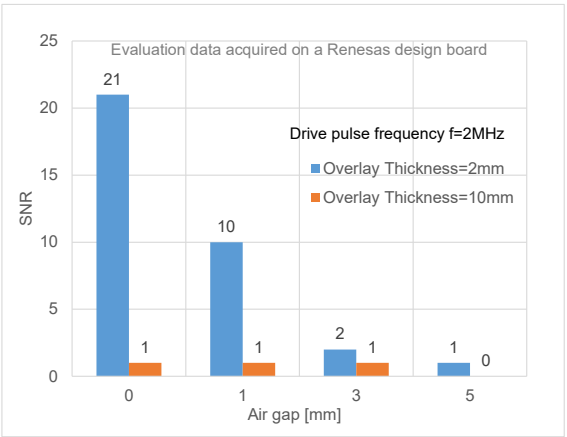


Figure 5-51 Overlay Air Gap and Parasitic Capacitance



Detected capacitance difference



SNR

Figure 5-52 Overlay Air Gap and Sensitivity Characteristics

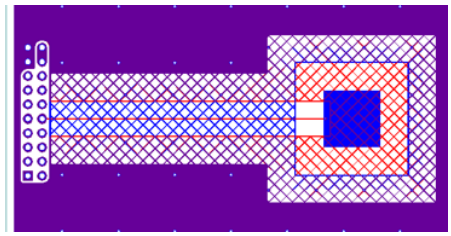
5.4.6.2 Electrode Damping Resistance Value and Sensitivity Characteristics

Table 5-25 lists Board Specifications for Damping Resistance. For evaluation purposes, all other design parameters remained fixed.

Table 5-25 Board Specifications for Damping Resistance Variations

Design Parameter	Specification	Unit	Notes
Damping resistance value	**10、560、1000**	**Ω**	
Shield type	Cross-hatched GND	-	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

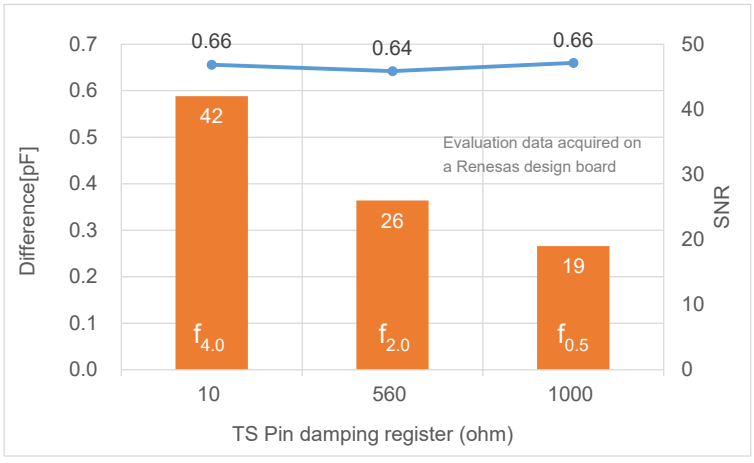


Layer indication ■ : Top layer, ■ : Bottom layer

Figure 5-53 Evaluation Board Pattern

Figure 5-54 shows Damping Resistance Value and Sensitivity.

- The time constant and the charging/discharging time of the circuit increase in proportion to the damping resistance value. It is necessary to ensure sufficient charging and discharging time for the parasitic capacitance of the TS pin to ensure successful CTSU measurements. Insufficient charging/discharging will result in unstable measurement values. Therefore, the drive pulse frequency must be lowered in order to secure sufficient charging/discharging time.
- The automatic adjustment function of QE for Capacitive Touch determines the most suitable drive pulse frequency based on the largest parasitic capacitance at non-touch.
- Since the role of the damping resistor is to attenuate external noise, reducing the resistance value may result in unstable measurement values due to external noise or run the risk of stopping CTSU operations due to TSCAP voltage errors, etc. Always be sure to evaluate the resistance value thoroughly, especially if it is smaller than the recommended value of 560 Ohm.



Note: f = drive pulse frequency

Figure 5-54 Damping Resistance Value and Sensitivity Characteristics

5.4.6.3 Board-Housing GND Distance and Sensitivity

Table 5-26 lists Board Specifications for Board-Housing GND Distance Variations. For evaluation purposes, all other design parameters remained fixed.

Table 5-26 Board Specifications for Board-Housing GND Distance Variations

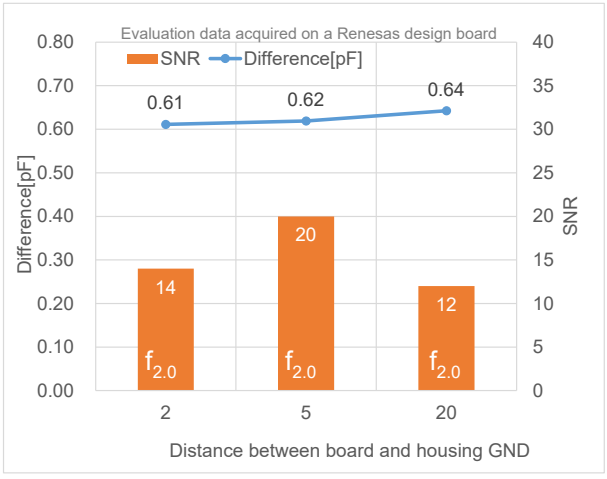
Design Parameter	Specification	Unit	Notes
Distance between board and housing GND (board spacer height)	**2.0, 5.0, 20.0**	**mm**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

Figure 5-55 Evaluation Condition

Figure 5-56 shows Board-Housing GND Distance and Sensitivity Characteristics。 Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- The shorter the distance from board surface to housing (assuming GND level conductors), the lower the sensitivity. Capacitive coupling becomes stronger the closer the board is to the housing, making it difficult for capacitance changes to occur when the electrode is touched.



Note: drive pulse frequency f = 2MHz

Figure 5-56 Board-Housing GND Distance and Sensitivity Characteristics

5.4.6.4 Sensitivity Characteristics with ESD Protection Diode Connected

Table 5-27 lists Board Specifications for Parasitic Capacitance Variations of ESD Protection Diode. For evaluation purposes, all other design parameters remained fixed. Note that this table indicates the sensitivity characteristics when an ESD protection diode is connected to the TS pin, but ESD tests have not been conducted. Also note that specifications such as location of the ESD protection diode and required pressure resistance differ according to system. Please keep this in mind when designing the pattern and selecting materials.

Table 5-27 Board Specifications for Parasitic Capacitance Variations of ESD Protection Diode

Design Parameter	Specification	Unit	Notes
ESD protection diode capacitance (Typ value)	**0 (not connected), 0.75, 10, 30**	**pF**	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

Figure 5-57 shows Circuit Diagram for ESD Protection Diode Parasitic Capacitance Evaluation Board

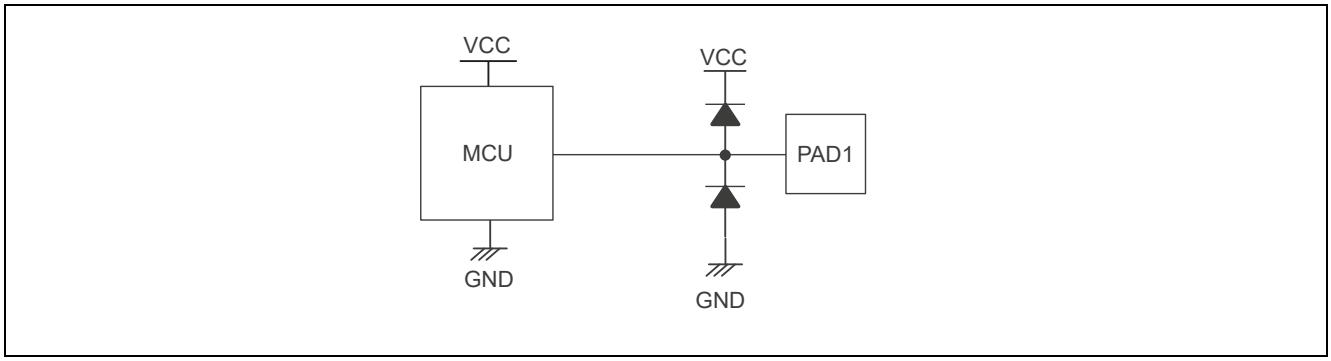


Figure 5-57 Circuit Diagram for ESD Protection Diode Parasitic Capacitance Evaluation Board

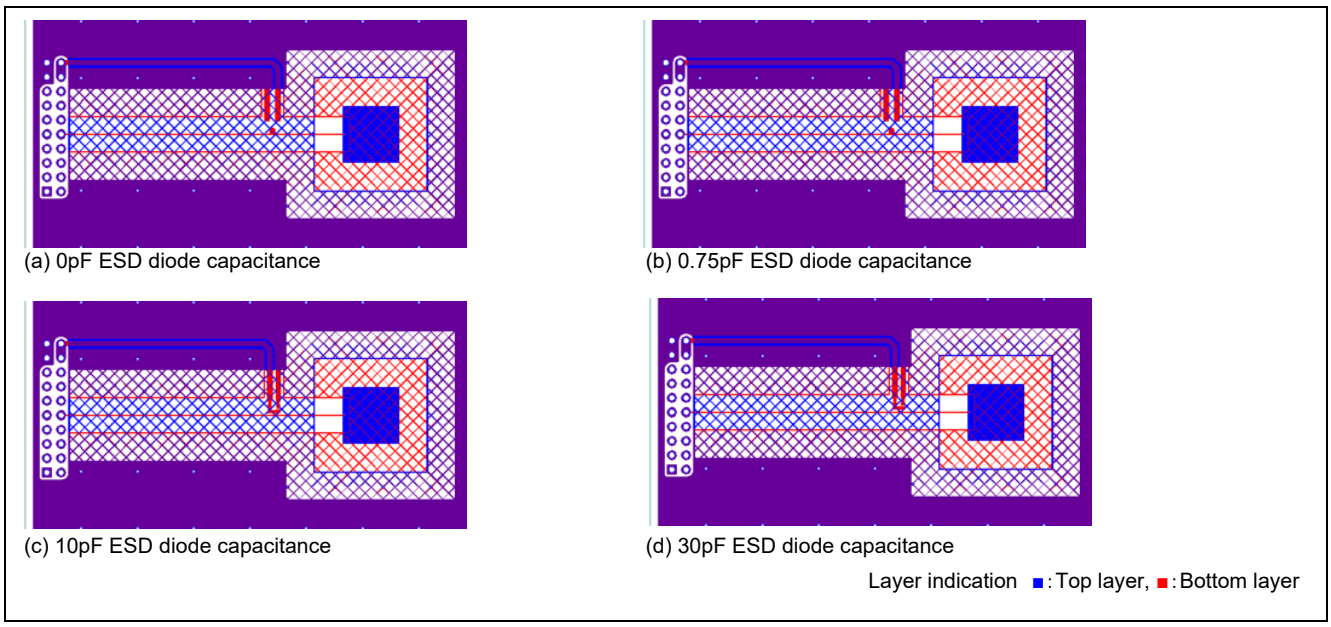
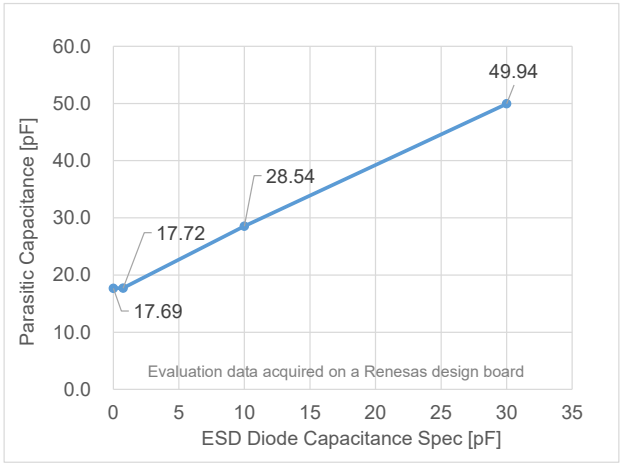


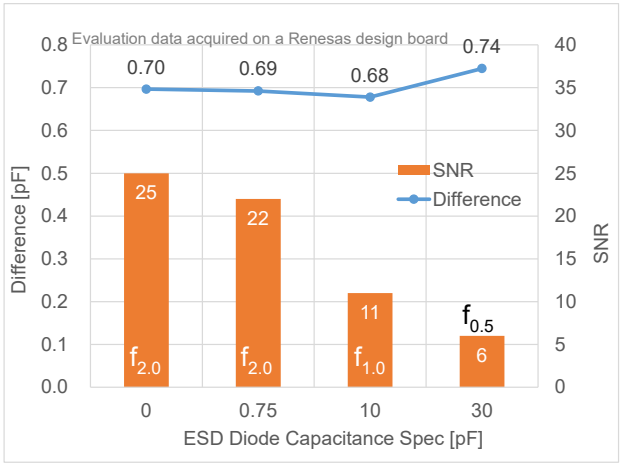
Figure 5-58 Evaluation Board Pattern

Figure 5-59 shows ESD Protection Diode Parasitic Capacitance and Sensitivity Characteristics. Parasitic capacitance includes the CPU board parasitic capacitance of approximately 10.48pF.

- When an ESD protection diode is connected to the TS pin, the capacitance of the connected element is added; if the capacitance is large, the drive pulse frequency drops, making the sensitivity lower as well.
- Since the CTSU estimates capacitance from the amount of current applied to parasitic capacitance, if you plan to use an ESD protective diode, make sure to select a product with a low capacitance value and minimal leakage current.



(i) Parasitic capacitance including CPU board



(ii) Detected capacitance difference and SNR

Figure 5-59 ESD Protection Diode Parasitic Capacitance and Sensitivity Characteristics

5.4.6.5 Supply Voltage and Sensitivity Characteristics

Table 5-28 lists Electrode Specifications for Supply Voltage Variations. For evaluation purposes, only the supply voltage was varied; all other design parameters remained fixed.

Table 5-28 Electrode Specifications for Supply Voltage Variations

Design Parameter	Specification	Unit	Notes
Supply voltage	**1.8、3.3、5.0**	**V**	
Shield type	Cross-hatched GND	-	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

Table 5-29 lists CTSU1 Device Evaluation Conditions and Table 5-30 lists CTSU2 Device Evaluation Conditions. This evaluation was conducted for the CTSU1 device and CTSU2 device.

Table 5-29 CTSU1 Device Evaluation Conditions

Item	Specifications
CPU board	RX130 Cap Touch CPU Board (RTK0EG0004C01002BJ) (RX130 Capacitive Touch Evaluation System (RTK0EG0003S02001BJ) accessory)
MCU	RX130 (R5F51305ADFN)
Operating frequency	32MHz

Table 5-30 CTSU2 Device Evaluation Conditions

Item	Specifications
CPU board	RX140 Cap Touch CPU Board (RTK0EG0038C01001BJ) (RX140 Capacitive Touch Evaluation System (RTK0EG0039S01001BJ) accessory)
MCU	RX140 (R5F51406ADFN)
Operating frequency	48MHz

Table 5-31 provides the Evaluation Software Development Environment (RX MCU) and Figure 5-60 shows the List of Selected Components.

Table 5-31 Evaluation Software Development Environment (RX MCU)

Item	Specifications
Integrated Development Environment	Renesas e² studio Version: 2022-04
Compiler	Renesas CC-RX v3.04.00
Development support tool for capacitive method touch sensor	QE for Capacitive Touch V3.0.2
Emulator	Renesas E2 Lite emulator

Selected components:

Component	Version	Configuration
Board Support Packages. (r_bsp)	7.10	r_bsp(used)
Byte-based circular buffer library. (r_...	2.00	r_byteq(used)
CMT driver (r_cmt_rx)	5.10	r_cmt_rx(used)
CTSU QE API (r_ctsu_qe)	2.10	r_ctsu_qe(used)
Ports	2.3.0	Config_PORT(PORT: used)
SCI/SCIF Asynchronous Mode	1.11.0	Config_SCI6(SCI6: used)
Touch QE API (rm_touch_qe)	2.10	rm_touch_qe(used)

Figure 5-60 List of Selected Components

Figure 5-61 shows Automatic Adjustment Results by QE for Capacitive Touch. "Scan Time[ms]" indicates the measurement time for each channel including software overhead processing. The hardware measurement time is 0.526ms for CTSU1 and 0.256ms for CTSU2. CTSU2 supports the multi-frequency measurements in hardware and configures three frequencies of multi-frequency measurements with automatic tuning of QE for Capacitive Touch. At this time, the measurement time for each frequency is 0.128ms. Measurement result of the multi-frequency measurement is calculated from the two frequencies of measurement value selected by majority decision, so the measurement time is equivalent to 0.256 ms. CTSU1 measures at only one frequency.

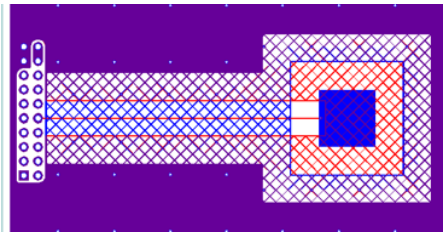
Method	Kind	Name	Touch Sensor	Parasitic Capacitance[pF]	Sensor Drive Pulse Frequency[MHz]	Threshold	Scan Time[ms]	Overflow
config01	Button(self)	PAD1	TS29	15.105	1.886 (BASE: 2.0)	1240	0.559	None

(a) CTSU1 (RX130)

Method	Kind	Name	Touch Sensor	Parasitic Capacitance[pF]	Sensor Drive Pulse Frequency[MHz]	Threshold	Scan Time[ms]	Overflow
config01	Button(self)	Button00	TS29	15.417	2.0	883	0.576	None

(b) CTSU2 (RX140)

Figure 5-61 Automatic Adjustment Results by QE for Capacitive Touch



Layer indication ■ : Top layer, ■ : Bottom layer

Figure 5-62 Evaluation Board Pattern

(1) Normal Mode Operations

Figure 5-63 shows Normal Mode Supply Voltage and Sensitivity Characteristics. Normal mode operations indicate conditions in which the CTSU operates with the CTSUCR1.CTSUATUNE0 bit set to '0' for RX130 and the CTSUCRA.ATUNE0 bit is set to '0' for RX140.

- Supply voltage does not cause changes in the measured values or sensitivity.
- The difference in the measured values and SNR of CTSU1 and CTSU2 is due to the difference in measurement time. The measurement time of CTSU2 is about 1/2 that of CTSU1, but the measured value and SNR are about 2/3, so the measurement accuracy per unit time is improved.

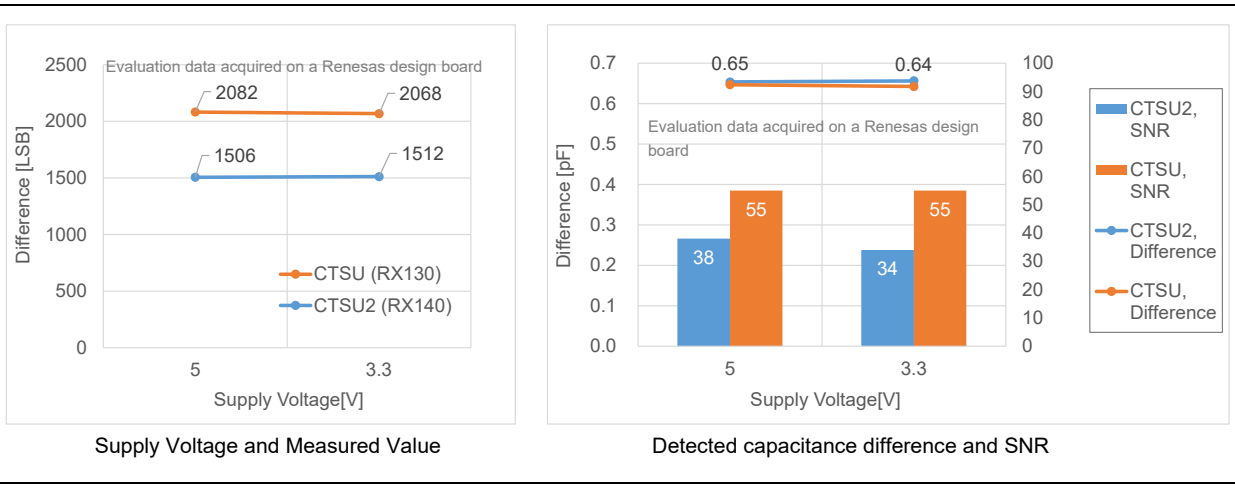


Figure 5-63 Normal Mode Supply Voltage and Sensitivity Characteristics

(2) Low Voltage Mode

Low voltage mode operations indicate conditions in which the CTSU operates with the CTSUCR1.CTSUATUNE0 bit set to '1' for RX130 and the CTSUCRA.ATUNE0 bit is set to '1' for RX140. Not all MCUs support low voltage mode operations. Please confirm whether the MCU you plan on using supports low voltage mode in the corresponding MCU User's Manual. Operations are not guaranteed when the related registers are set on MCUs that do not support this feature.

- Supply voltage does not cause changes in the measured values or sensitivity.
- The difference in the measured values and SNR of CTSU1 and CTSU2 is due to the difference in measurement time. The measurement time of CTSU2 is about 1/2 that of CTSU1, but the measured value and SNR are about 2/3, so the measurement accuracy per unit time is improved.

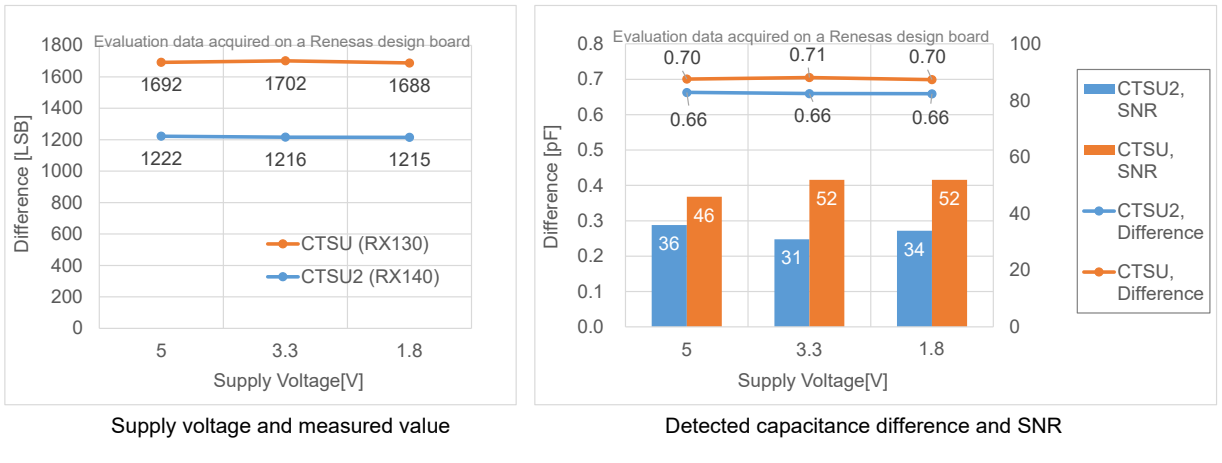


Figure 5-64 Low Voltage Mode Supply Voltage and Sensitivity Characteristics

5.4.6.6 Sensitivity at Wire Touch

Table 5-32 lists Board Specifications at Electrode Wire Touch. For evaluation purposes, all other design parameters remained fixed.

Table 5-32 Board Specifications at Electrode Wire Touch

Design Parameter	Specification	Unit	Notes
Shield type	**Cross-hatched GND, active shield**	-	
Overlay thickness	2.0	mm	Acrylic
Air gap	0	mm	
Board spacer	5.0	mm	

Note: Recommended design values shown in Table 5-5, except as noted.

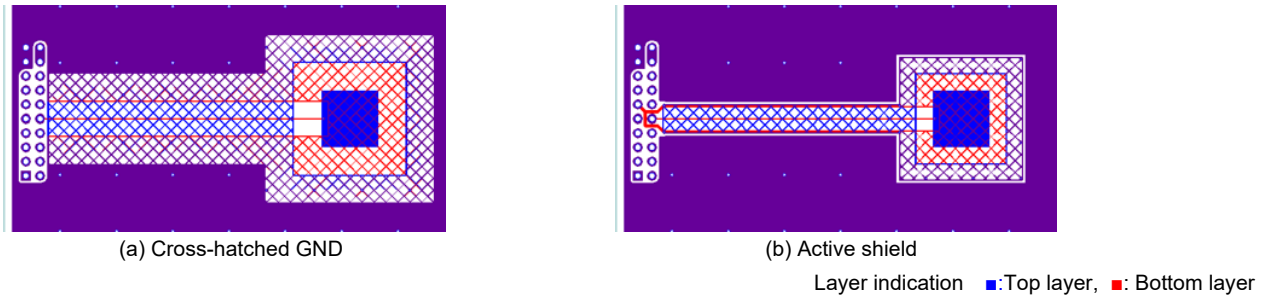


Figure 5-65 Evaluation Board Pattern

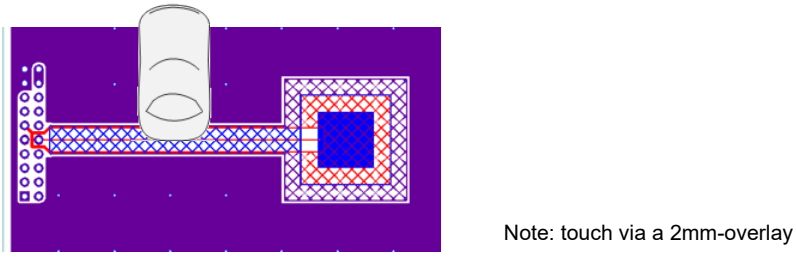


Figure 5-66 Wire Touch Position

Figure 5-67 shows Sensitivity at Wire Touch. Wire touch on the overlay above the shield pattern does not generate a touch-detectable SNR.

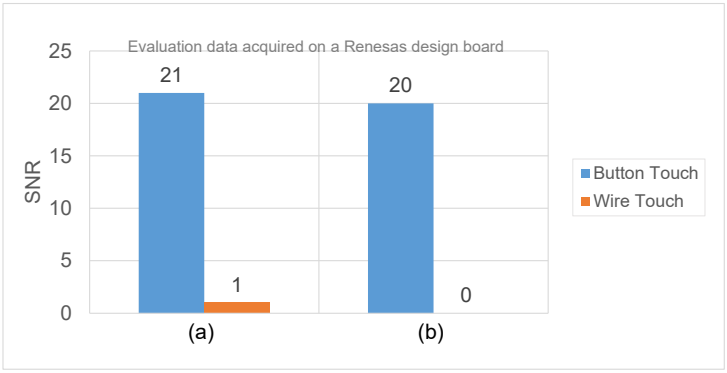


Figure 5-67 Sensitivity at Wire Touch

Website and Support

For information on capacitive touch, download tools and documentation, and technical support, please visit the Renesas website links below.

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	Apr.12.21	-	First edition issued
2.0	Sep.30.22	9	Corrections to recommended dimension descriptions and values Figure2-9 (a): dimensions corrected, Figure2-9: added (b)
		16	Figure2-20: added notes to calculation method Added Table 2-1
		24	Figure3-5: corrected Type C electrode dimensions
		34	Added 5. Self-capacitance Method Button Patterns and Characteristics Data

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
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