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H8SX Family

Cascade Connection of 8-Bit Timers

Introduction

A unit of timers in the 8-bit timer module (TMR) are cascade-connected to operate as a 16-bit timer.

Target Device

H8SX/1663

Contents

1. Specification

- Two 8-bit timers are cascade-connected, with one acting as the higher-order eight bits and the other acting as the lower-order eight bits, for operation as a 16-bit timer.
- The output-comparison function is employed to confirm operation as a 16-bit timer by producing an output pulse waveform with a specified duty cycle. When this sample task is executed on a microcontroller with Pϕ = 24 MHz, the output pulse waveform has a period of 13.65 ms and a duty cycle of 70%.

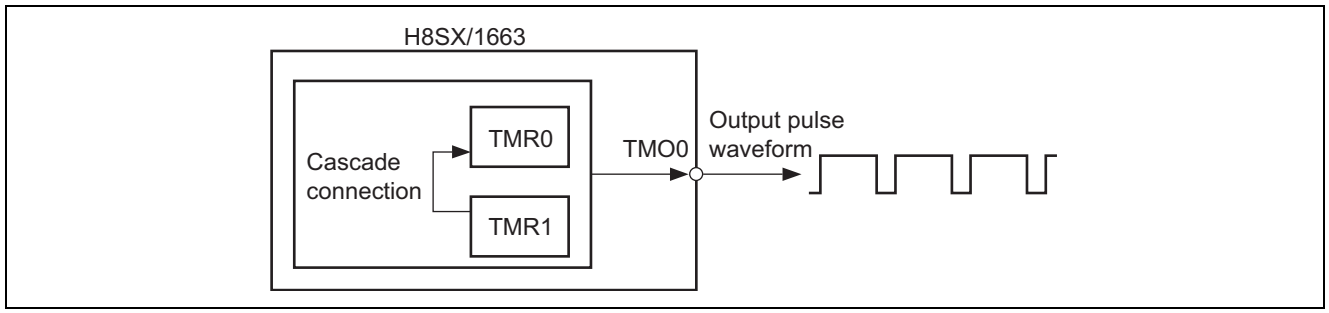


Figure 1 Example of Pulse Output by Cascade-Connected 8-Bit Timers

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 12 MHz System clock (Iϕ): 48 MHz Peripheral-module clock (Pϕ): 24 MHz External bus clock (Bϕ): 48 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)

3. Description of Modules Used

3.1 8-Bit Timer Module (TMR)

Cascade connection (of 8-bit timers TMR_0 and TMR_1) within TMR unit 0 is employed to obtain 16-bit timer operation and produce a pulse waveform with a fixed duty cycle as the output on pin TIO0. Figure 2 is a block diagram of timer unit 0, and explanations of the blocks are given after the figure.

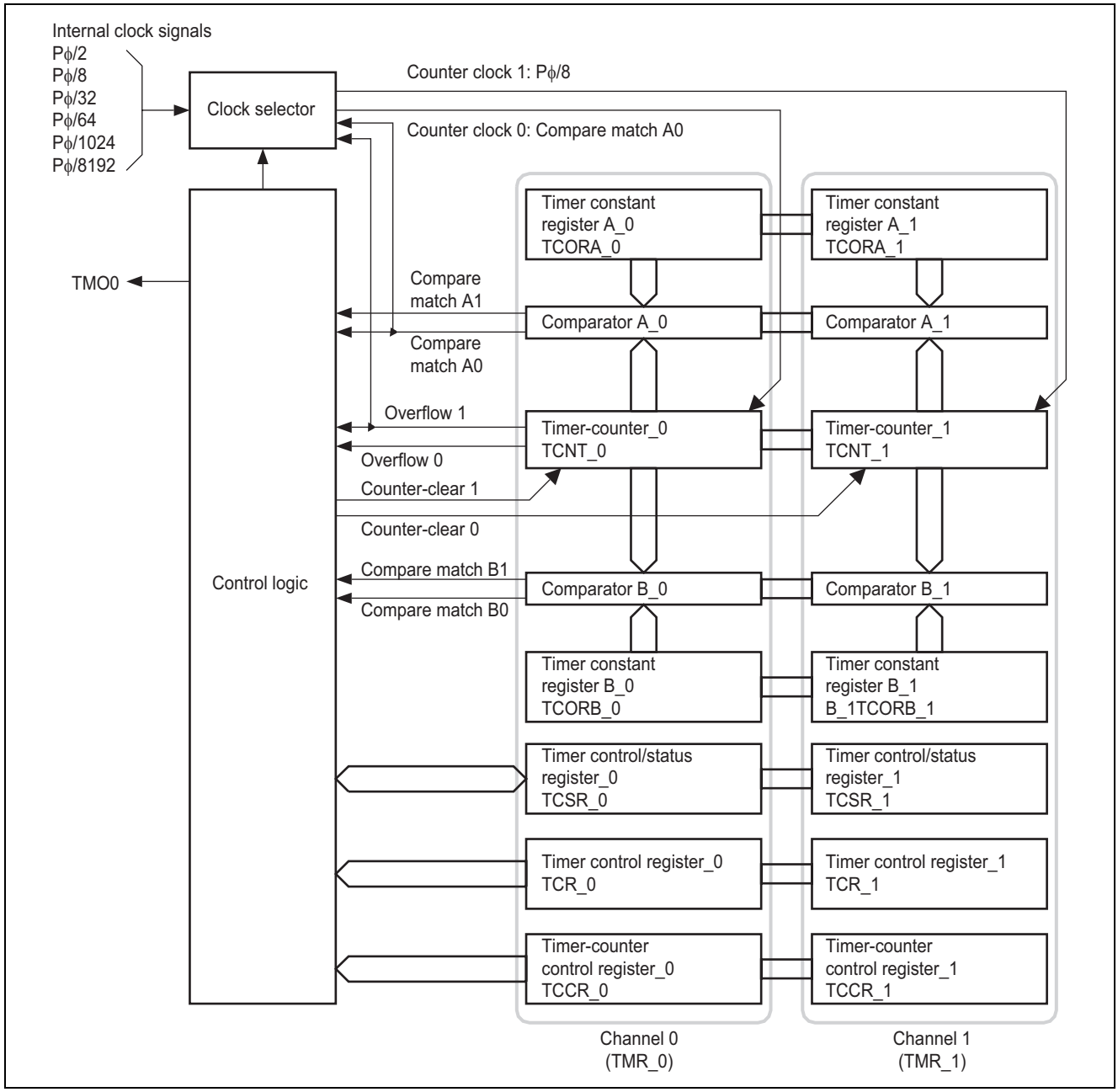


Figure 2 Block Diagram of Timer Unit 0

- Internal peripheral clock, Pϕ
  This is the standard clock that makes the internal peripheral modules run, and is generated by a clock oscillator.
- Timer-counter_0 (TCNT_0)
- Timer-counter_1 (TCNT_1)
  Each TCNT register is an 8-bit readable and writable up-counter. The clock signal that drives counting is selected by the CKS2 to CKS0 bits of the corresponding TCR and the ICKS1 and ICKS0 bits of the corresponding TCCR. TCNT can be cleared by an external reset signal, compare-match A signal, or compare-match B signal. The signal is selected by bits CCLR1 and CCLR2 of the TCR. The initial value of TCNT is H'00.
- Time Constant Register A_0 (TCORA_0)
- Time Constant Register A_1 (TCORA_1)
  Each TCORA is an 8-bit readable and writable register. The value in TCORA is continually compared with the value in the corresponding TCNT. When a match is detected, CMFA flag in the corresponding TCSR is set to one. Furthermore, the timer output from the TMO pin is controlled according to this compare-match signal (compare match A) and the settings of bits OS1 and OS0 in TCSR. The initial value of TCORA is H'FF.
- Time Constant Register B_0 (TCORB_0)
- Time Constant Register B_1 (TCORB_1)
  Each TCORB is an 8-bit readable and writable register. The value in TCORB is continually compared with the value in TCNT. When a match is detected, the corresponding CMFB flag in TCSR is set to one. Furthermore, the timer output from the TMO pin is controlled according to this compare-match signal (compare match B) and the settings of bits OS3 and OS2 in TCSR. The initial value of TCORB is H'FF.
- Timer Control Register 0 (TCR_0)
- Timer Control Register 1 (TCR_1)
  Each TCR selects the clock source and condition for clearing of the corresponding TCNT, and enables or disables the several interrupt requests.
- Timer Counter Control Register 0 (TCCR_0)
- Timer Counter Control Register 1 (TCCR_1)
  Each TCCR selects the internal clock source for the corresponding TCNT and controls external reset input.
- Timer Control/Status Register 0 (TCSR_0)
- Timer Control/Status Register 1 (TCSR_1)
  Each TCSR contains status flags and controls compare-match output.

3.2 16-Bit Counting Mode Obtained by Cascade Connection

When the bits CKS2 to CKS0 in TCR_0 are set to B'100, the timers function as a single 16-bit timer, with TMR_0 providing the eight higher-order bits and TMR_1 providing the eight lower-order bits.

1. Setting of Compare-Match Flags

- The CMF flag in TCSR_0 is set to one when a 16-bit compare-match event occurs.
- The CMF flag in TCSR_1 is set to one when a compare match for the eight lower-order bits occurs.

2. Counter-Clearing Specification

- If the CCLR1 and CCLR0 bits in TCR_0 have been set for counter-clearing on compare matches, the16-bit counter (TCNT_0 and TCNT_1 together) is cleared when a 16-bit compare-match event occurs. The 16-bit counter (combination of TCNT0 and TCNT1) is cleared in this case even when counter-clearing by the TMRI0 pin has been selected.
- The settings of the CCLR1 and CCLR0 bits in TCR_1 are ignored. The eight lower-order bits cannot be cleared independently.

3. Pin Output

- Control of output from the TMO0 pin by the OS3 to OS0 bits in TCSR_0 is in accord with the 16-bit compare-match condition.
- Control of output from the TMO1 pin by the OS3 to OS0 bits in TCSR_1 is in accord with the compare-match condition for the lower-order eight bits.

4. Principle of Operation

The operation of cascade-connected 8-bit timers is illustrated in figure 3. Processing by hardware and software processing in the numbered parts of figure 3 is explained in table 2.

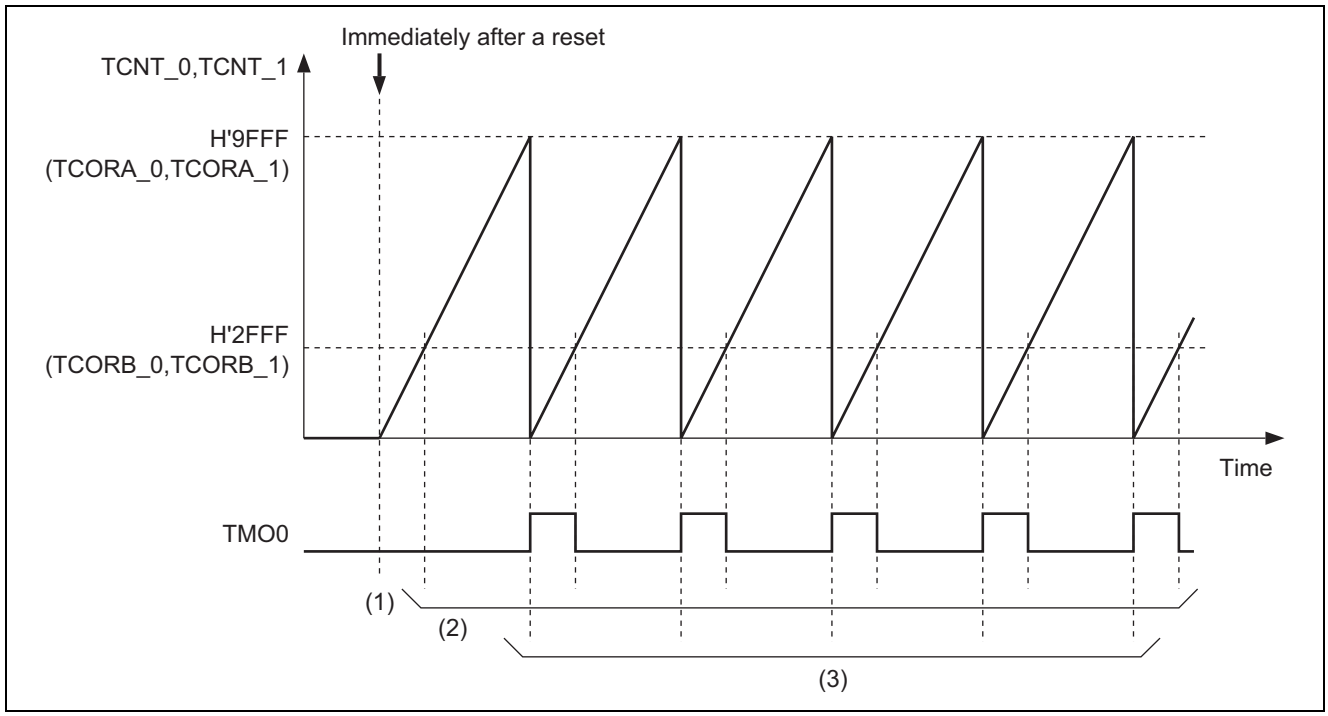


Figure 3 Illustration of the Operation of Cascade-Connected 8-Bit Timers

Table 2 Description of Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial settings*
(2)	Compare matches of TCORB_0, TCORB_1 and TCNT_0, TCNT_1 a. Zero is output on the TMO0 pin.	No processing
(3)	Compare matches of TCORA_0, TCORA_1 and TCNT_0, TCNT_1 a. One is output on the TMO0 pin. b. TCNT_0 and TCNT_1 are cleared.	No processing

Notes on initial settings: *

a. The 16-bit counting mode, where the timers are cascade-connected so that the overflow signal from TCNT_1 drives counting by TCNT_0, is set.
b. Generation of 16-bit compare matches (with TCORA_0 and TCORA_1) is set as the condition for clearing of TCNT_0 and TCNT_1.
c. Counter TCNT_1 is set to count rising edges of Pϕ/8.
d. The 16-bit counter (TCNT_0, TCNT_1) is cleared.
e. The period of the output pulse waveform is set (TCORA_0, TCORA_1 = H'9FFF).
f. The interval at high level of the output pulse waveform is set (TCORB_0, TCORB_1 = H'2FFF).
g. Compare match B, generated by matching of TCORB_0, TCORB_1 and TCNT_0, TCNT_1, is set to produce a zero output on the TMO0 pin.

5. Description of Software

5.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.01.01
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Ver.6.01.02 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register,shift,struct,expression)

Table 4 Setting of Sections

Address	Section	Description
H'001000	P	Program space

Table 5 Interrupt and Exception Handling Vector Table

Exception Handling Source	Vector Number	Vector Table Address	Exception Handling Routine
Reset	0	H'000000	init

5.2 List of Functions

Table 6 Functions in File main.c

Function Name	Functions
init	Initialization routine Sets the CCR and configures the clocks, releases the required modules from the module stop mode, and calls the main function.
main	Main routine Makes settings for cascade-connection of the 8-bit timers and for the output pulse waveform.

5.3 Calculating Parameters of the Output Pulse Waveform from Formulae

The clock signal that drives counting by TCNT_0, TCNT_1 is Pϕ/8, Pϕ = 24 MHz, TIOCA_0 = H'9F, TIOCA_1 = H'FF, TIOCB_0 = H'2F, and TIOCB_1 = H'FF, so the period, interval at high level, and duty cycle of the output pulse waveform are as calculated below.

Period = (TIOCA_0, 1 + 1) × 1/(Pϕ/8) = (H'9FFF + 1)/(24 MHz/8) ≅ 13.65 ms.

Interval at high level= (TIOCB_0, 1 + 1) × 1/(Pϕ/8) = (H'2FFF + 1)/(24 MHz/8) ≅ 4.10 ms.

Duty cycle = (interval at high level)/period × 100 = 4.10 ms/13.65 ms x 100 ≅ 30%.

5.4 Description of Functions

5.4.1 init Function

1. Functional overview
   Initialization routine, which releases the required modules from module-stop mode, configures the clocks, and calls the main function.
2. Argument
   None
3. Return value
   None
4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. The latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0 These bits indicate the operating mode selected by mode pins (MD2 to MD0; see table 7). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latching is released by a reset.
10	MDS2	Undefined*	R	
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Values are determined by the levels on pins MD0 to MD3.

Table 7 Settings of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select These bits select the frequency of the system clock, which is provided to the CPU, DMAC, and DTC. 000: Input clock × 4
9	ICK1	0	R/W	
8	ICK0	0	R/W	
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select These bits select the frequency of the peripheral module clock. 001: Input clock × 2
5	PCK1	0	R/W	
4	PCK0	1	R/W	
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select These bits select the frequency of the external bus clock. 000: Input clock × 4
1	BCK1	0	R/W	
0	BCK0	0	R/W	

- MSTPCRA, B and C control module-stop mode. Setting a bit to 1 makes the corresponding module enter the module-stop state, while clearing the bit to 0 releases the module from module-stop state.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable This bit enables/disables all-module-clock-stop mode for reducing current consumption by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3 and TMR_2)
8	MSTPA8	0	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

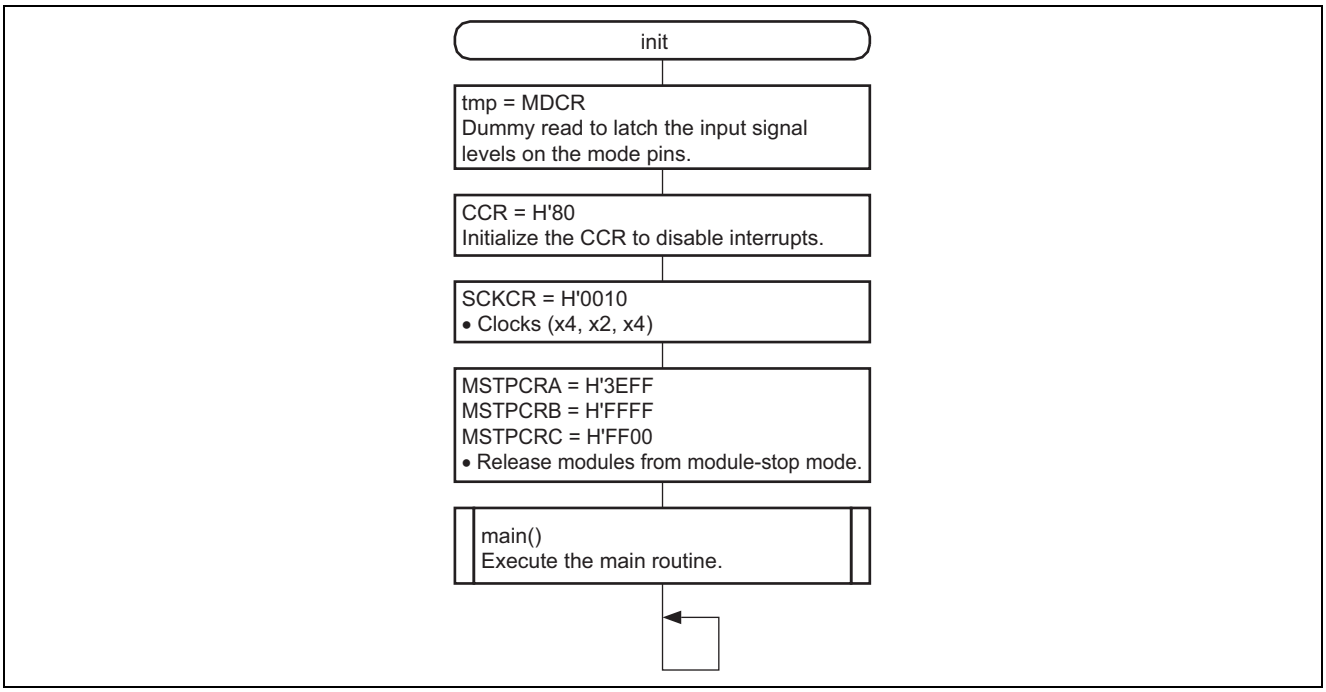
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface 1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface 0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5) , (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check module
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input signal levels on the mode pins.
CCR = H'80
Initialize the CCR to disable interrupts.
SCKCR = H'0010
• Clocks (x4, x2, x4)
MSTPCRA = H'3EFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Release modules from module-stop mode.
main()
Execute the main routine.

5.4.2 main Function

1. Functional overview
   Makes settings for cascade-connection of the 8-bit timers and for the output pulse waveform.

2. Argument
   None

3. Return value
   None

4. Description of internal registers
   The internal registers used in this sample task are described below. The settings shown in these tables are the values used in this sample task and differ from the initial values.

- Timer control register_0 (TCR_0) Number of bits: 8 Address: H'FFFFB0

Bit	Bit Name	Setting	R/W	Description
4	CCLR1	0	R/W	Counter Clear 1 and 0
3	CCLR0	1	R/W	01: Compare match A clears TCNT_0.
2	CKS2	1	R/W	Clock Select 2 to 0
1	CKS1	0	R/W	Refer to table 8.
0	CKS0	0	R/W	CKS2 to CKS0 = B'100: Counting is driven by the overflow signal from TCNT_1.

- Timer control register_1 (TCR_1) Number of bits: 8 Address: H'FFFFB1

Bit	Bit Name	Setting	R/W	Description
2	CKS2	0	R/W	Clock Select 2 to 0
1	CKS1	0	R/W	Refer to table 8.
0	CKS0	1	R/W	CKS2 to CKS0 = B'001, ICKS1 and ICKS0 = B'00: Counting is of rising edges of Pϕ/8.

- Timer control/status register_0 (TCSR_0) Number of bits: 8 Address: H'FFFFB2

Bit	Bit Name	Setting	R/W	Description
3	OS3	0	R/W	Output Select 3, 2
2	OS2	1	R/W	These bits select the output on pin TMO0 in response to compare match B, i.e. a match between TCNT_0 and TCORB_0. 01: 0 output
1	OS1	1	R/W	Output Select 1, 0
0	OS0	0	R/W	These bits select the output on pin TMO0 in response to compare match A, i.e. a match between TCNT_0 and TCORA_0. 10: 1 output

- Timer constant register A_0 (TCORA_0) Number of bits: 8 Address: H'FFFFB4

Function: This is an 8-bit readable and writable register. Its value is constantly compared with TCNT_0; when a match is detected, the CMFA bit of TCSR_0 is set to 1.

Value: H'9F

- Timer constant register A_1 (TCORA_1) Number of bits: 8 Address: H'FFFFB5

Function: This is an 8-bit readable and writable register. Its value is constantly compared with TCNT_1; when a match is detected, the CMFA bit of TCSR_1 is set to 1.

Value: H'FF

- Timer constant register B_0 (TCORB_0) Number of bits: 8 Address: H'FFFFB6

Function: This is an 8-bit readable and writable register. Its value is constantly compared with TCNT_0; when a match is detected, the CMFB bit of TCSR_0 is set to 1.

Value: H'2F

- Timer constant register B_1 (TCORB_1) Number of bits: 8 Address: H'FFFFB7

Function: This is an 8-bit readable and writable register. Its value is constantly compared with TCNT_1; when a match is detected, the CMFB bit of TCSR_1 is set to 1.

Value: H'FF

- Timer counter_0 (TCNT_0) Number of bits: 8 Address: H'FFFFB8

Function: This is an 8-bit readable and writable register. In this sample task, it is cleared by a compare match A for TMR_0.

Value: H'00

- Timer counter_1 (TCNT_1) Number of bits: 8 Address: H'FFFFB9

This is an 8-bit readable and writable register. In this sample task, it is cleared by a compare match A for TMR_1.

Value: H'00

- Timer counter control register_1 (TCCR_1) Number of bits: 8 Address: H'FFFFBA

Bit	Bit Name	Setting	R/W	Description
1	ICKS1	1	R/W	Internal Clock Select 1, 0
0	ICKS0	0	R/W	See table 8.

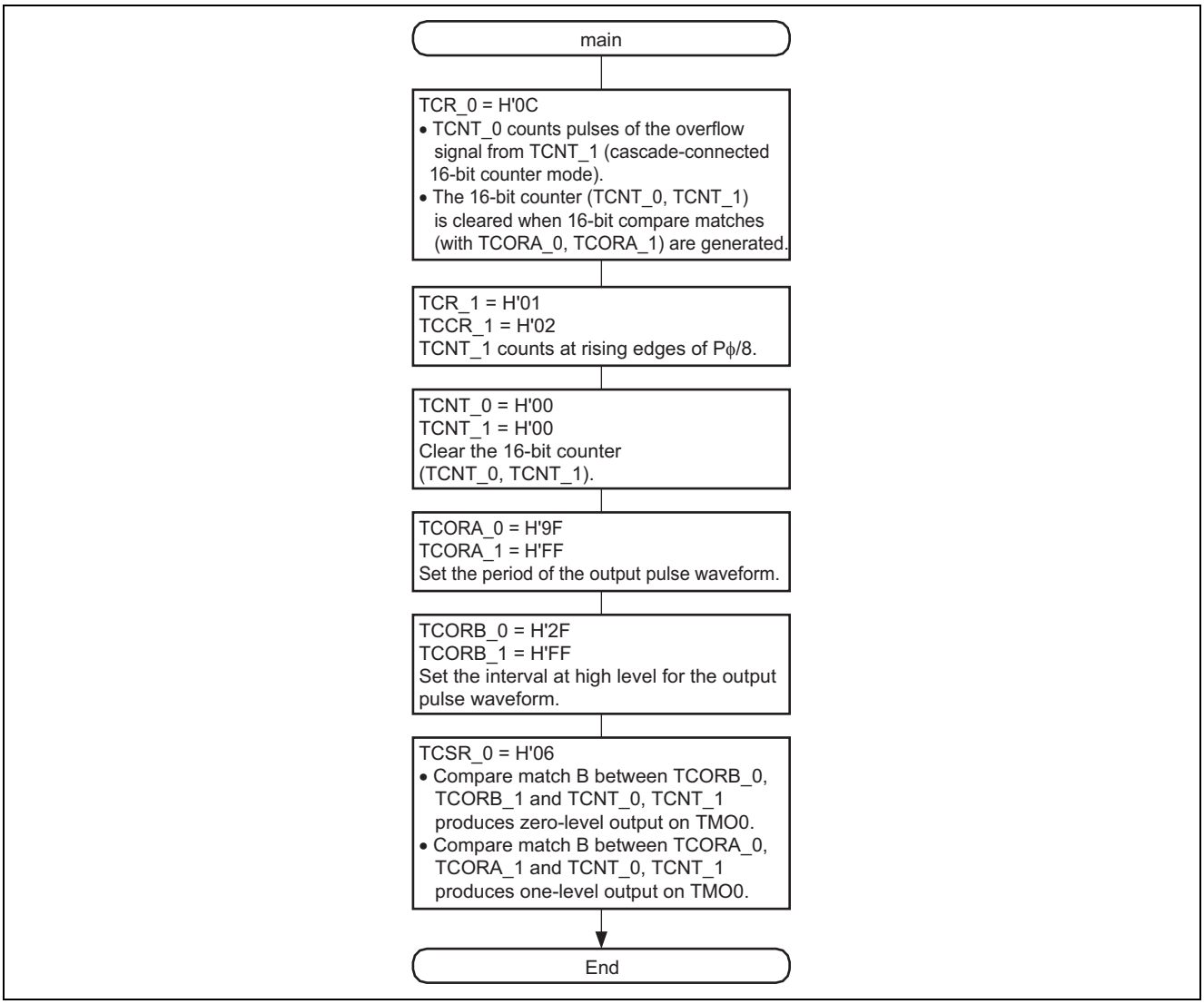
Table 8 Clock Signal Input to TCNT and Condition for Counting (for Units 0 and 1)

	TCR			TCCR		
	Bit 2	Bit 1	Bit 0	Bit 1	Bit 0	
Channel	CKS2	CKS1	CKS0	ICKS1	ICKS0	Description
TMR_0	0	0	0	—	—	Clock input disabled
	0	0	1	0	0	Input clock signal is Pϕ/8, count rising edges.
				0	1	Input clock signal is Pϕ/2, count rising edges.
				1	0	Input clock signal is Pϕ/8, count falling edges.
				1	1	Input clock signal is Pϕ/2, count falling edges.
	0	1	0	0	0	Input clock signal is Pϕ/64, count rising edges.
				0	1	Input clock signal is Pϕ/32, count rising edges.
				1	0	Input clock signal is Pϕ/64, count falling edges.
				1	1	Input clock signal is Pϕ/32, count falling edges.
	0	1	1	0	0	Input clock signal is Pϕ/8192, count rising edges.
				0	1	Input clock signal is Pϕ/1024, count rising edges.
				1	0	Input clock signal is Pϕ/8192, count falling edges.
				1	1	Input clock signal is Pϕ/1024, count falling edges.
	1	0	0	—	—	Count times the overflow signal from TCNT_1 is generated. *1
TMR_1	0	0	0	—	—	Clock input disabled
	0	0	1	0	0	Input clock signal is Pϕ/8, count rising edges.
				0	1	Input clock signal is Pϕ/2, count rising edges.
				1	0	Input clock signal is Pϕ/8, count falling edges.
				1	1	Input clock signal is Pϕ/2, count falling edges.
	0	1	0	0	0	Input clock signal is Pϕ/64, count rising edges.
				0	1	Input clock signal is Pϕ/32, count rising edges.
				1	0	Input clock signal is Pϕ/64, count falling edges.
				1	1	Input clock signal is Pϕ/32, count falling edges.
	0	1	1	0	0	Input clock signal is Pϕ/8192, count rising edges.
				0	1	Input clock signal is Pϕ/1024, count rising edges.
				1	0	Input clock signal is Pϕ/8192, count falling edges.
				1	1	Input clock signal is Pϕ/1024, count falling edges.
	1	0	0	—	—	Count times the compare-match A signal from TCNT_0 is generated. *1
Common	1	0	1	—	—	Count rising edges of the external clock signal. *2
	1	1	0	—	—	Count falling edges of the external clock signal. *2
	1	1	1	—	—	Count both rising and falling edges of the external clock signal. *2

Notes: *1 If the overflow of TCNT_1 is selected as the clock input for TMR_0 and the compare-match signal from TMR_0 is selected as the clock input for TMR_1, an up-counting clock will not be produced. Accordingly, do not make this setting

*2 If you are using the external clock, be sure to set the DDR bit to 0 and the ICR bit to 1 for the corresponding pin.

5. Flowchart


main
TCR_0 = H'0C
• TCNT_0 counts pulses of the overflow signal from TCNT_1 (cascade-connected 16-bit counter mode).
• The 16-bit counter (TCNT_0, TCNT_1) is cleared when 16-bit compare matches (with TCORA_0, TCORA_1) are generated.
TCR_1 = H'01
TCCR_1 = H'02
TCNT_1 counts at rising edges of Pϕ/8.
TCNT_0 = H'00
TCNT_1 = H'00
Clear the 16-bit counter (TCNT_0, TCNT_1).
TCORA_0 = H'9F
TCORA_1 = H'FF
Set the period of the output pulse waveform.
TCORB_0 = H'2F
TCORB_1 = H'FF
Set the interval at high level for the output pulse waveform.
TCSR_0 = H'06
• Compare match B between TCORB_0, TCORB_1 and TCNT_0, TCNT_1 produces zero-level output on TMO0.
• Compare match B between TCORA_0, TCORA_1 and TCNT_0, TCNT_1 produces one-level output on TMO0.
End

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Revision Record

		Description	
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