
CCE4502 Application Note

Abstract

The CCE4502 application note.

Contents

Abstract	1
Introduction	2
Example flow	2
Revision History	4

Introduction

The CCE4502 comprises a versatile frame handler for the IO-Link™ protocol as specified in the „IO-Link Interface and System“ Specification Version 1.1.2, July 2013.

The frame handler's functions include

- Status signaling via the STAT register and the SPI status byte
- Automatic CRC checking of the master message with indication via STAT register and the SPI status byte
- Automatic CRC generation and replacement in the CKS byte at the end of each device message
- Maskable interrupt flags for different timeouts, start of transmission, start of receiving, framebuffer level, and completed reception of a master message (see registers INT_EN_FH and INT_SRC_FH)
- Maskable interrupt flag for automatic wake-up request detection in SIO mode (see registers INT_EN_SIO and INT_SRC_SIO)
- Device message transmission with automatic timing based on COM mode configuration

Example flow

In the following example a flow is presented which uses the functionalities of the CCE4502 to reduce the complexity of the microcontroller unit (MCU) software. The flow can be altered to meet the needs of the application. We assume that the MCU is connected to the CCE4502 via SPI and is also connected to the INTX pin of the CCE4502.

After powering on the system the MCU should configure the CCE4502:

- Register CONF1: SIO mode, push-pull
- Registers FHC, TRSH: adapt to your requirements
- Register INT_EN_SIO: Enable WURQ detection interrupt by setting WURQ_EN

This will allow the CCE4502 to send an interrupt request (IRQ) when a wake-up request is detected. The configuration of the registers ODL, MPDL and DPDL are ignored for messages of type 0. Since the first messages from the master will be of type 0 the registers can be configured later during the configuration phase.

If a wake-up request is detected the interrupt service routine (ISR) of the MCU has to

- Re-configure the CONF1 register to the frame handler mode and the desired COM mode, and
- Enable the frame handler interrupts in register INT_EN_FH.

The device is now ready to receive and transmit messages using the frame handler. The message type registers (ODL, MPDL, DPDL) have to be configured during the configuration phase of the IO-Link communication to match the desired message type.

According to the M-sequence control (MC) octet and the message type registers the CCE4502 will automatically detect the start of receiving a master message and will indicate its end using the interrupt INT_SRC_FH.MSG. This should trigger an ISR in the MCU which reads the message from the buffer FHD and writes a proper device message to the buffer FHD, including the device CKS byte. The six least significant bits of the CKS byte are automatically replaced with the compressed checksum. Optionally, the frame handler state can be read from the STAT register or the SPI status byte to determine the results of the CRC check.

The example flow is depicted in Figure 1.

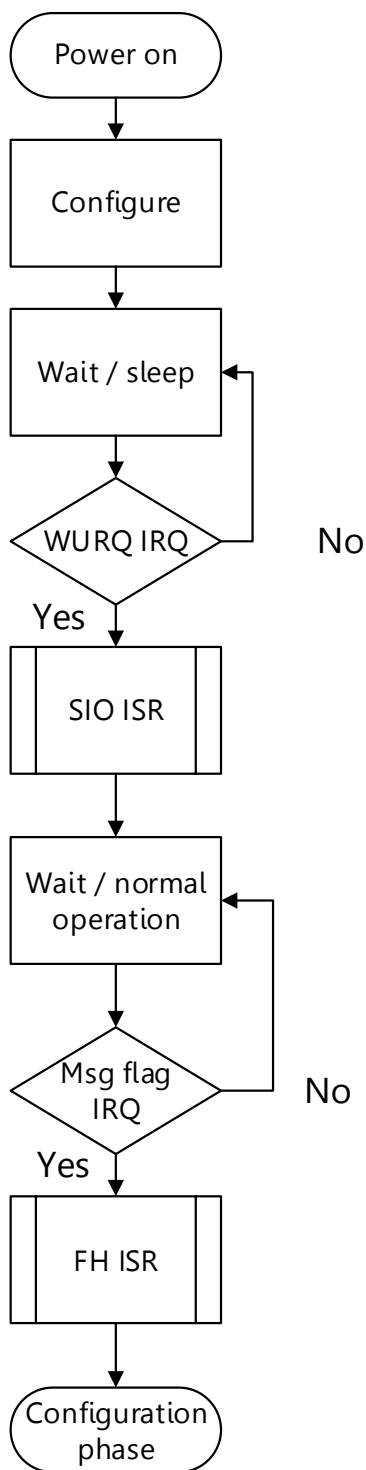


Figure 1: Example MCU flow in combination with the CCE4502

Revision History

Revision	Date	Description
1.3	29-Jan-2022	Rebrand
1.2	1-Nov-2019	Updated Template
1.1	09-Aug-2017	Clarified transition to configuration phase, message type configuration and CKS byte substitution
1.0	27-Jul-2017	Initial version

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.