ClockMatrix - Phase Noise Contributors

This application note explains the major contributors of phase noise for the ClockMatrix family of devices. The document discusses the clocking architecture and how phase noise is shaped depending on the loop architecture and the bandwidths chosen. It also provides the reader with an idea of how to optimize for the lowest phase noise in a certain integration bandwidth.

For more information, visit our website at ClockMatrix™ Timing Solutions.

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1. Introduction

Phase noise is always of interest in designs because customers set a maximum amount of noise (jitter/wander) given a certain integration bandwidth. For example, for an Ethernet application with an output frequency of 125MHz, the integration bandwidth is 12kHz to 20MHz. For a SONET application with an output frequency of 19.44MHz, the integration bandwidth is 12kHz to 5MHz. This means that within the integration bandwidth, the jitter must be optimized to be below a certain mask defined by network specifications.

Phase noise and jitter are different ways of quantifying the same phenomenon. They are just different representations of each other in a different domain. Phase noise (frequency domain) is just the noise power relative to the carrier at a particular offset, which is caused by the carrier sliding back and forth randomly. Jitter/wander (time domain) is variations of a digital signal's edge relative to the ideal edge. Phase noise can be converted to jitter and vice versa.

This document focuses mainly on phase noise. Phase noise from the device comes from many different sources, including:

- Output dividers (integer and DCO fractional divider), which set the noise floor for the device
- VCO noise
- Digital in-band noise (phase detector, charge pump, and loop filter)
- Input reference noise (SyncE or OCXO)
- XTAL noise

2. ClockMatrix Architecture

Figure 1 shows the noise model block diagram to be used in the phase noise analysis. The device can be viewed as a number of nested PLL loops. Each loop tracks its own reference and has its own loop bandwidth. Each successive loop has a lower loop filter bandwidth. All DPLL loop bandwidths are programmable.

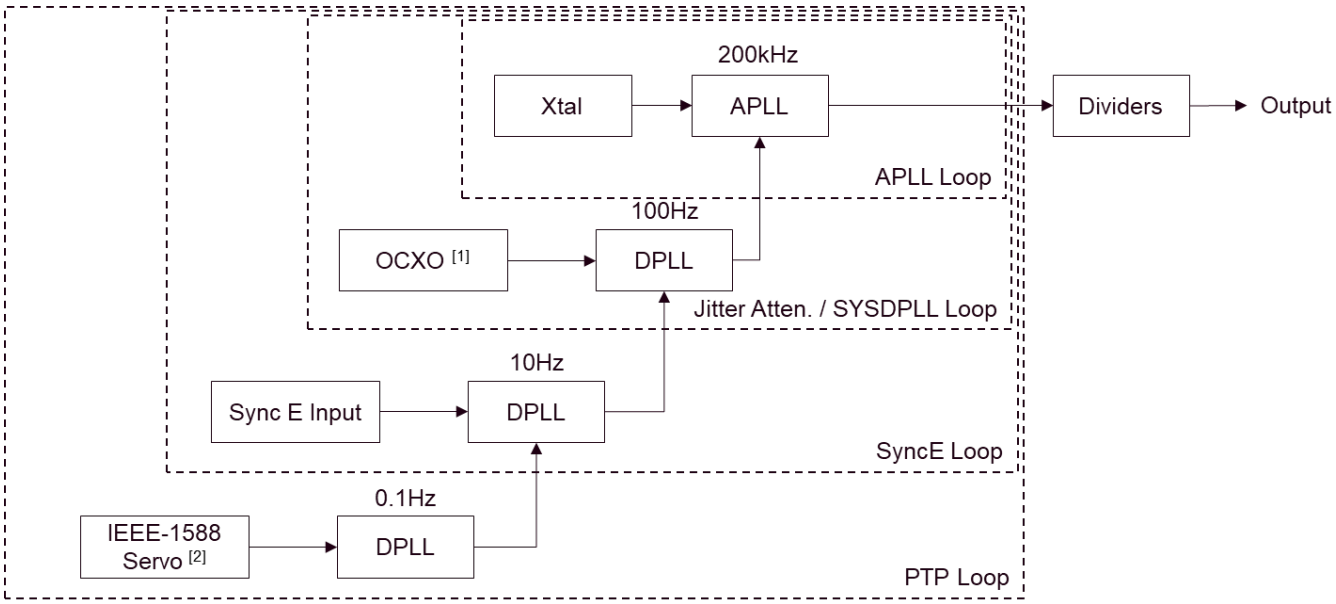

Figure 1. ClockMatrix Noise Model Block Diagram

Note 1: If the device is just a jitter attenuator, it would use a regular input reference.

Note 2: IEEE 1588 servo function is not located within the device, but still controls the inner loops.

Each loop will be broken down and analyzed from a phase noise point of view.

3. Phase Noise

3.1 External Sources

Each loop has an external input. The close-in phase noise, which is noise below the loop bandwidth, depends on the input source. As the number of nested loops increase, the input source also needs to become of higher quality especially at the low frequency offsets. The OCXO has a higher quality at low frequency offsets relative to the XTAL/XO. The SyncE source (PRC) has a higher quality relative to the OCXO. The PTP source (PRTC) has a higher quality relative to the SyncE source. Since the quality of the input is better after each successive nested loop, the loop bandwidth can be smaller after each successive loop.

In Figure 2, a TXC XO is compared to an SMA100B at 62.5MHz to analyze the purity of a typical XO versus a very clean signal generator with low phase noise. The close-in phase noise of the SMA100B is much better than the TXC XO. The plot represents actual measured data.

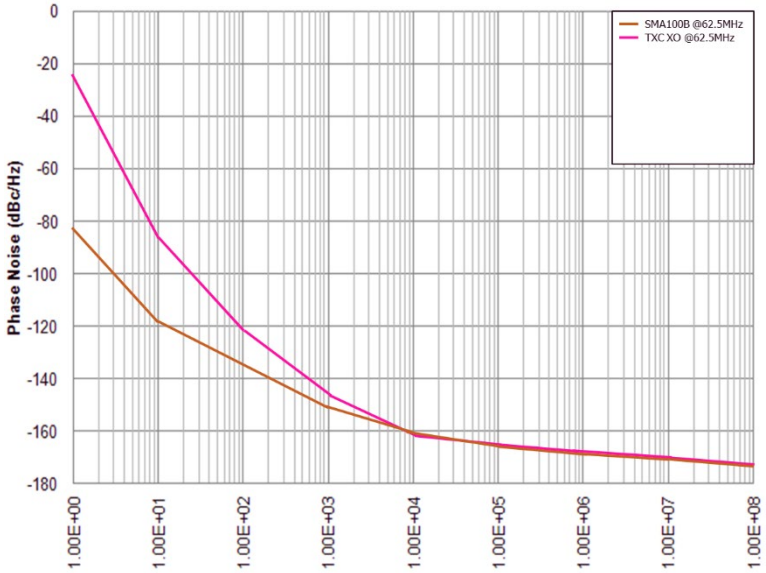

Figure 2. Input Reference Source: XTAL vs. SMA100B

In the region between 1Hz and 10Hz, often referred to as random walk FM noise, noise is very difficult to measure since it is close to the carrier and requires many sweeps at large intervals to average out the error. The slope is normally $1/f^4$. The SMA100B clearly has superior noise in this region.

In the region between 10Hz and 1kHz, flicker FM noise can be seen in the XO. The slope is roughly $1/f^3$. The SMA100B has a slope of roughly $1/f^2$ in this region.

After 10kHz, the phase noise approaches the thermal noise floor, which is called white PM noise.

The above indicates how the input source noise is very important in shaping the in-band phase noise. The following sections analyze each nested loop progressively. The plots represent idealized phase noise plots and do not represent actual data.

3.2 APLL Loop.

The simplest loop is the APLL Loop, which is shown in Figure 3. Output Divider and DCO noise defines the noise floor. The shape is flat across the band as shown in Figure 4. The exact value varies with output frequency. The higher the frequency, the higher the noise floor because phase noise increases by 6dB for every doubling of the carrier frequency. This is because 20log(N) is added, where N is the multiplication factor. In contrast, phase noise decreases by 6dB for every halving of the carrier frequency. The noise floor value shown below is for 983.04MHz. The noise floor cannot go below -174 dBc/Hz, which is the thermal noise floor limit.

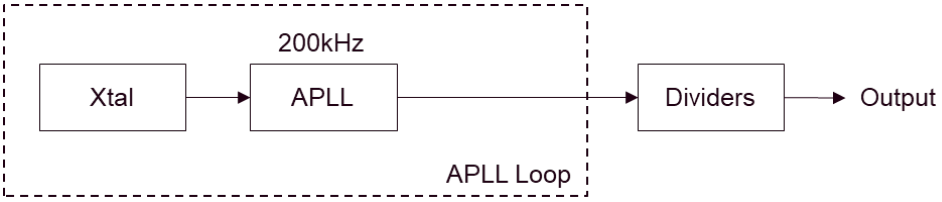

Figure 3. APLL Loop

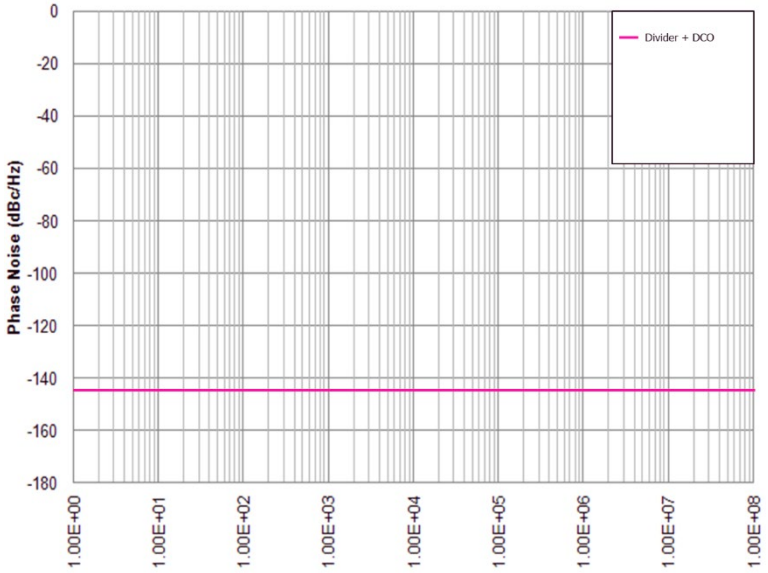

Figure 4. Output Divider and DCO Noise

Open Loop Analog PLL Noise is shown in Figure 5. Idealistic XTAL noise is modelled as -30dB/decade to 10kHz due to flicker noise. Then it is a flat line onwards. Idealistic analog VCO noise has a -20dB/decade slope. It does not roll-off to negative infinity but will be limited by the thermal noise floor in reality. Finally, analog in-band noise such as the phase detector, charge pump, and loop filter can be modeled as a flat line.

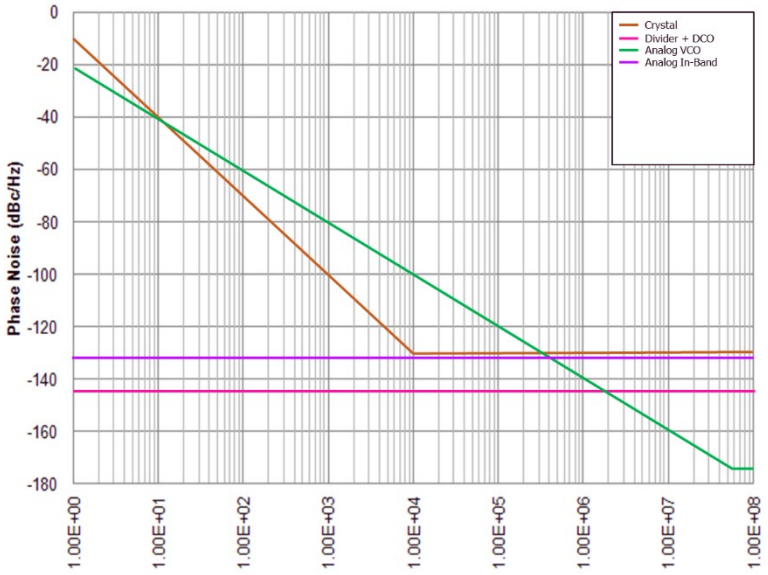

Figure 5. Open Loop Analog PLL Noise

Closing the APLL reshapes the noise as shown in Figure 6. The output dividers are after the APLL loop, so remain as a flat line. The in-band noise and the XTAL are shaped by a -20 dB/decade low-pass filter (forward path to positive terminal of phase detector) with a knee at the intrinsic PLL loop bandwidth. The loop filter can include an extra pole to increase the attenuation, but that is likely very far out to be visible. The VCO noise is shaped by a high-pass filter (return path to negative terminal of phase detector) by the same PLL loop bandwidth. The dashed lines show the noise in open-loop for reference. The intrinsic PLL loop bandwidth is set to 200kHz. The closed-loop plots do not go below the thermal noise floor of -174 dBc/Hz.

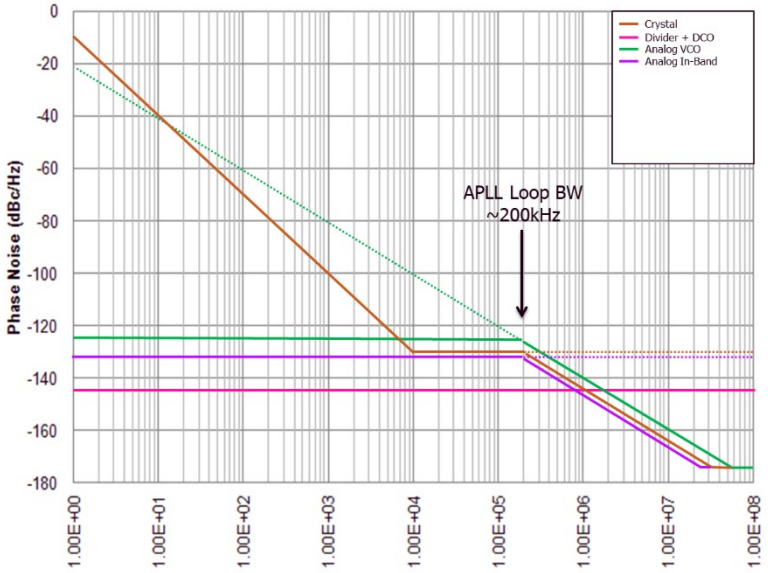

Figure 6. APLL Closed-Loop Noise

The resultant phase noise is shown in Figure 7. Phase noise is additive, so the most dominant noise at every frequency offset gives the overall phase noise plot.

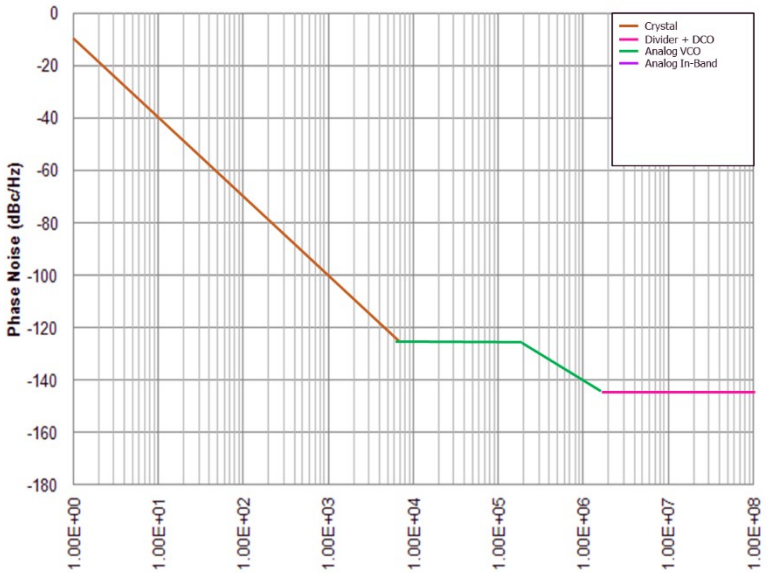

Figure 7. APLL Closed-Loop Resultant Noise

3.3 Jitter Attenuator/SYSDPLL Loop

Combining the APLL Loop with the SYSDPLL Loop is shown in Figure 8. The entire closed-loop APLL curve becomes the SYSDPLL open-loop VCO noise curve as shown in Figure 9. If an OCXO/TCXO does not exist, the SYSDPLL just becomes a regular DPLL jitter attenuator with a clock input. The phase noise analysis is done assuming an OCXO input.

The open-loop digital in-band noise from the DPLL is flat across the band, while the OCXO (input reference) is sloped twice until 1kHz.

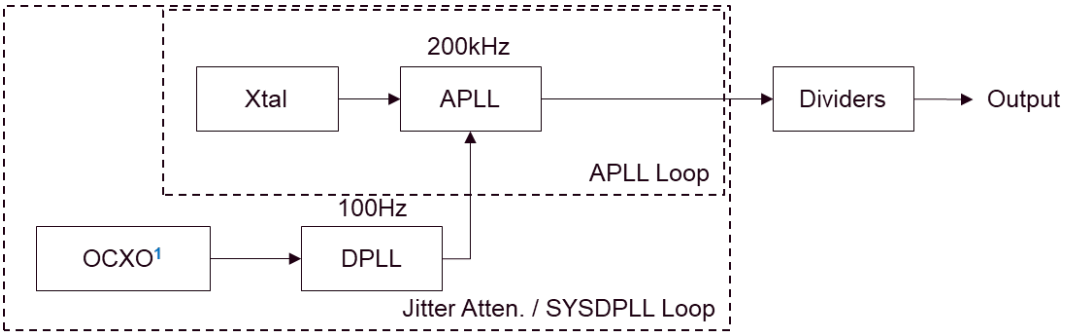

Figure 8. APLL Loop + Jitter Atten/SYSDPLL Loop

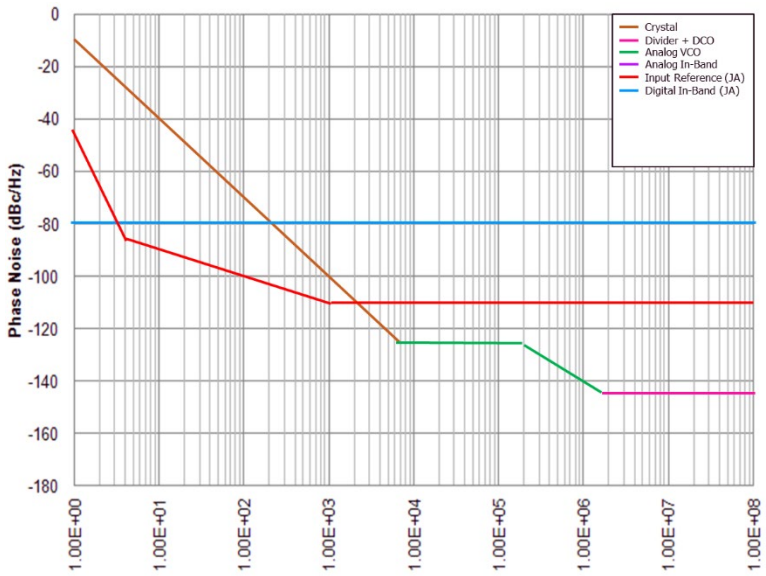

Figure 9. Digital Jitter Atten/SYSDPLL Open-Loop VCO Noise

Closing the SYSDPLL loop using a digital filter loop bandwidth (LBW) of 10Hz in the DPLL and including the APLL closed-loop noise gives the plots in Figure 10. The output dividers are still after the DPLL loop so remain flat across the band. The digital in-band noise and OCXO (input reference) are low-pass filtered at 10Hz because they are part of the forward path of the DPLL. The decimator also provides another pole further out. The VCO noise from the APLL is high-pass filtered because its noise is part of the return path of the DPLL. The closed-loop plots do not go below the thermal noise floor.

When the LBW is too low such as 10Hz, not enough of the VCO noise from the APLL is attenuated because of the high-pass filter at 10Hz. The digital in-band and OCXO noise are strongly attenuated.

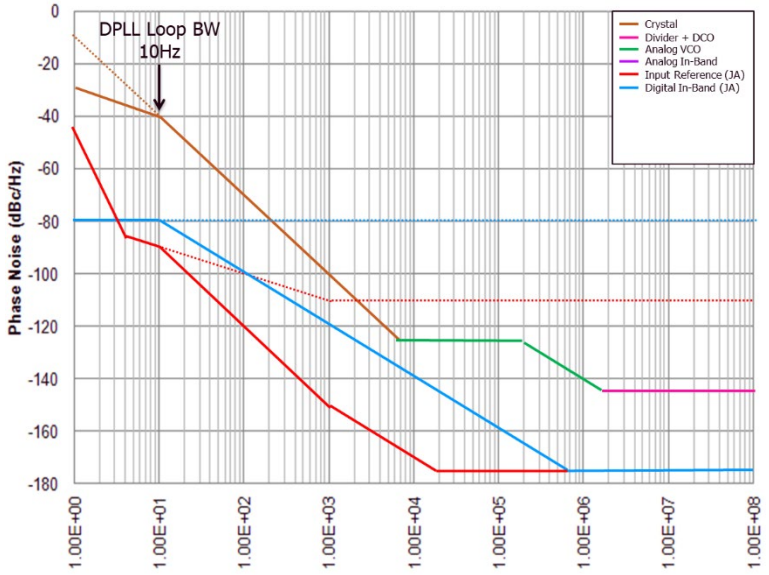

Figure 10. SYSDPLL Closed-Loop Noise Assuming a DPLL BW = 10Hz

When the LBW is too high such as 1kHz as shown in Figure 11, the VCO noise is strongly attenuated. However, the digital in-band and OCXO noise are not attenuated enough.

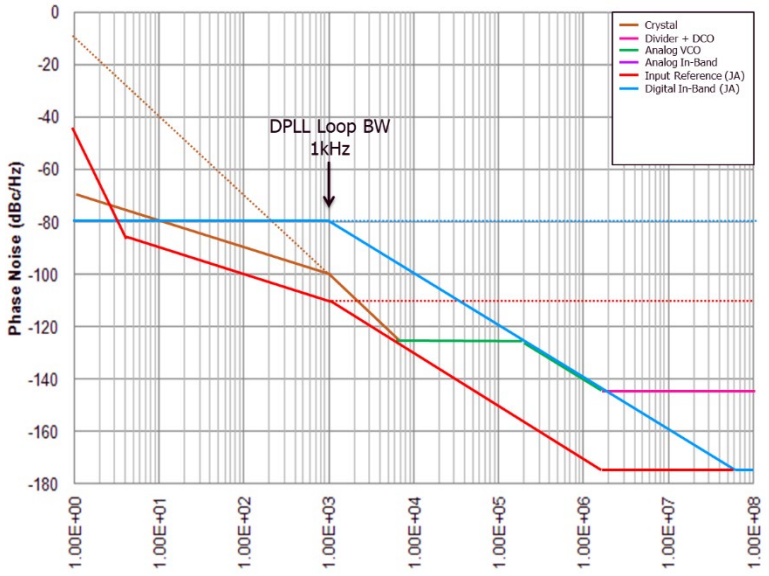

Figure 11. SYSDPLL Closed-Loop Noise assuming a DPLL BW = 1kHz

Figure 12 shows the LBW at 100Hz, which is a good compromise between attenuating VCO noise versus digital in-band noise plus OCXO noise.

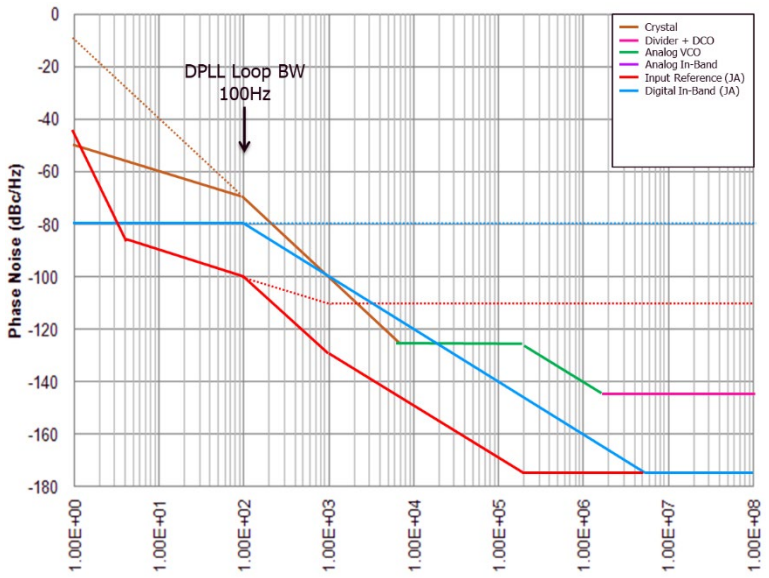

Figure 12. SYSDPLL Closed-Loop Noise Assuming a DPLL BW = 100Hz

Just showing the resultant SYSDPLL noise with nested APLL noise is shown in Figure 13.

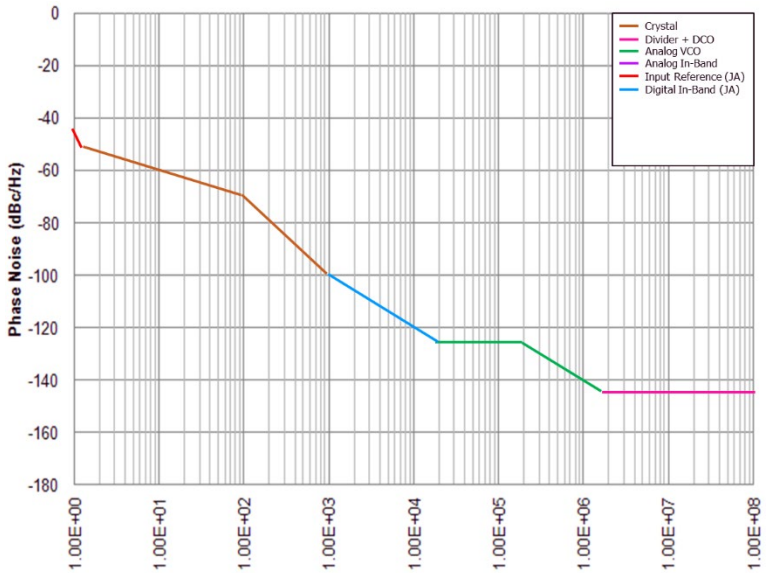

Figure 13. SYSDPLL Closed-Loop Resultant Noise

3.4 SyncE Loop

Combining the APLL Loop with the SYSDPLL Loop and the SyncE Loop is shown in Figure 14. Same analysis as before is done. The entire closed-loop APLL curve and the closed-loop SYSDPLL curve become the SyncE DPLL open-loop VCO noise curve as shown in Figure 15.

The SyncE open-loop digital in-band noise from the DPLL is again flat across the band, while the SyncE input noise has a zero at 1kHz, a pole at 30kHz, and a zero at 1MHz. The SyncE noise source is shaped like a traditional DPLL output noise source.

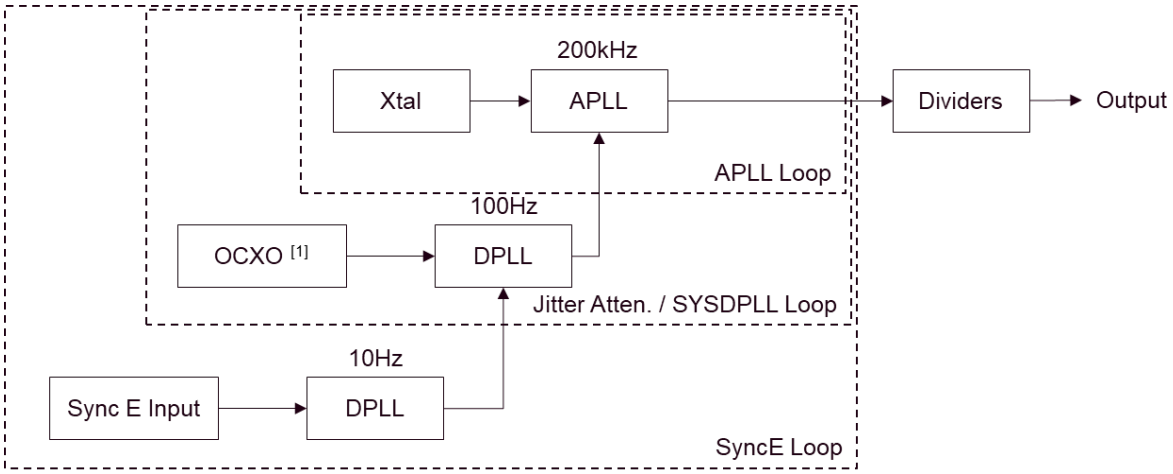

Figure 14. APLL Loop + Jitter Atten/SYSDPLL Loop + SyncE Loop

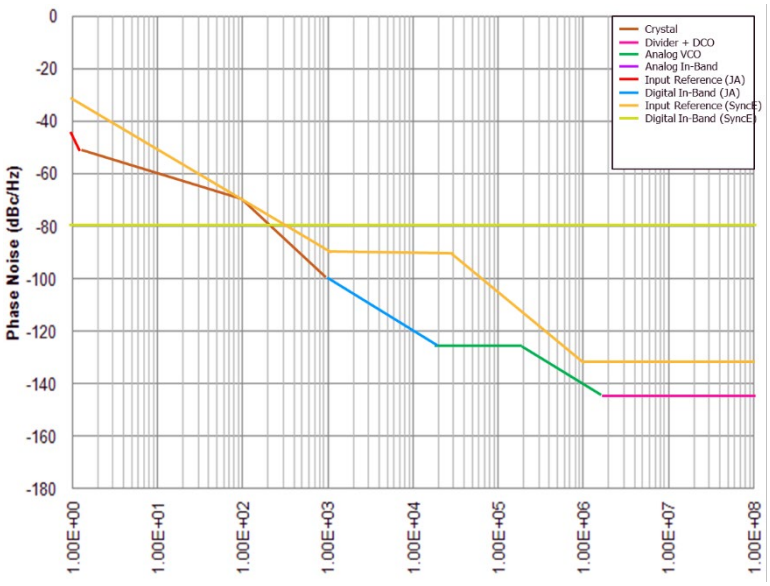

Figure 15. SyncE DPLL Open-Loop VCO Noise

Closing the SyncE loop using a digital filter LBW of 10Hz in the DPLL and including the closed-loop noise from the other two nested loops gives the plots in Figure 16. The digital in-band noise and SyncE input are low-pass filtered at 10Hz because they are part of the forward path of the DPLL. The noise from the other two nested loops is high-pass filtered at 10Hz because its noise is part of the return path of the SyncE DPLL. The closed-loop plots do not go below the thermal noise floor.

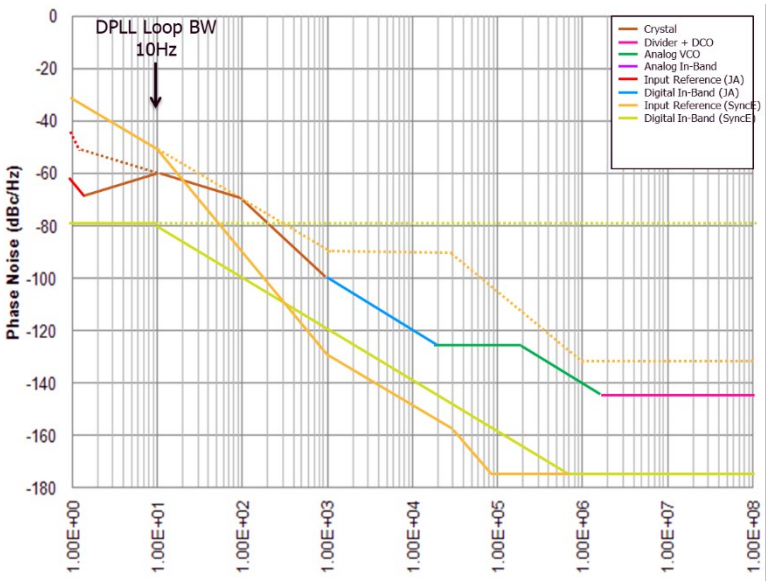

Figure 16. SyncE DPLL Closed-Loop Noise Assuming a DPLL BW = 10Hz

Just showing the resultant SyncE DPLL noise with noise from the other two nested loops is shown in Figure 17. Additional high-pass filtering effect due to the 10Hz LBW in the SyncE DPLL removes jitter attenuator input (OCXO) noise. The XTAL noise is still present in the mid-band. The close in noise is dominated by the SyncE input reference noise.

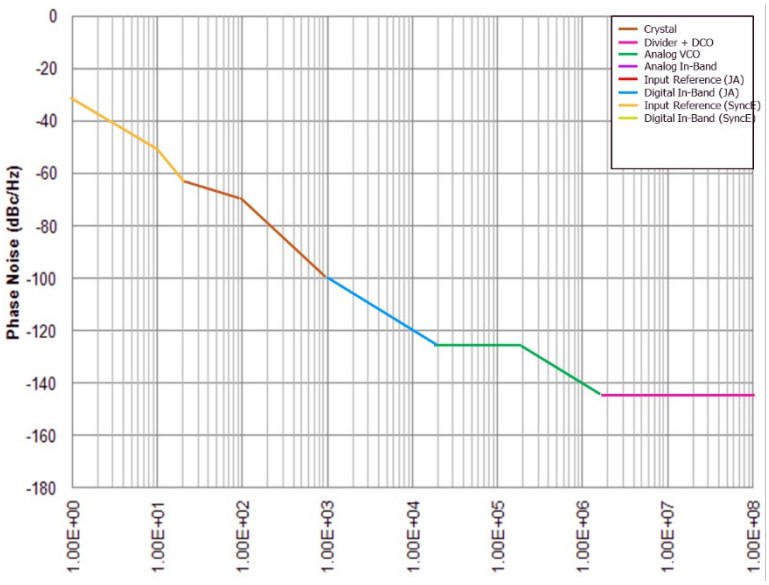

Figure 17. SyncE DPLL Closed-Loop Resultant Noise

3.5 PTP (1588) Loop

Combining all four loops is shown in Figure 1. The entire closed-loop APLL curve, the closed-loop SYSDPLL curve, and the closed-loop SyncE DPLL curve become the PTP DPLL open-loop VCO noise curve.

The PTP loop is closed externally by a host. The LBW is normally 0.1Hz for G.8273.2. Closing the PTP loop and including the closed-loop noise from the other three nested loops gives the plots in Figure 18. The closed-loop plots do not go below the thermal noise floor.

For digital IEEE 1588 (PTP) PLL, an external host (software) is used to lock the IEEE-1588 packet clocks. The in-band or reference noise cannot be predicted. The SyncE input noise is high-pass filtered at 0.1Hz because its

noise goes to the PTP return path (external). The IEEE 1588 input noise and the digital in-band noise are low-pass filtered at 0.1Hz because their noise go to the PTP forward path.

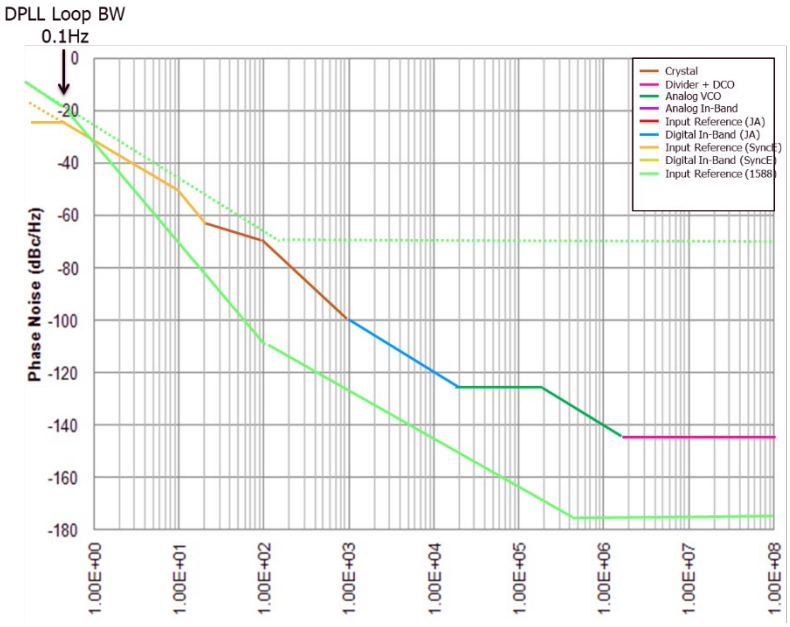

Figure 18. PTP DPLL Closed-Loop Noise Assuming a BW = 0.1Hz

Just showing the resultant PTP DPLL noise with noise from the other three nested loops is shown in Figure 19. For the PTP DPLL, the SyncE noise only affects the output noise within a narrow range between 1Hz and 20Hz. The IEEE 1588 input noise and the digital in-band noise only affect the output noise at very low frequency offsets (< 1Hz).

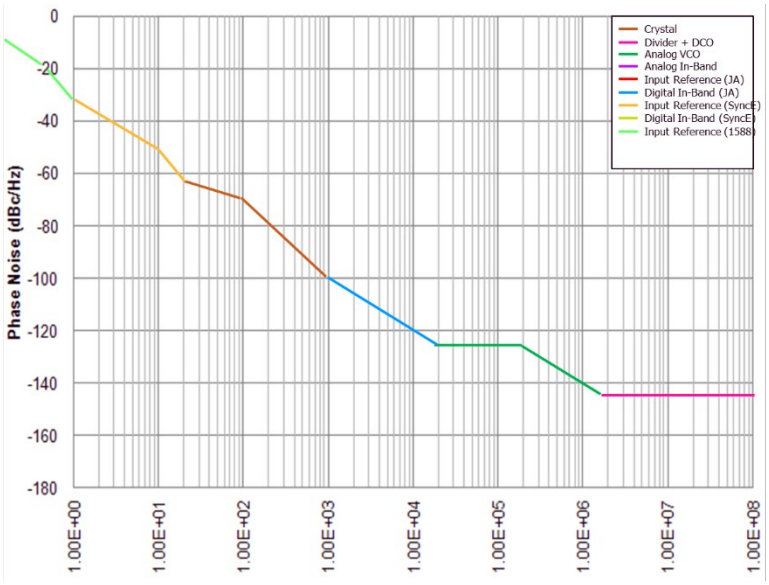

Figure 19. PTP DPLL Closed-Loop Resultant Noise

3.6 Gain Peaking

Although a PLL attenuates phase noise in the stopband, there is also a small amplification in the passband as shown in Figure 20. This amplification is called gain peaking. It can be controlled by adjusting the damping constant of the PLL loop filter for a single PLL. However, several nested loops can compound the issue by causing gain upon gain which could reduce the PLL phase margin and thereby cause the loop to become unstable. Network specifications also limit the amount of gain peaking allowed.

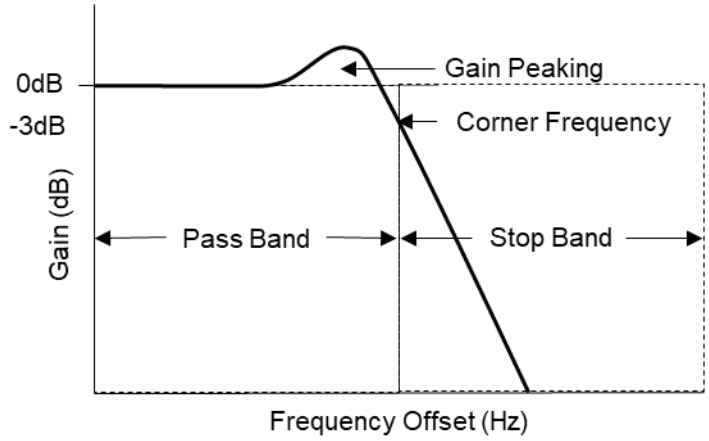

Figure 20. PLL Filter Plot

There are ways to mitigate the effect of gain peaking. The first, as mentioned, is adjusting the damping constant. An underdamped system will oscillate but converge very quickly. An overdamped system will move slowly toward equilibrium but will not oscillate. The second is to stagger the filter loop bandwidth of every successive nested loop such that the gain is not overlapped, which is done in the architecture as stated in Section 2.

4. How External Sources are Affected

4.1 XTAL Noise Transfer Function to Output

- Affected by low-pass filter at APLL loop bandwidth of 200kHz
- Affected by SYSDPLL loop bandwidth as a high-pass filter at 100Hz
- Affected by SyncE DPLL loop bandwidth as a high-pass filter at 10Hz
- Affected by PTP IEEE-1588 DCO filter bandwidth as a high-pass filter at 0.1Hz

The entire transfer function is shown in Figure 21.

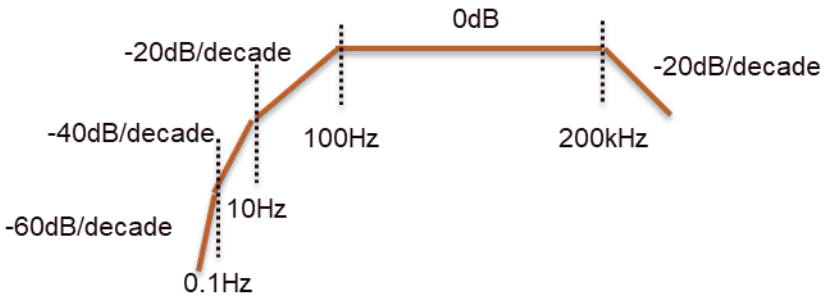

Figure 21. XTAL Noise Transfer Function to Output

4.2 OCXO Input Reference Noise Transfer Function to Output

- Affected by low-pass filter at jitter attenuator PLL loop bandwidth of 100Hz
- Affected by SyncE DPLL loop bandwidth as a high-pass filter at 10Hz
- Affected by IEEE-1588 DCO filter bandwidth as a high-pass filter at 0.1Hz

The entire transfer function is shown in Figure 22.

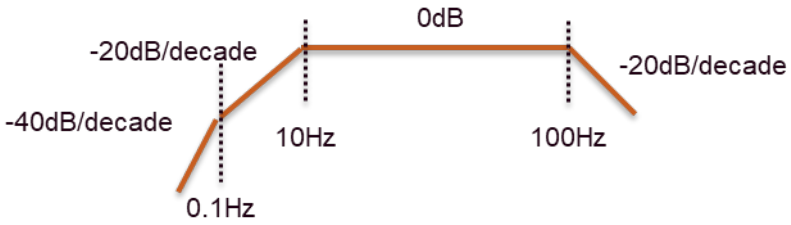

Figure 22. OCXO Input Reference Noise Transfer Function to Output

4.3 SyncE Input Reference Noise Transfer Function to Output

- Affected by low-pass filter at SyncE PLL loop bandwidth of 10Hz
- Affected by IEEE-1588 DCO filter bandwidth as a high-pass filter at 0.1Hz

The entire transfer function is shown in Figure 23.

Figure 23. SyncE Input Reference Noise Transfer Function to Output

4.4 IEEE-1588 External PLL Noise Transfer Function to Output

- Affected by low-pass filter at IEEE-1588 write-phase DCO filter at 0.1Hz

The transfer function is shown in Figure 24.

Figure 24. IEEE 1588 External PLL Noise Transfer Function to Output

5. Revision History

Revision	Date	Description
1.00	Mar 28, 2022	Initial release.

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