Application Note

Applying GreenFET Load Switches in Power-splitting Applications

AN-CM-260

Abstract

This application note describes some solutions of power splitter design using the GreenFET load switches, showing advantages and disadvantages of each solution. Schematics and operation waveforms are provided as well.

Contents

Figures

1 Terms and Definitions

OVP	Over-voltage protection
OCP	Over-current protection
OVLO	Over-voltage lockout
PCB	Printed circuit board

2 References

[1] SLG59H1313C, Datasheet
[2] SLG59H1008V, Datasheet
[3] SLG59H1006V, Datasheet
[4] SLG59H1302C, Datasheet
[5] AN-1068, GreenFET and High Voltage GreenFET Load Switch Basics

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3 Introduction

The design of modern electronics has become ever more demanding. These systems require higher power delivery, more components in smaller PCBs, reduced power consumption, etc. In many of these modern systems, power rails need to be switched on and off depending on load and input voltage levels. Oftentimes, it is important to have the ability to accommodate multiple input voltages for an output while offering one or more system-level protection features. Some of these protection features include: input or output over-voltage protection (OVP), over-current protection (OCP), high input voltage tolerance, and surge protection. Monolithic power splitter ICs can be used in systems with multiple input voltages and, in this application note, we will describe some power splitter solutions using the GreenFET load switches.

4 Using the SLG59H1313C and the SLG59H1008V in Power-splitting Applications

The SLG59H1313C [1] is a feature-rich, 23 mΩ RDS_{ON} nFET load switch that protects operating systems against voltage faults up to 29 Vdc. An internal clamp circuit protects the downstream components from surge voltage up to 100 V. The SLG59H1313C features a fast 50 ns (typ) over-voltage response time that turns off the internal nFET if the input voltage exceeds the OVP threshold. The OVP threshold is adjustable with optional external resistors to any voltage between 4 V and 20 V. Over-temperature protection powers down the device at 145°C (typ). SLG59H1313C also features an over-current protection that turns off the switch if the current exceeds 7 A (typ), this gives additional protection from over-heating the device. SLG59H1313C incorporates an open-drain Power-is-Good (PG) digital output pin. When $V_{IN\_min} < V_{IN} < V_{OVLO}$ and the switch is on, the PG will be driven low indicating a good power input, otherwise, this digital output is high impedance.

The SLG59H1008V [2] is another feature-rich, high-performance 13.3 mΩ RDS_{ON} nFET load switch designed to control 12 V or 24 V power rails up to 4 A. Using a proprietary MOSFET design, the SLG59H1008V achieves a stable 13.3 mΩ RDS_{ON} across a wide input voltage range. In combining novel FET design and copper-pillar interconnects, the SLG59H1008V package also exhibits a low thermal resistance for high-current operation.

Connecting and configuring these two GreenFET load switches as shown in Figure 1, a high-performance power splitter with the ability to select an output power rail depending on input voltage level can be achieved. For example, the SLG59H1313C was configured to operate for a 5 V input voltage range by connecting an external resistor divider to the OVLO pin (Figure 1) [1]. The SEL pin of SLG59H1008V selects one of two undervoltage/overvoltage lockout windows. When SEL = LOW, its V_{IN} undervoltage/overvoltage lockout is set for 12 V ±10% applications [2] and if SEL = HIGH, its V_{IN} undervoltage/overvoltage lockout is set for 24 V ±10% applications [2]. In our example, the SLG59H1008 is configured for 12 V operation. The sequencing of the two ICs is executed by the SLG59H1313C's PG signal to the SLG59H1008V's ON pin.

When a 5 V input voltage appears at the V_{IN} pin of the SLG59H1313C, its PG becomes asserted high. After a 15 ms delay, this load switch closes its internal nFET switch and the voltage appears at V_{OUT1} (Figure 2). The voltage at V_{OUT2} remains 0 V because of SLG59H1008V's undervoltage lockout feature [2]. When V_{OUT1} reaches its steady-state value, SLG59H1313C's PG becomes asserted low and turns off the SLG59H1008V.

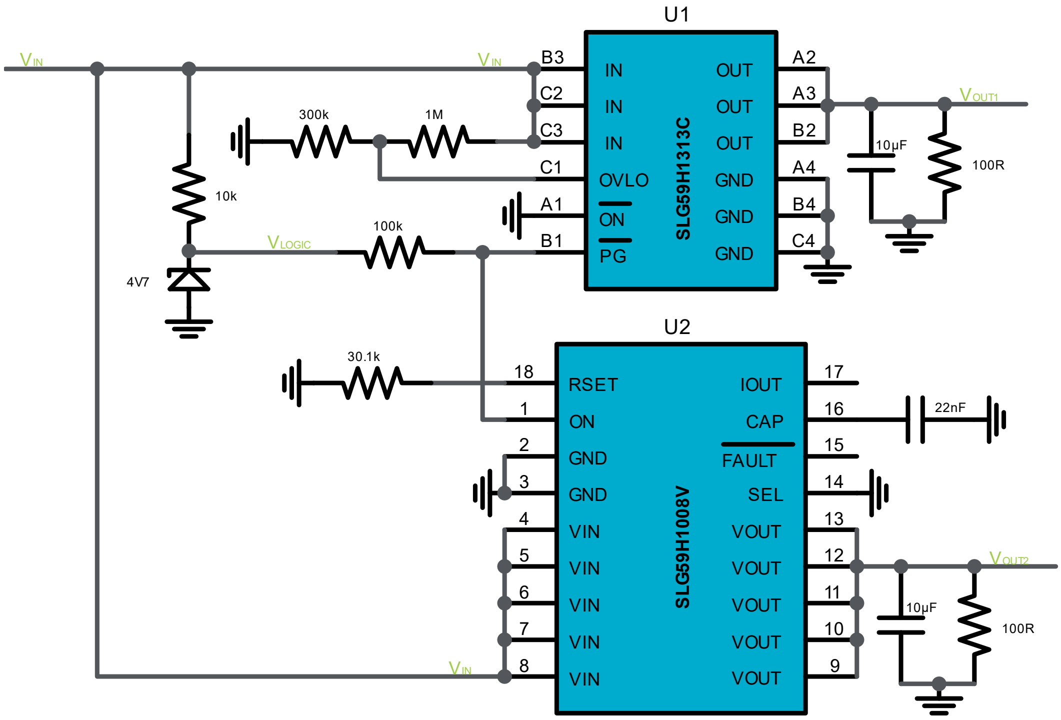

Figure 1: A schematic of a power splitter using SLG59H1313C and SLG59H1008V GreenFET Load Switches

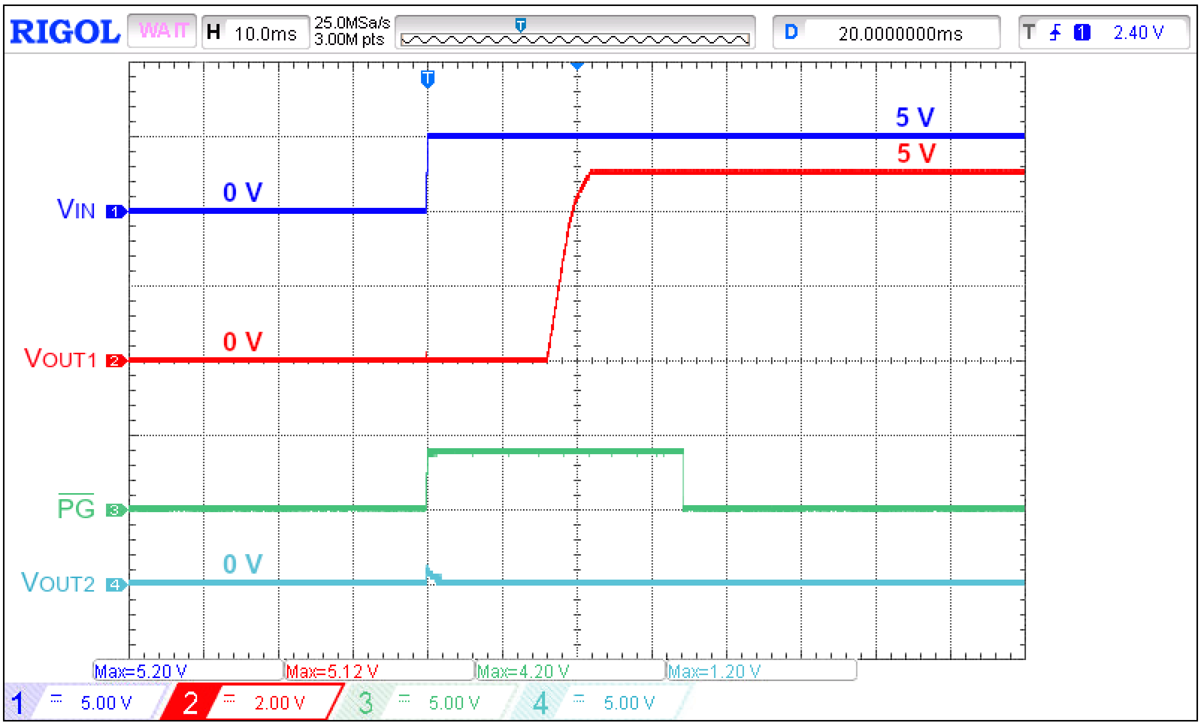

Figure 2: 5 V power splitter operation using SLG59H1313C and SLG59H1008V GreenFET Load Switches

If 12 V initially is applied at V_{IN}, the SLG59H1313C's overvoltage protection is triggered where the voltage doesn't appear at V_{OUT1}. Its PG output becomes asserted high which turns on the SLG59H1008V, hence, 12 V now appears at V_{OUT2} (please see Figure 3). Such a design allows to select an output power rail depending on the voltage level at the input common to both ICs. Illustrated in Figure 4 is the transition from 5 V to 12 V. As can be observed, when V_{IN} is higher than the SLG59H1313C's OVLO level, it is switched off and its PG is asserted high, closing SLG59H1008V's nFET switch. Thus, 12 V appears at V_{OUT2}. The reverse transition from 12 V to 5 V is illustrated in Figure 5. In Figure 6 and Figure 7, the transitions from 12 V to 0 V and from 5 V to 0 V, respectively, are illustrated.

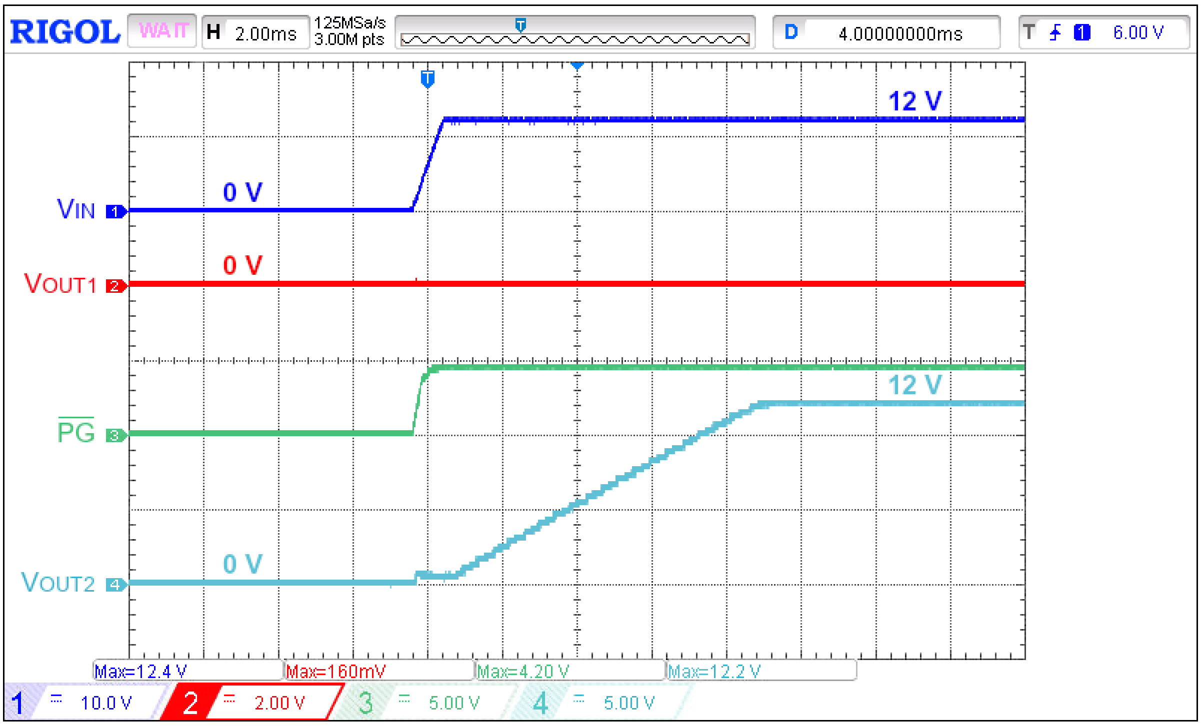

Figure 3: 12 V power splitter operation using SLG59H1313C and SLG59H1008V GreenFET Load Switches

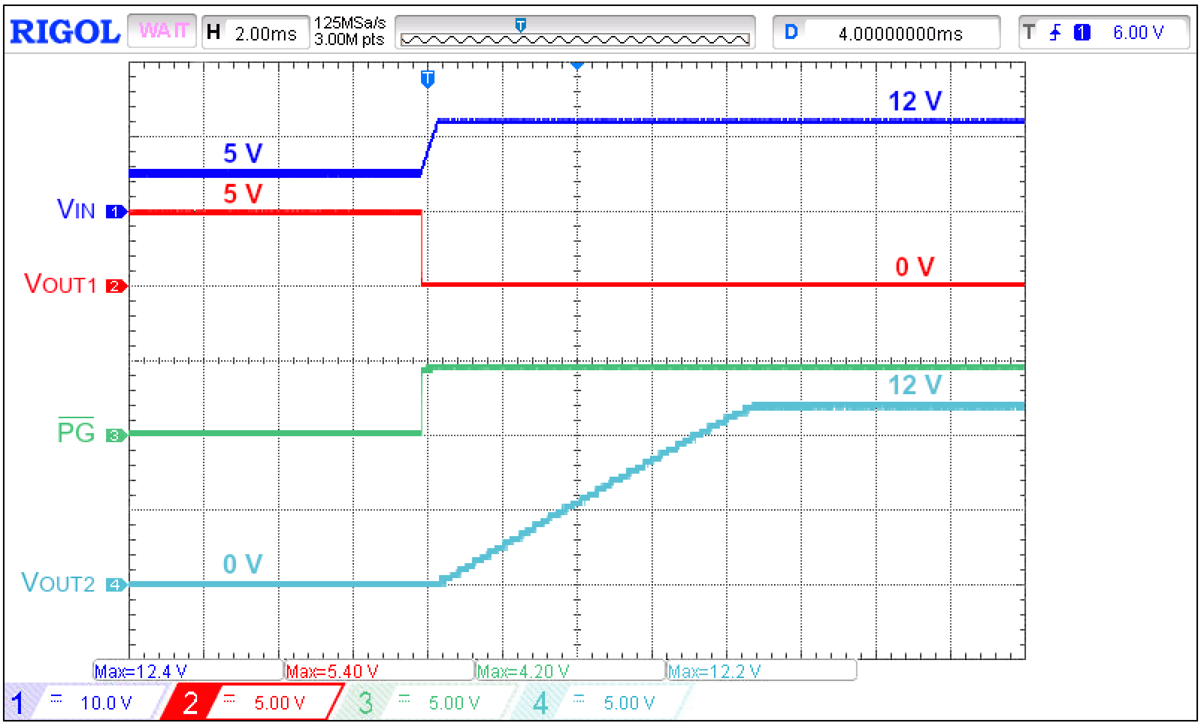

Figure 4: 5 V to 12 V power splitter transition operation using SLG59H1313C and SLG59H1008V GreenFET Load Switches

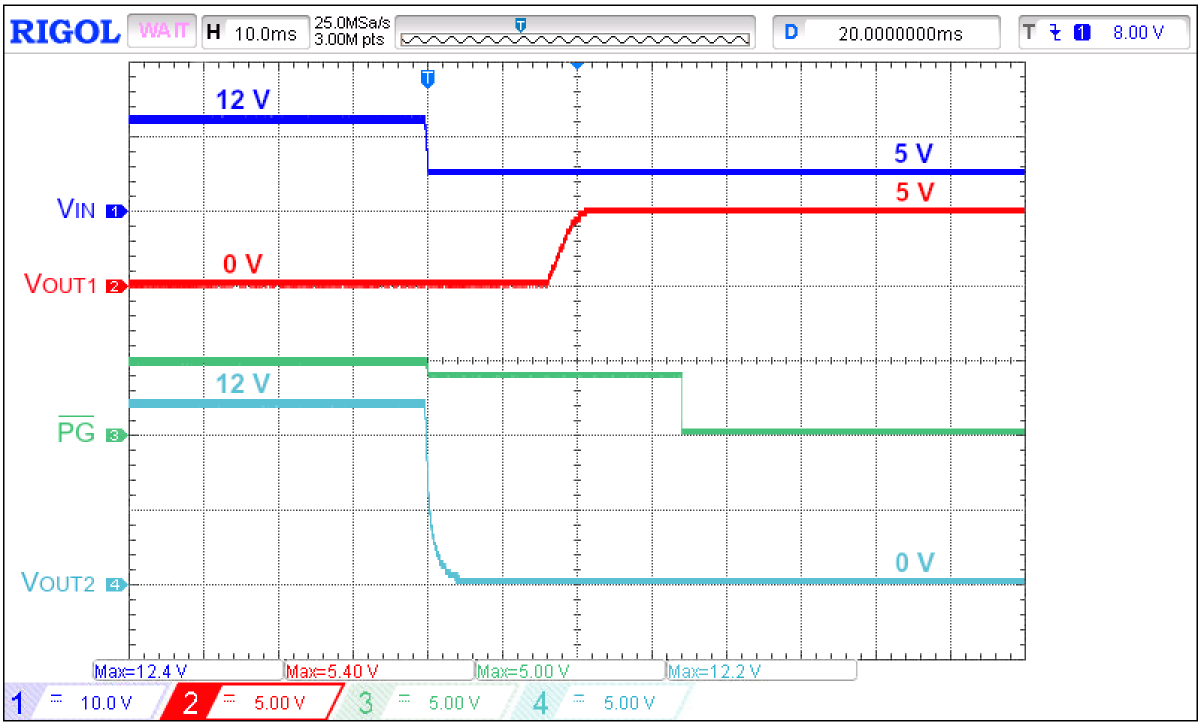

Figure 5: 12 V to 5 V power splitter transition operation using SLG59H1313C and SLG59H1008V GreenFET Load Switches

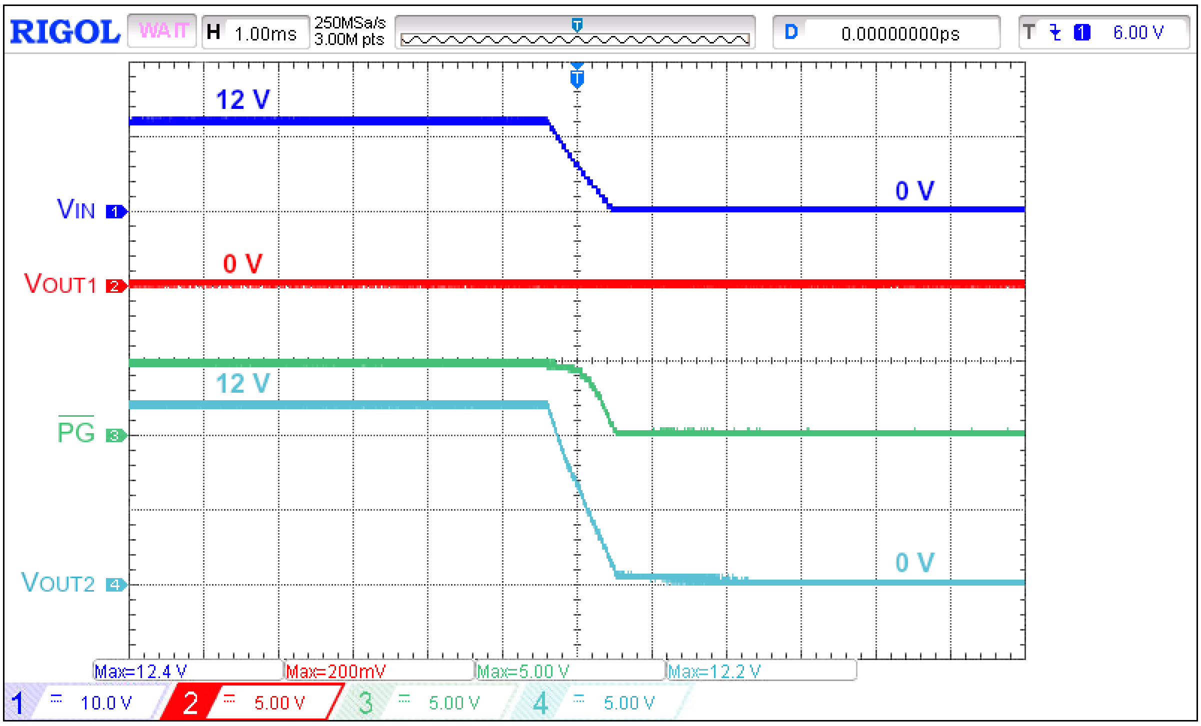

Figure 6: 12 V to 0 V power splitter transition operation using SLG59H1313C and SLG59H1008V GreenFET Load Switches

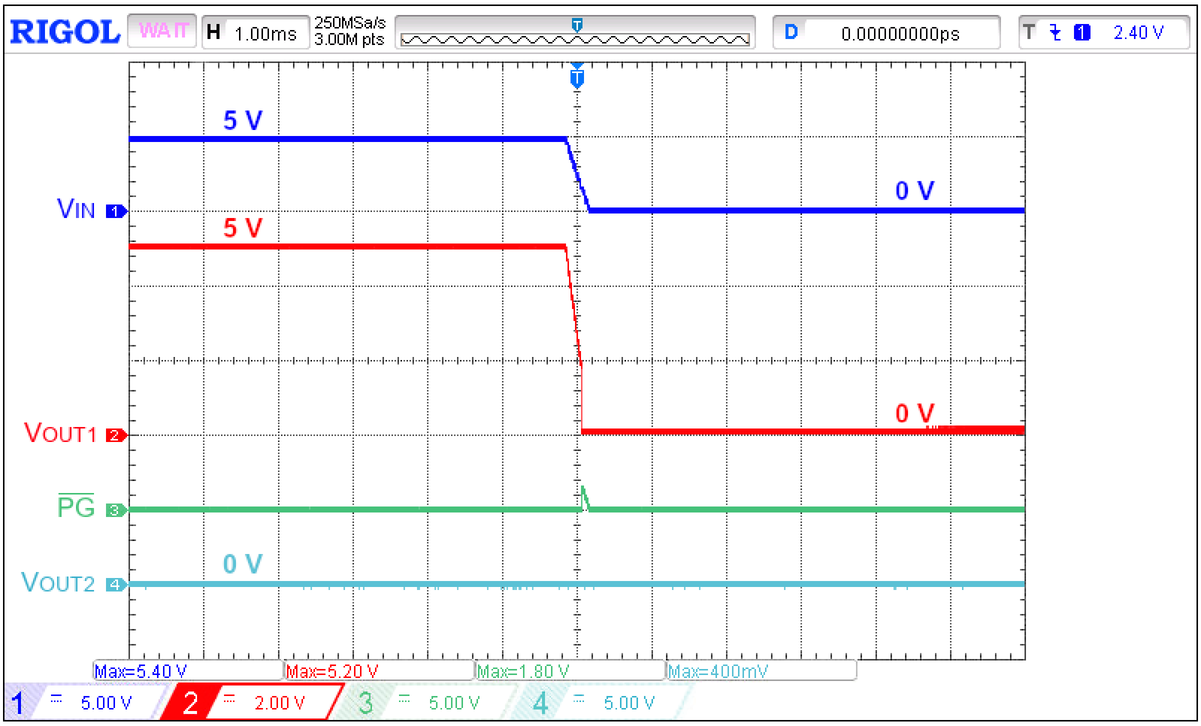

Figure 7: 5 V to 0 V power splitter transition operation using SLG59H1313C and SLG59H1008V GreenFET Load Switches

Keeping the SLG59H1313C in its OVLO state means that its power consumption is higher than it would be in its OFF state. Power consumption can be reduced by turning off the SLG59H1313C while SLG59H1008V's nFET is closed. This operating mode can be enabled by adding a voltage divider at V_{OUT2} and connecting the resistive-divider's tap directly to the SLG59H1313C's ON pin. This schematic is illustrated in Figure 8. The behavior of such design remains the same, however, the power consumption of SLG59H1313C is decreased from 165 μA to 150 nA when V_{IN} = 12 V.

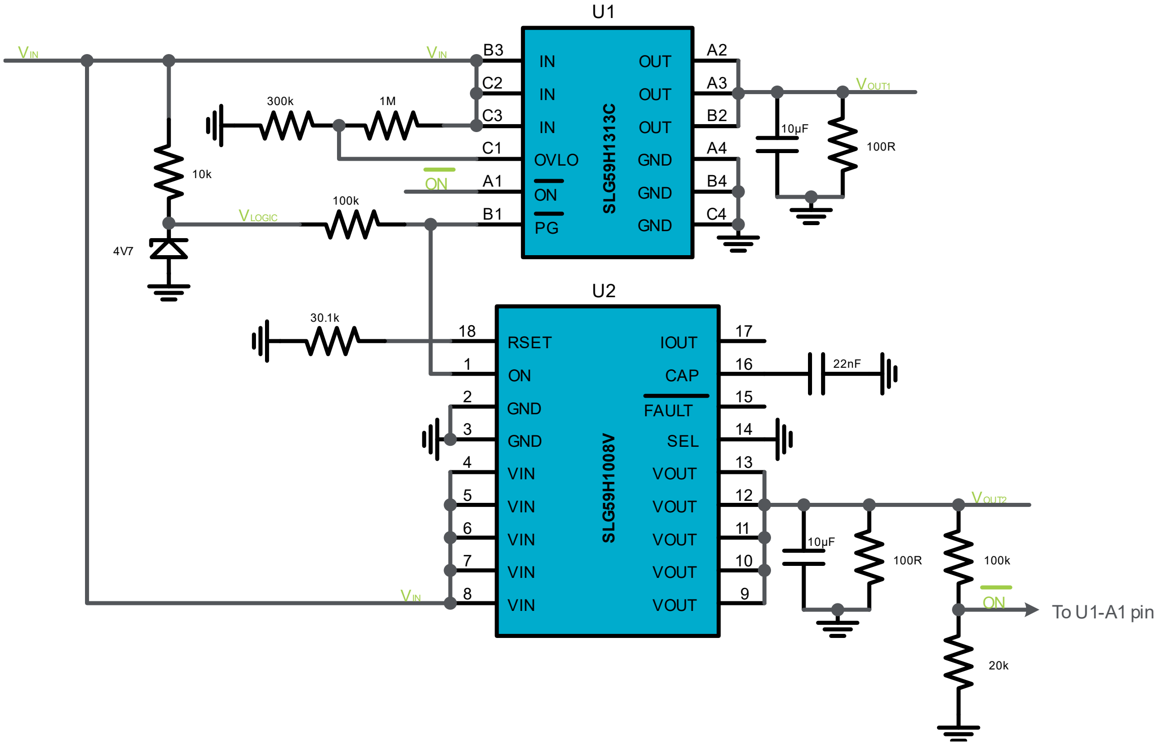

Figure 8: A SLG59H1313C and SLG59H1008 connection to decrease power consumption when V_{IN} = 12 V

5 Using the SLG59H1313C and the SLG59H1006V in Power-splitting Applications

In the previous design, the SLG59H1008V was configured to control 12 V or 24 V power rails. Optionally, a SLG59H1006V [3] can be used in its place as the SLG59H1006V provides a 4-Level V_{IN} Overvoltage Lockout feature enabled via two pins. Like the SLG59H1008V, the SLG59H1006V is a high-performance, self-powered 13.1 mΩ nFET load switch designed for all 4.5 V to 22 V power rails up to 5 A. Using a proprietary MOSFET design, the SLG59H1006V achieves a stable 13.1 mΩ RDS_{ON} across a wide input voltage range. The SLG59H1006V package also exhibits a low thermal resistance for high-current operation.

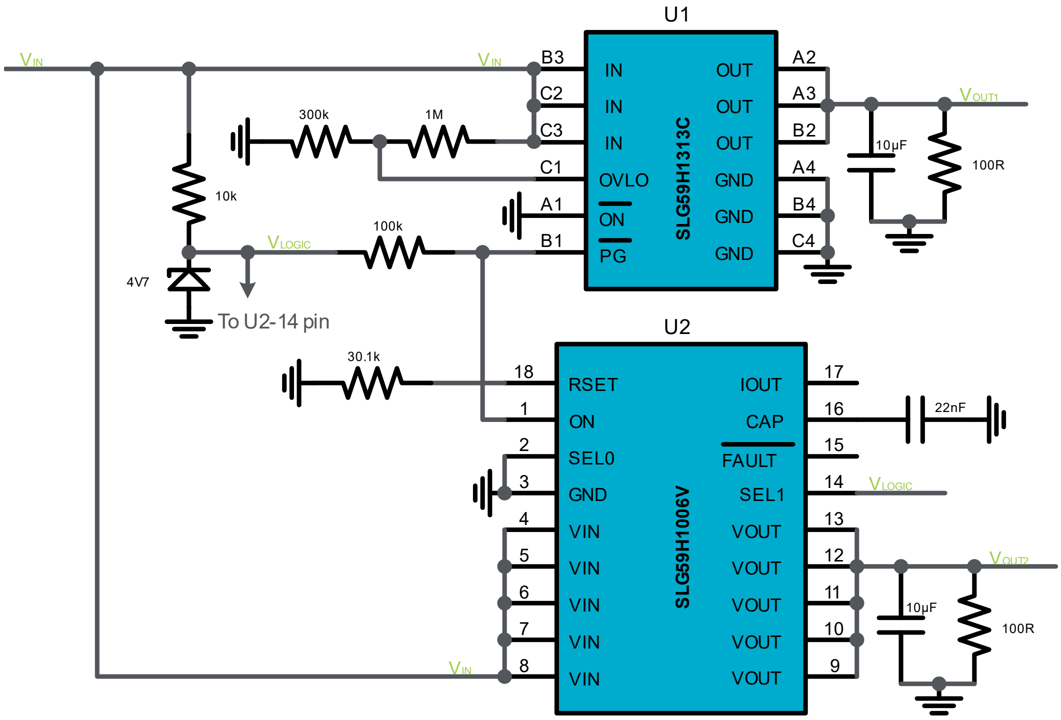

Figure 9: A schematic of a power splitter using SLG59H1313C and SLG59H1006V GreenFET Load Switches

In Figure 9, the SLG59H1313C remains configured for 5 V input voltages. The SEL0 and SEL1 pins of SLG59H1006V select one of four V_{IN} overvoltage lockout thresholds. When SEL0 = LOW and SEL1 = HIGH, its V_{IN} overvoltage lockout threshold is set to 14.4 V [3].

When a 5 V input voltage is applied at V_{IN}, the SLG59H1313C's PG becomes asserted high. Because PG is connected to the SLG59H1006V's ON pin and its undervoltage lockout is 3.8 V max, the SLG59H1006V turns on and voltage appears at V_{OUT2} as well (please see Figure 10). After a 15 ms delay, the SLG59H1313C's internal nFET is closed and the voltage now appears at V_{OUT1}. When the voltage at V_{OUT1} has reached its steady-state value, the SLG59H11313C's PG becomes asserted low and turns off the SLG59H1006V (V_{OUT2}).

When 12 V appears at V_{IN}, the SLG59H1313C's PG becomes asserted high and turns on the SLG59H1006V - 12 V now appears at V_{OUT2} (please see Figure 11). The PG output remains asserted high because of theSLG59H1313C overvoltage protection feature, preventing V_{IN} to appear at V_{OUT1}. Figure 12 shows the transition from V_{IN} = 5 V to 12 V. When V_{IN} is higher than the SLG59H1313C's OVLO threshold level, the SLG59H1313C opens its internal switch and its PG output becomes asserted high. In turn, the SLG59H1006V's ON signal is high and 12 V appears at V_{OUT2}. The reverse transition from 12 V to 5 V is illustrated on Figure 13. Figure 14 and Figure 15 show the transitions from 12 V to 0 V and from 5 V to 0 V, respectively.

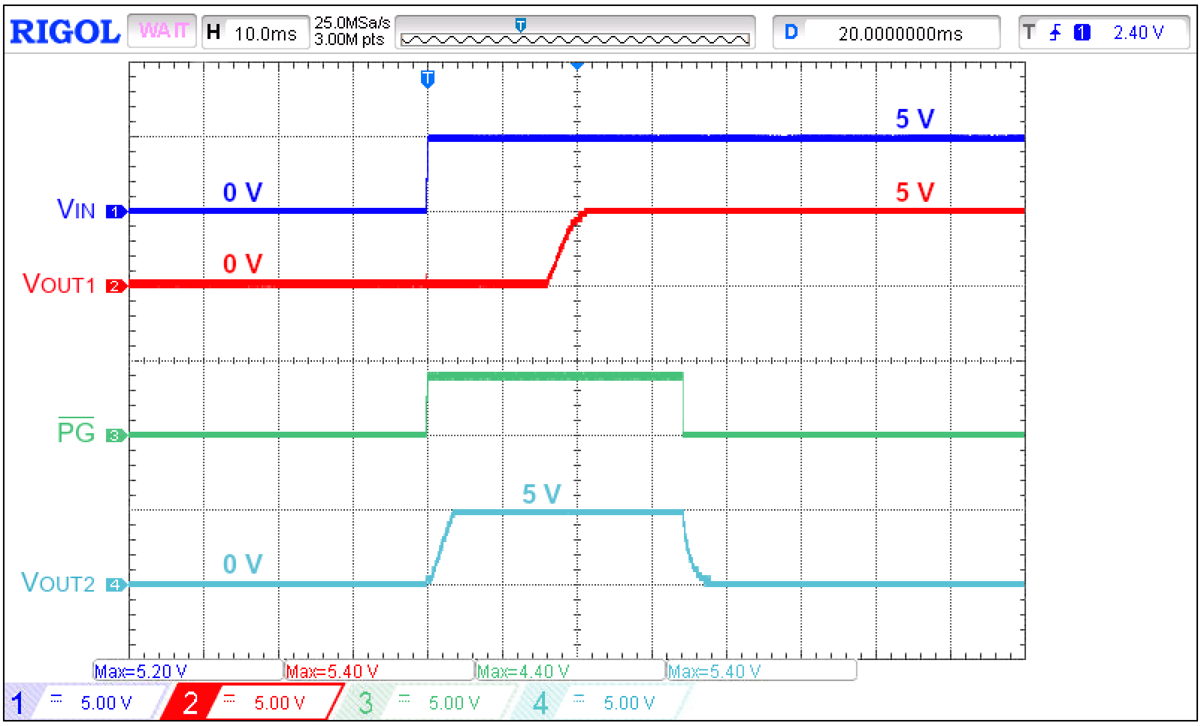

Figure 10: 5 V power splitter operation using SLG59H1313C and SLG59H1006V GreenFET Load Switches

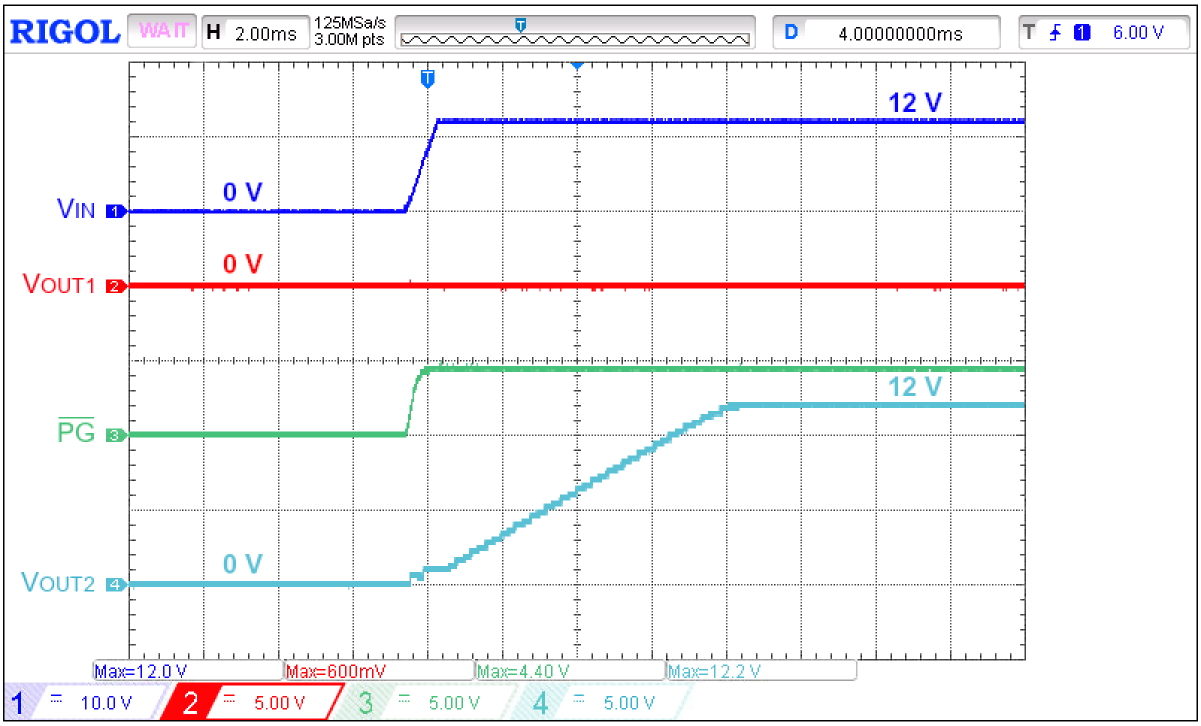

Figure 11: 12 V power splitter operation using SLG59H1313C and SLG59H1006V GreenFET Load Switches

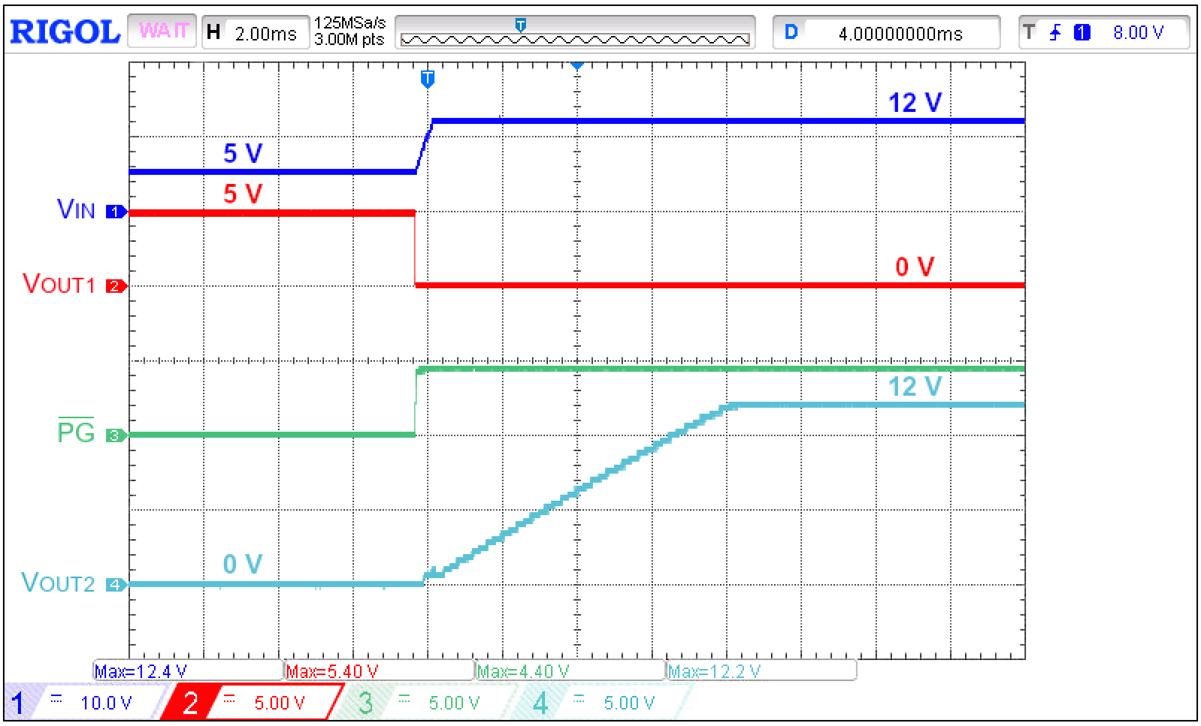

Figure 12: 5 V to 12 V power splitter transition operation using SLG59H1313C and SLG59H1006V GreenFET Load Switches

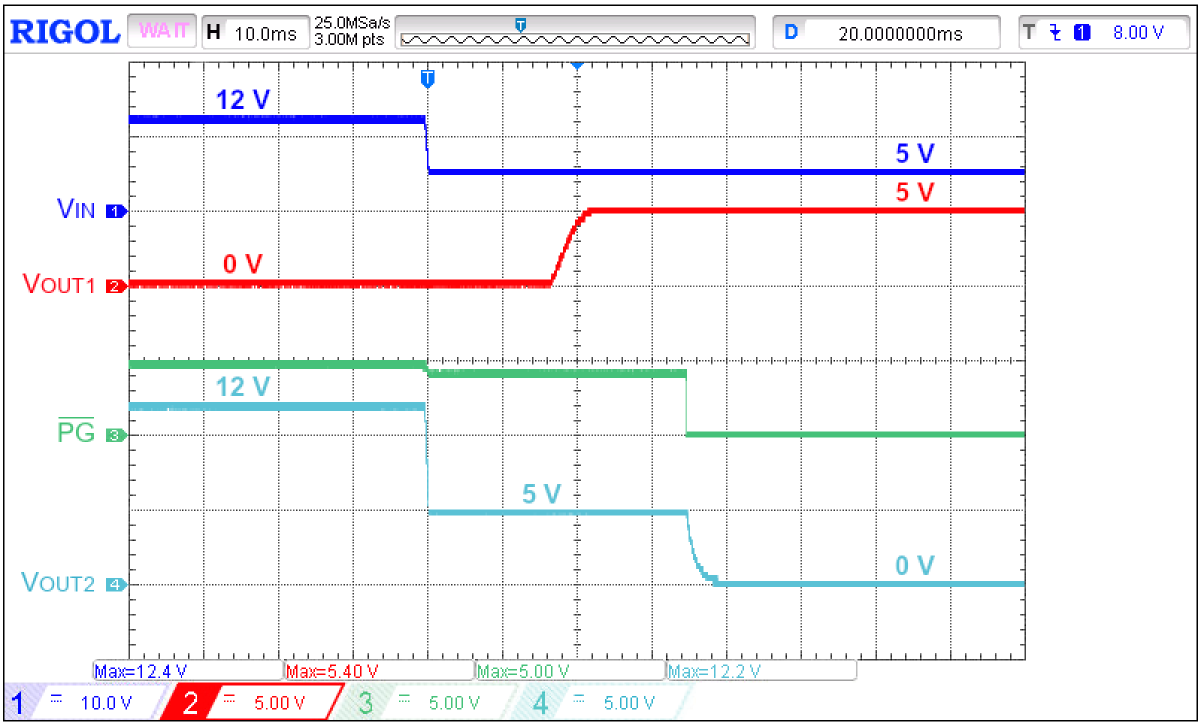

Figure 13: 12 V to 5 V power splitter transition operation using SLG59H1313C and SLG59H1006V GreenFET Load Switches

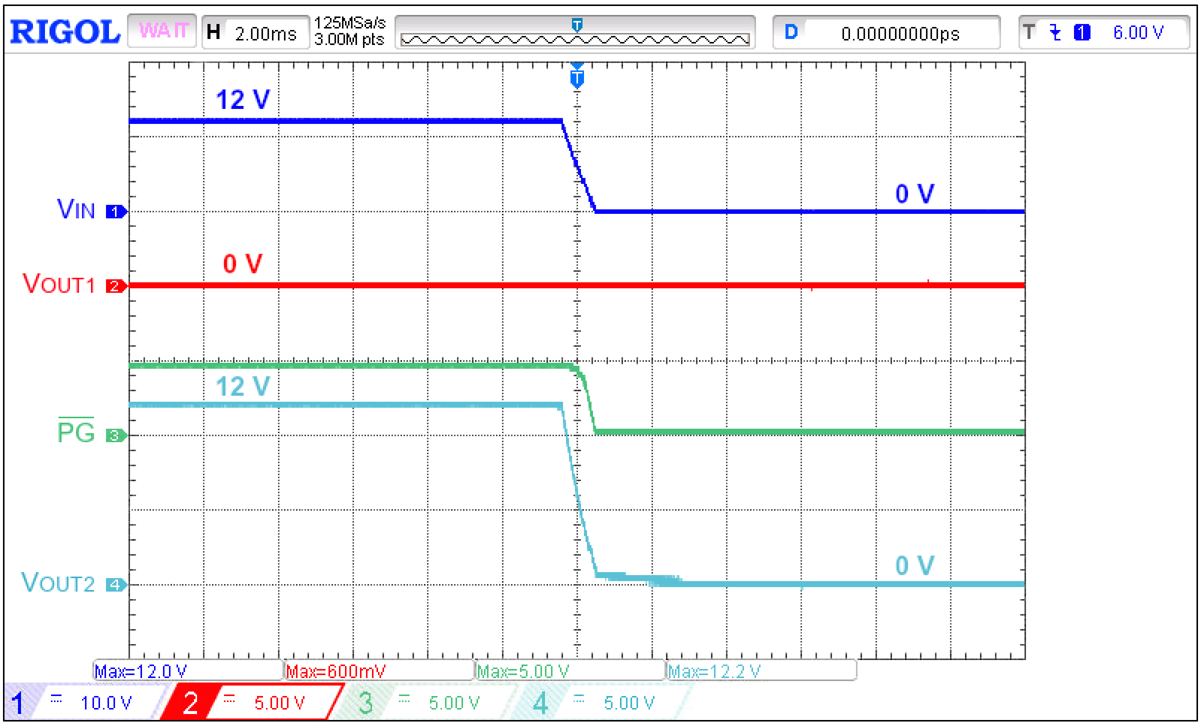

Figure 14: 12 V to 0 V power splitter transition operation using SLG59H1313C and SLG59H1006V GreenFET Load Switches

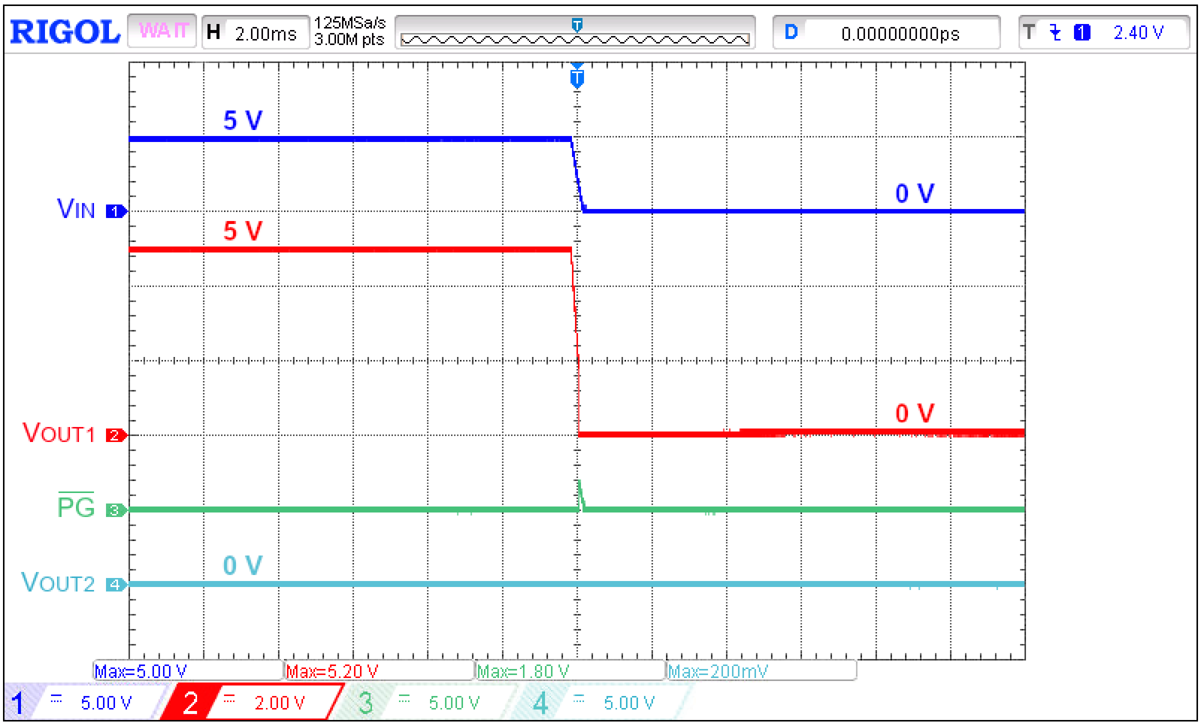

Figure 15: 5 V to 0 V power splitter transition operation using SLG59H1313C and SLG59H1006V GreenFET Load Switches

6 Using Two SLG59H1313Cs in Power-splitting Applications

Yet another alternative power splitter solution is to use a pair of SLG59H1313C as shown in Figure 16. U1 is configured to operate for 5 V input voltages and U2 is configured to operate for 12 V input voltages. V_{OUT1} output is connected to the ON pin of U2 to turn it off when a 5 V power rail is used and to prevent 5 V from appearing at the 12 V power rail output. The PG output of U2 is connected to the gate of transistor Q1, to turn off U1 when a 12 V power rail is used. Lowest total power consumption is achieved implementing this solution.

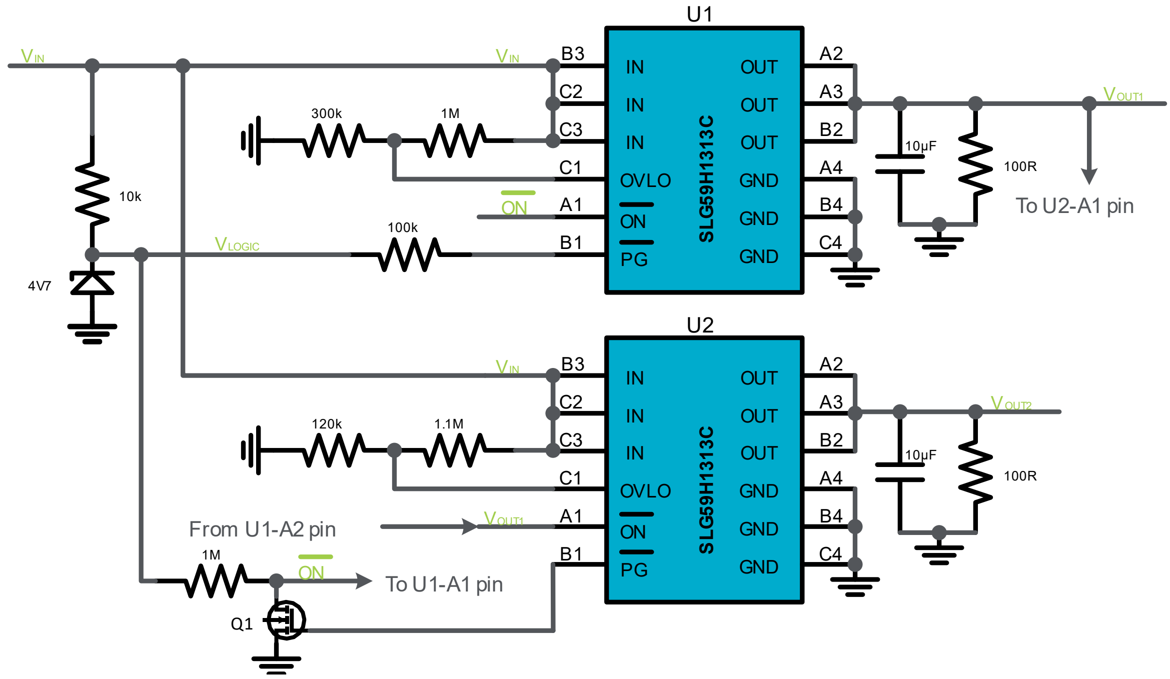

Figure 16: A schematic of a power splitter using two SLG59H1313C GreenFET Load Switches

Figure 17 illustrates 5 V operation of the power splitter using two SLG59H1313Cs. When a 5 V input voltage appears at V_{IN}, U1's PG becomes asserted high. After 15 ms, GreenFET load switch U1 is closed and the voltage appears at V_{OUT1}, which is connected to the ON pin of U2 and switches it off, so the voltage doesn't appear at V_{OUT2}.

When applying 12 V at V_{IN}, load switch U1's overvoltage protection is triggered, and the voltage doesn't appear at V_{OUT1}. Since V_{OUT1} is used as the control signal for U2's ON pin, load switch U2 is turned on and 12 V appears at V_{OUT2} (please see Figure 18). Once V_{OUT2}'s voltage has reached its steady-state value, U2's PG becomes asserted low which open-circuits the discrete n-channel MOSFET Q1. Since the drain of Q1 is connected to U1's ON pin, U1 is turned off, thereby saving power instead of its idling in its OVP state. Figure 19 shows the transition from V_{IN} = 5 V to 12 V. Figure 20 and Figure 21 show the transitions from 12 V to 0 V and from 5 V to 0 V, respectively.

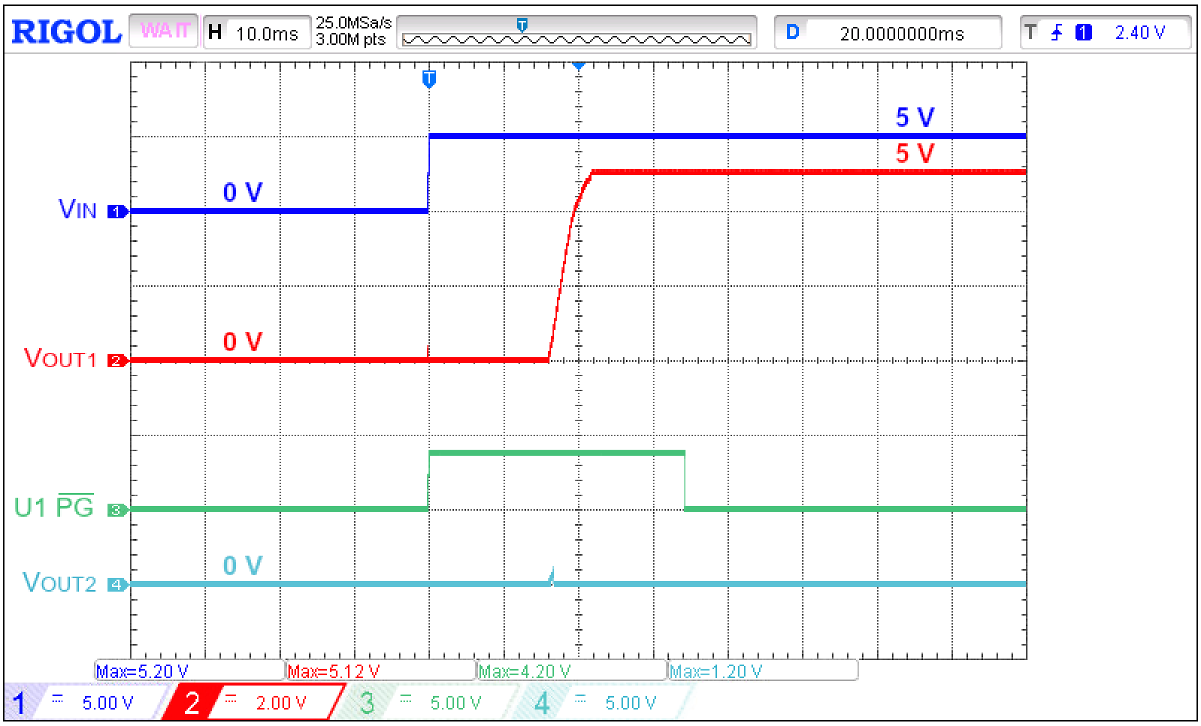

Figure 17: 5 V power splitter operation using two SLG59H1313C GreenFET Load Switches

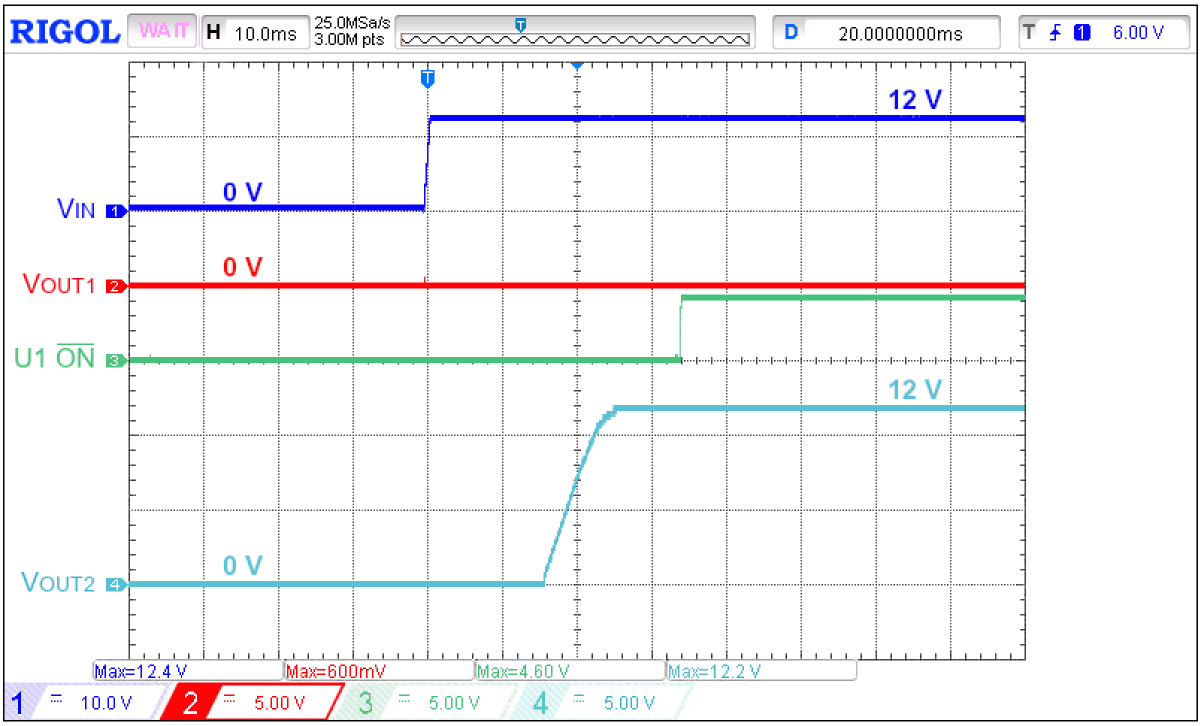

Figure 18: 12 V power splitter operation using two SLG59H1313C GreenFET Load Switches

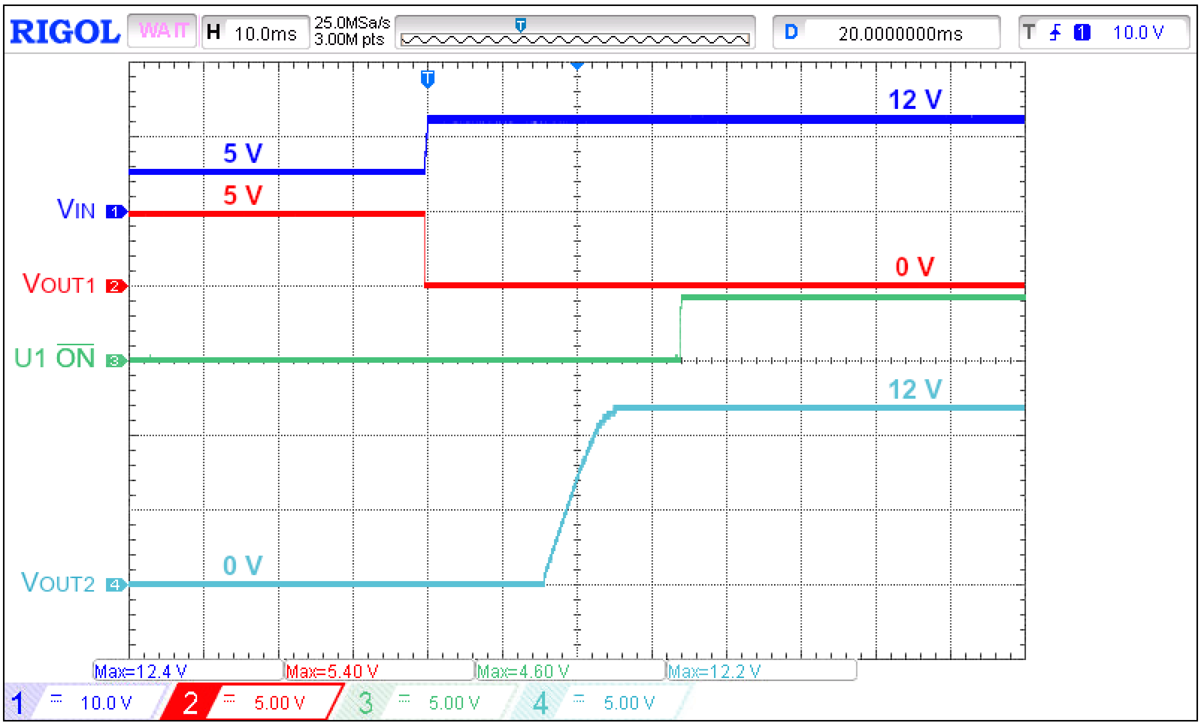

Figure 19: 5 V to 12 V power splitter transition operation using two SLG59H1313C GreenFET Load Switches

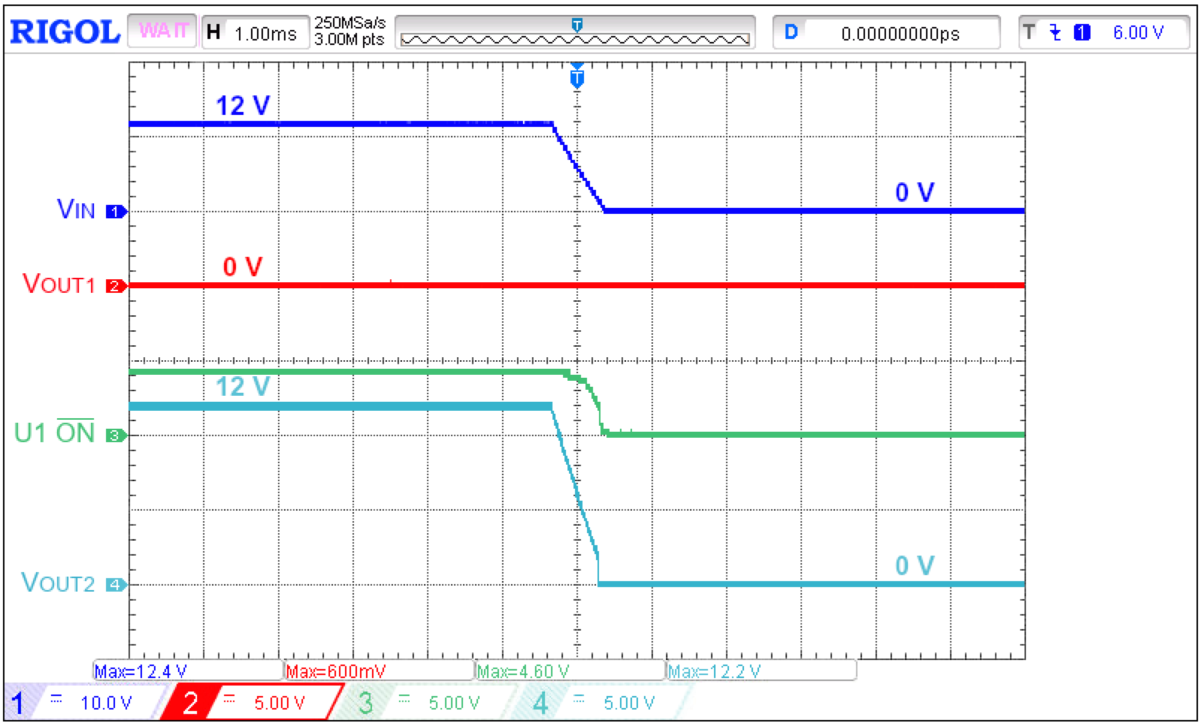

Figure 20: 12 V to 0 V power splitter transition operation using two SLG59H1313C GreenFET Load Switches

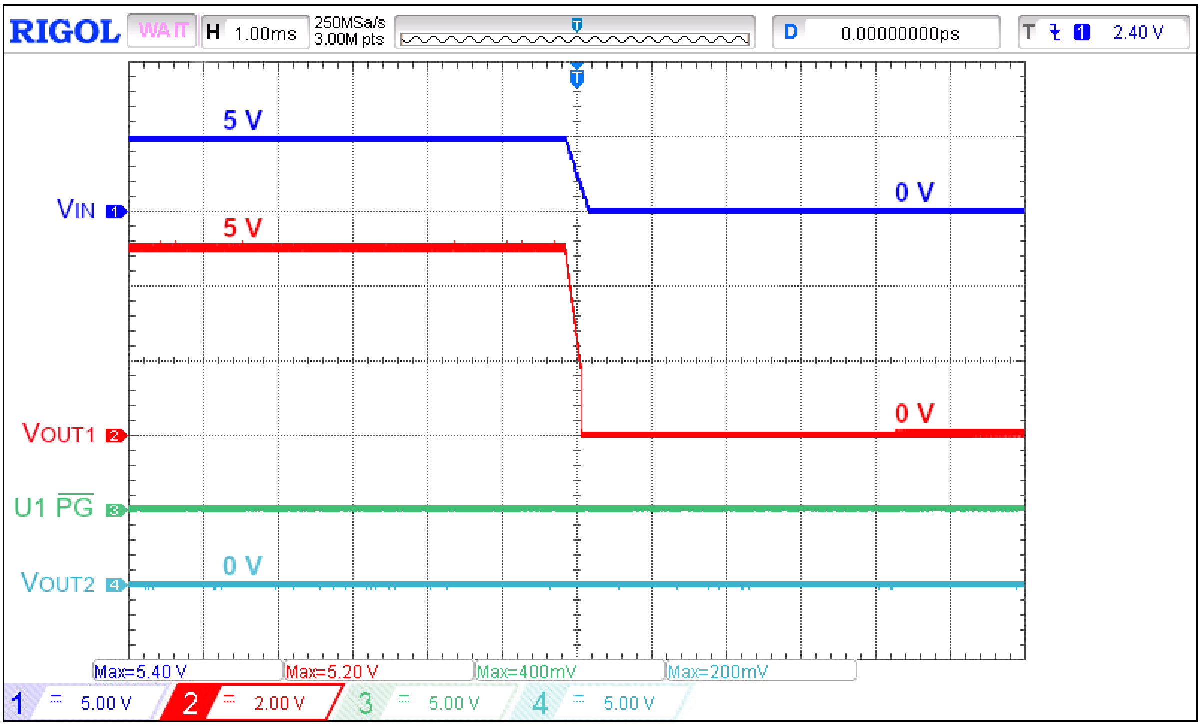

Figure 21: 5 V to 0 V power splitter transition operation using two SLG59H1313C GreenFET Load Switches

One disadvantage of such a design is that it doesn't allow a clean transition from 12 V to 5 V. Since load switch U2 is configured to operate for voltages up to 12 V, so when the voltage at V_{IN} drops to 5 V, it remains ON. Thus, U2's PG remains low, Q1 is open-circuited, so V_{LOGIC} on U1's ON pin keeps U1 in its OFF state. That's why V_{OUT1} remains 0 V when V_{OUT2} drops from 12 V to 5 V.

If a transition from 12 V to 5 V is required, then the design illustrated in Figure 22 can be used. The overall behavior of such a system is the same. Now, a transition from 12 V to 5 V is allowed (please see Figure 23). However, because load switch U1 is always powered up, overall power consumption is higher when a 12 V power rail is present at V_{IN}.

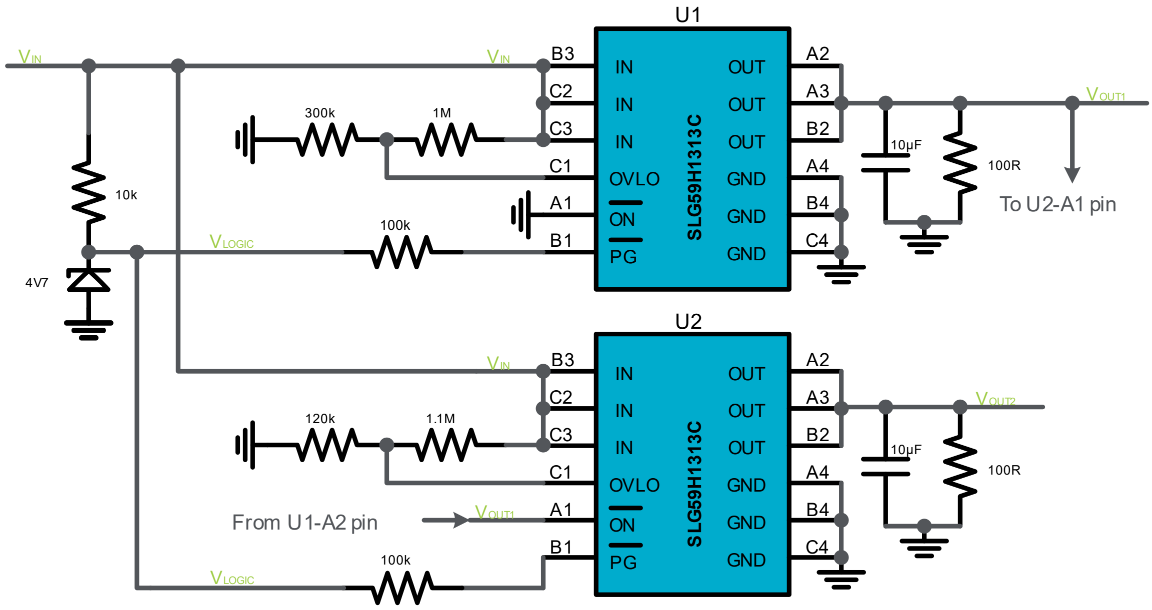

Figure 22: A schematic of a power splitter using two SLG59H1313C GreenFET Load Switches

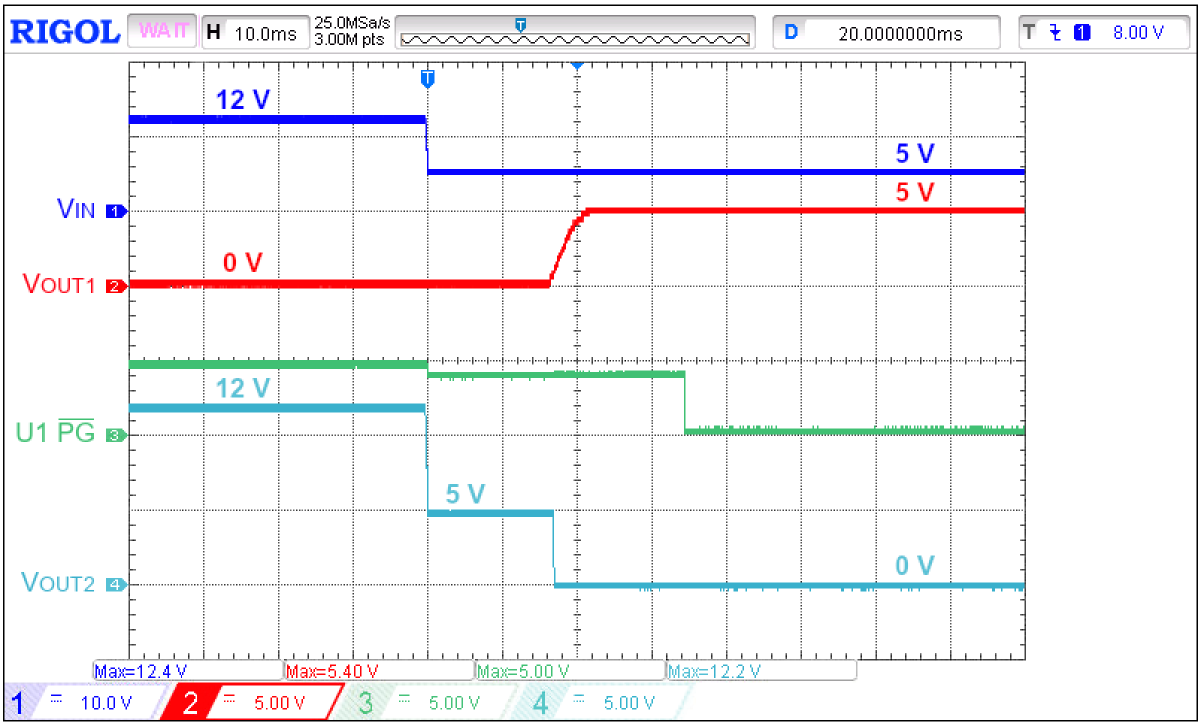

Figure 23: 12 V to 5 V power splitter transition operation using two SLG59H1313C GreenFET Load Switches

7 Using a SLG59H1302C in Power-splitting Applications

Another way to implement power-splitting is to use SLG59H1302C [4]. The SLG59H1302C is a 130 V surge-protected, 28 V tolerant power splitter with two high-current switches. With independent control for each channel, the SLG59H1302C contains a 6 A capable, 12 mΩ nFET switch for the

BUS-to-OUT path and a reverse-blocking 6 A capable, 24 mΩ nFET switch for the BUS-to-SYS path. Figure 24 illustrates a power splitter schematic using SLG59H1302C load switch.

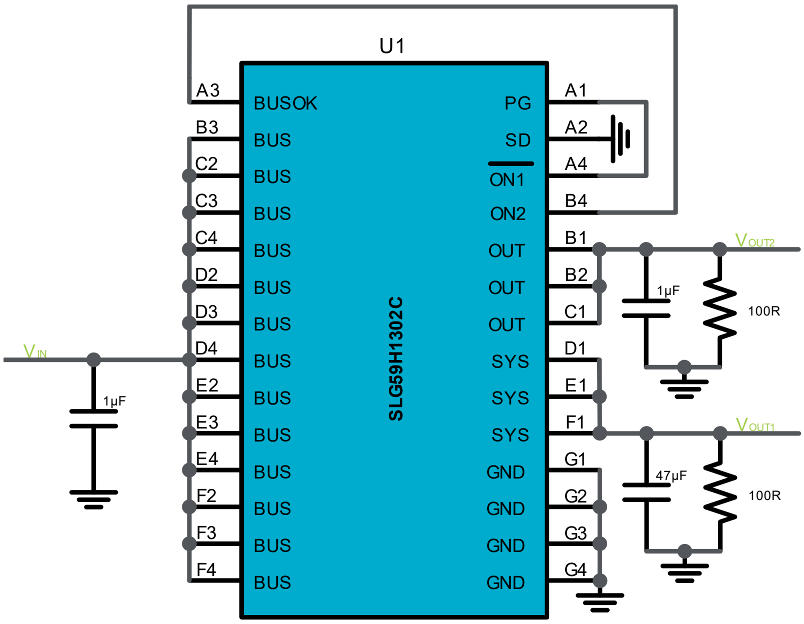

Figure 24: A schematic of a power splitter using SLG59H1302C GreenFET Load Switch

A BUS-to-SYS (V_{OUT1}) switch has an overvoltage lockout level at 5.25 V and is controlled with the ON2 pin. In our application, the ON2 pin is connected to the BUSOK output terminal. BUSOK becomes asserted high when there is no fault condition at V_{IN}. A BUS-to-OUT (V_{OUT2}) switch has an overvoltage lockout level at 13.9 V and is controlled by the ON1 pin. The ON1 pin is connected to the IC's PG output, which is an active-high push-pull output and is asserted high when ON2 is high.

Initially, when there is no input voltage applied to the IC, ON1 and ON2 signals are low. When 4.5 V is applied at the BUS terminal (please see Figure 25), the BUS-to-OUT switch is closed, and 4.5 V appears at V_{OUT2}. After approximately 30 ms [4] when BUSOK voltage level becomes high, 4.5 V appears at V_{OUT1}, PG goes high, and the BUS-to-OUT switch is opened.

When V_{IN} = 12 V is applied, the BUS-to-SYS switch's overvoltage protection feature is triggered preventing any voltage from appearing at V_{OUT1}. PG remains asserted low which turns on the BUS-to-OUT switch. Thus, 12 V appears at V_{OUT2} (please see Figure 26).

Figure 27 shows the transition from V_{IN} = 4.5 V to 12 V. The reverse transition from 12 V to 4.5 V is illustrated in Figure 28. Figure 29 and Figure 30 show the transitions from 12 V to 0 V and from 4.5 V to 0 V respectively.

Choosing SLG59H1302C realizes a single-case power splitter to save valuable PCB space.

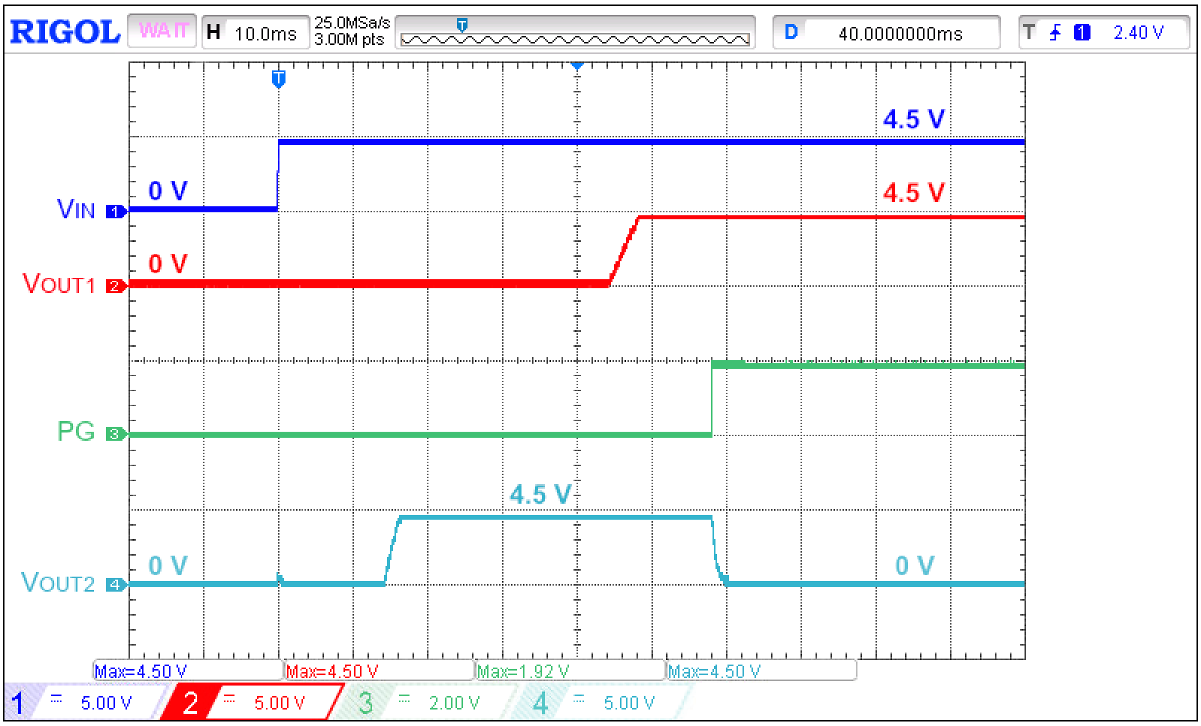

Figure 25: 4.5 V power splitter operation using SLG59H1302C GreenFET Load Switch

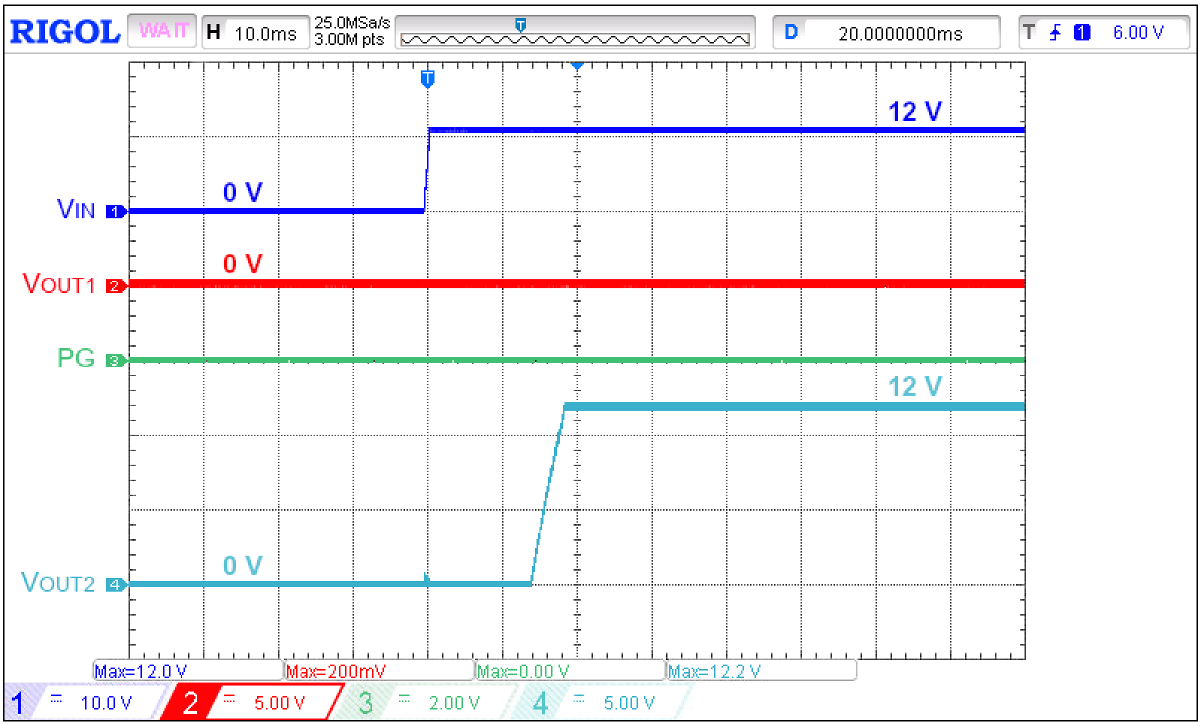

Figure 26: 12 V power splitter operation using SLG59H1302C GreenFET Load Switch

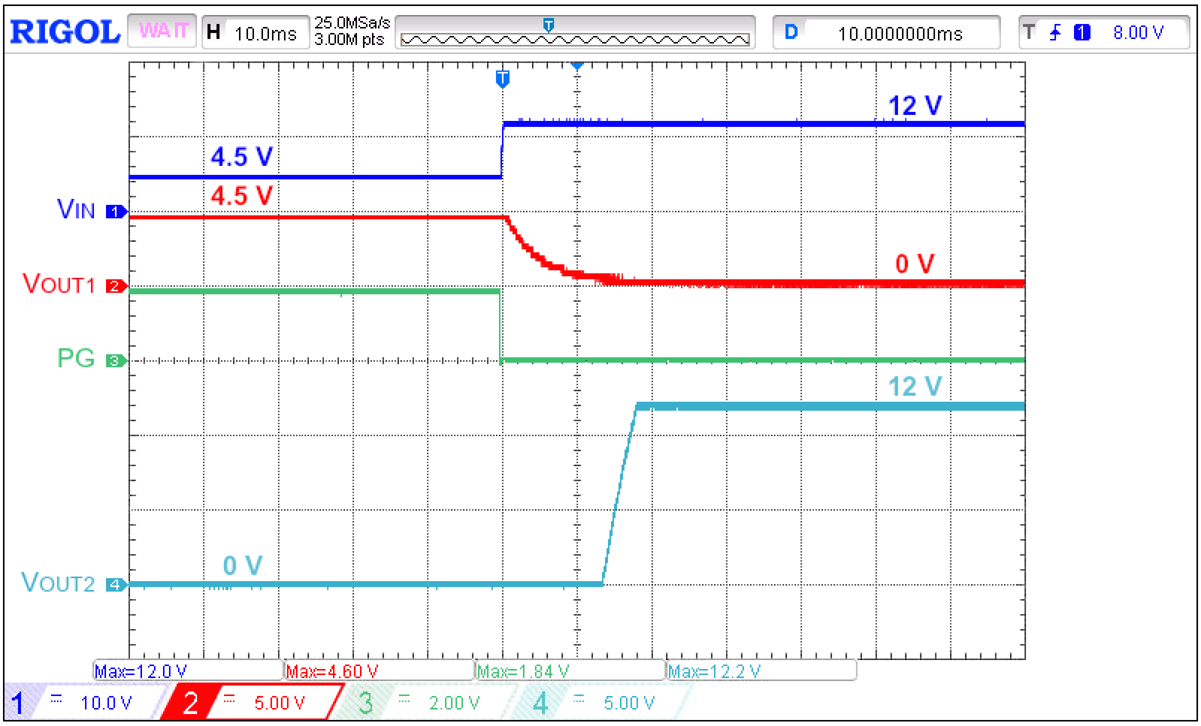

Figure 27: 4.5 V to 12 V power splitter transition operation using SLG59H1302C GreenFET Load Switch

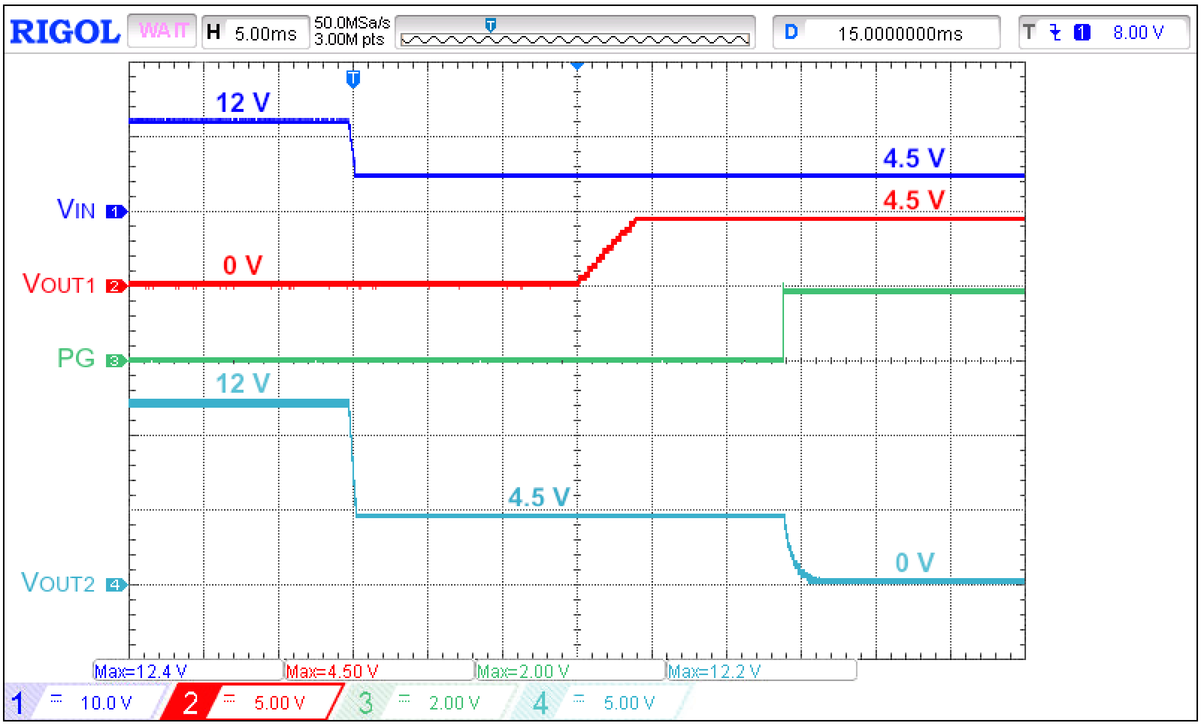

Figure 28: 12 V to 4.5 V power splitter transition operation using SLG59H1302C GreenFET Load Switch

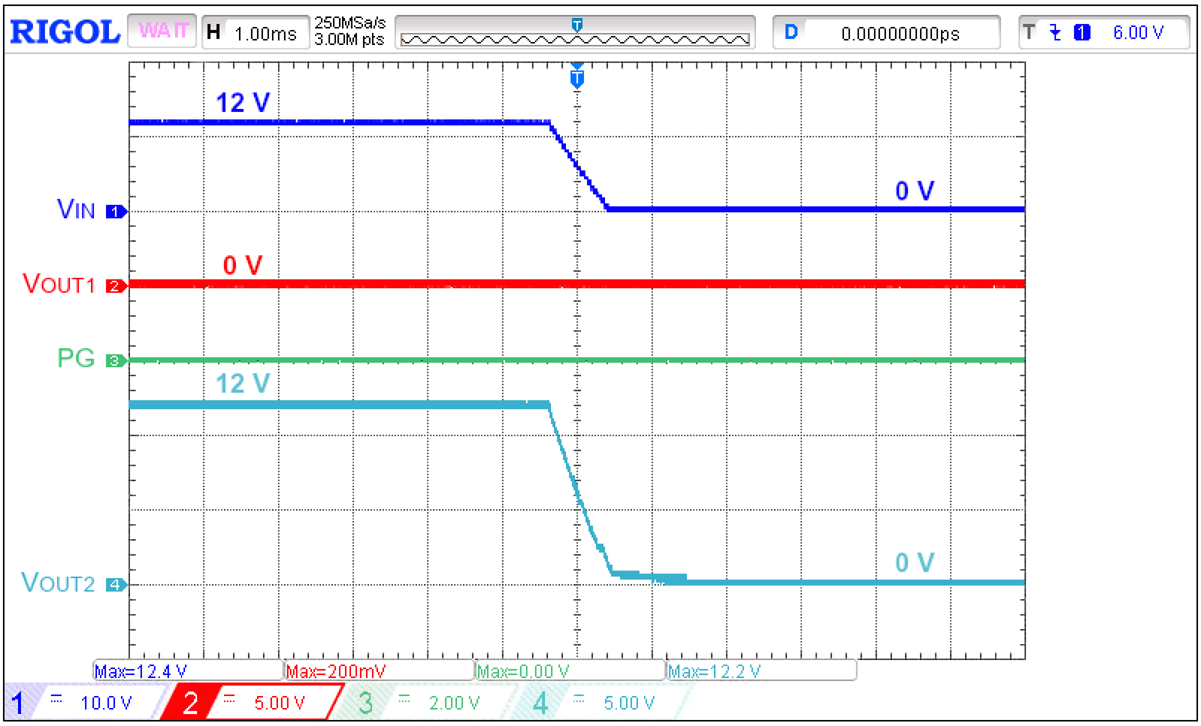

Figure 29: 12 V to 0 V power splitter transition operation using SLG59H1302C GreenFET Load Switch

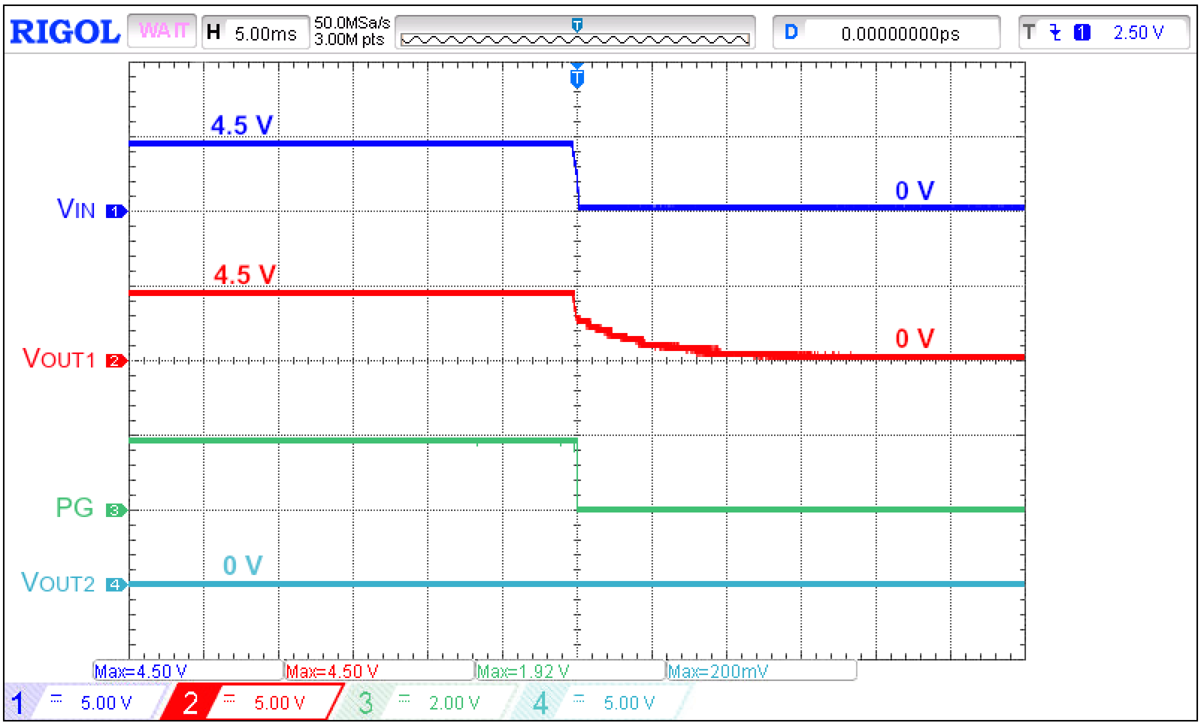

Figure 30: 4.5 V to 0 V power splitter transition operation using SLG59H1302C GreenFET Load Switch

8 Conclusions

Renesas offers several solutions addressing power-splitting systems. Using the SLG59H1313C and SLG59H1008V for power-splitting applications provides the latitude to have fixed undervoltage/overvoltage lockout windows. The combination of SLG59H1313C and SLG59H1006V GreenFET load switches allows choosing one of four V_{IN} Overvoltage Lockout Thresholds. The SLG59H1302C realizes a high-performance self-contained power splitter to save extra PCB space. An inconvenience in using such solutions is that the overvoltage lockout thresholds are strictly fixed. The freedom to set user-defined over-voltage lockout levels for both power rails across a wide voltage range is best achieved using a pair of SLG59H1313C GreenFET load switches.

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