

Application Note

8-channels Analog max/min Voltage Monitor

AN-CM-281

Abstract

This application note implements a max (or min) voltage finder among several analog inputs. It describes the functional logic, GreenPAK implementation and the obtained results. This application note comes complete with design files which can be found in the References section.

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1 Terms and Definitions

IC	Integrated circuit
I/O	Input/output
LSB	Least significant bit
MSB	Most significant bit
PGA	Programmable gain amplifier
ADC	Analog-to-digital converter
ACMP	Analog compare component
INT	Interrupt signal, a digital signal issued by ADC once a conversion is completed
DCMP	Digital Compare Module
SPI	Serial peripheral interface
CLK	Clock, generally a signal used to synchronize logic components or store data
DFF	D-type Flip-Flop, a single-bit clocked memory element
AND gate	A digital logic gate that gives a true (1 or high) output when all the inputs are true
OR gate	A digital logic gate that gives a true (1 or high) output when at least one of the inputs is true
XOR gate	A digital logic gate that gives a true (1 or high) output when the number of true inputs is odd
NXOR gate	A digital logic gate that works as the logic negation of a XOR gate

2 References

For related documents and software, please visit:

[GreenPAK™ Programmable Mixed-signal Products | Renesas](#)

Download our free GreenPAK Designer software Ref. [1] to open the .gp files Ref. [2] and view the proposed circuit design. Use the GreenPAK development tools to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes Ref. [4] featuring design examples Ref. [1], as well as explanations of features and blocks within the Renesas IC.

- [1] [Go Configure Software Hub](#), Software Download and User Guide, Renesas Electronics
- [2] [AN-CM-281 8 Channels Analog max-min Voltage GP](#), GreenPAK Design File, Renesas Electronics
- [3] [GreenPAK Application Notes](#), GreenPAK Application Notes Webpage, Renesas Electronics
- [4] SLG46620G, [Product Page](#) and [Datasheet](#), Renesas Electronics
- [5] [The GreenPAK Cookbook](#), Datasheet, Renesas Electronics
- [6] [AN-1066 Voltage Slope Direction Determination Circuit](#)
- [7] [AN-CM-242 Binary Parity Generator and Checker](#)

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3 Introduction

Control systems and related devices deal with multiple power sources, such as bias lines or batteries, and must track the highest (or the lowest) line among a given set.

For example, load switching in a “multi battery”-powered system requires that the system monitors either the minimum or the maximum voltage among the battery array (max or min as a function of the particular switching algorithm) and dynamically routes the load to the most appropriate source in real time. Alternatively, the system may need to temporarily un-connect the lowest-voltage battery for proper charging.

Another example is the modern solar power system, where every solar panel is equipped with a tilt-rotate mechanism and with a solar tracking circuit (the latter providing the Sun position information to orient the panel). With the max-voltage info, each solar panel position can be fine-tuned on the basis of the string’s panel actually delivering the highest output voltage, thus achieving a superior level of power optimization.

There are several different brands of commercial IC’s (mainly microcontrollers) that can in principle implement a max voltage follower. However, they require programming and are less cost effective than a mixed-signal solution. Supplementing a Dialog GreenPAK™ design can positively affect the affordability, size, and modularity of the design. This design exploits the benefit of integrating both analog and digital circuitry into one single chip.

In this application note, the analog front-end and the digital logic required to implement a max (or eventually min) voltage finder among eight distinct sources is implemented.

To implement the 8-channel analog max/min voltage monitor a SLG46620G is used.

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4 Block Diagram

The following Figure shows the global diagram of the implemented system:

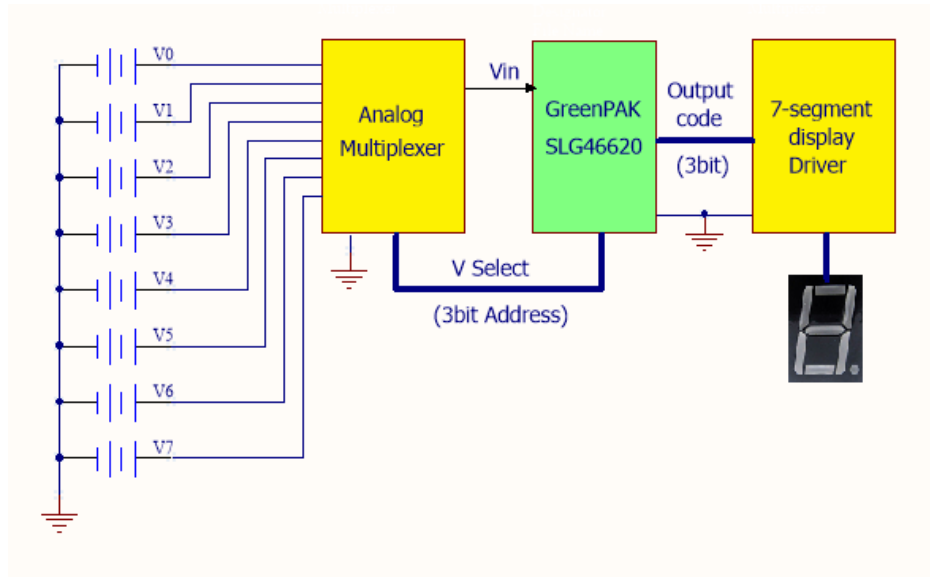


Figure 1: Block Diagram of the 8-Channels Max Voltage Finder

A string of up to 8 variable voltage sources is multiplexed and interfaced to a GreenPAK's ADC module connected to a customized internal design capable of selecting the source with the highest voltage in respect to the others. The internal logic outputs this information for display or further processing.

The design is based on the GreenPAK SLG46620G product, because it embeds all the necessary analog and digital building blocks for the application. In this implementation the array is scanned by means of an ADG508 analog multiplexer directly driven by the GreenPAK IC.

The output information is a 3-bit digital number corresponding to the voltage source number at max voltage. A direct way to get this information is to show the number by means of a 7-segment display. It can be easily accomplished by interfacing the SLG46620G's digital output to a 7-segment display driver, such as the GreenPAK solution described in Ref. [8] or to a common 74LS47 IC.

The circuit presented looks for maximum voltage. To convert the design into a minimum voltage finder, a simple pre-conditioning circuit must be added between the analog multiplexer and the GreenPAK analog input, subtracting the multiplexer output from a 1 V reference voltage.

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5 Principle of Operation

The design aims to select the source with max voltage, therefore a scan is performed on the whole array while storing the last-max value and comparing it with the next value in input (which belongs to the next voltage source in the scan).

In the following we will refer to a complete multiplexing sequence along all the inputs as a “scan” or “loop”.

Comparison between two values is not accomplished by means of ACMP components (however, available in the SLG46620G), but rather by the DCOMP module, once the values are respectively digitized. This is an advanced and refined technique first addressed in Ref. [7].

Figure 2 shows how the SLG46620G is structured for this design:

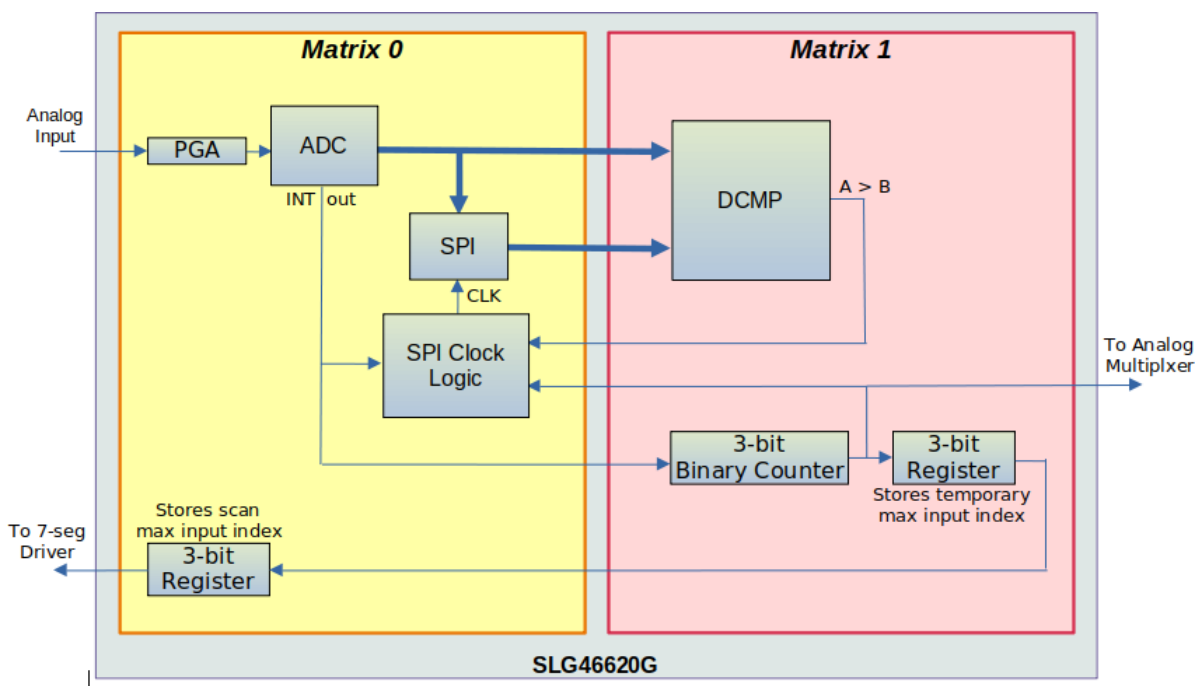


Figure 2: Internal Design of the GreenPAK IC

The analog input signal goes to the ADC input through the PGA component with a set Gain of 1. Various Gain settings are also possible to find the best match with the front-end conditioning electronics devoted to mapping the input voltages to the 0-1 V range of the GreenPAK ADC module.

The ADC operates in single-ended mode and converts the analog signal to an 8-bit digital code, which is then transferred to the DCOMP module. The digital code is also fed into the SPI block, configured as an ADC/FSM Buffer, where a digital code can be stored and won't change until the next pulse comes to the SPI CLK input. Notice that a dedicated logic block drives the SPI CLK input. We will investigate this part later, as this is the “core” logic responsible for proper operation. A new digital code is stored into the SPI module only if it belongs to the actual max input voltage.

The DCOMP component is used to compare current ADC data with the last winner (that is the last max found) which is stored in the SPI block. It will generate a pulse at the OUT+ output when new ADC data is greater than the previous one. We use the OUT+ signal to update the SPI block with the new winner.

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A global clock signal drives ADC conversions and general timings. Once a conversion is performed, the ADC's INT output signal pulses, coordinated in time with the ADC parallel data output. We use the INT output also to increment a 3-bit binary counter, implemented by DFFs in Matrix1, which is useful for three reasons:

1. The counter output lines address the external analog multiplexer, thus serving the next input voltage to the ADC;
2. The count is frozen into a 3-bit register (implemented in Matrix1) to store the temporary winner during a scan;
3. The count is decoded to update a second 3-bit register (implemented in Matrix0) once a scan is completed.

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6 Logic Implementation

The ADC module sequentially provides converted data of all the input voltages, one after the other, indefinitely. Once the Multiplexer is addressed 0b111 (decimal 7), the counter rolls off to 0b000 (decimal 0) thus starting a new scan of the input voltages.

During the scan, the ADC INT output signal is generated when the parallel data output is valid. When this signal pulses, the analog multiplexer must switch to the next input, providing the PGA with the corresponding voltage. Therefore, the ADC INT output is the direct clocking signal of the 3-bit Binary Counter of Figure 2, whose 3-bit parallel output word directly addresses the external analog multiplexer ("V select" in Figure 1).

Let us now refer to an example where the input voltages are supposed to have the following relationships:

$$\text{a) } V_0 < V_1 < V_2$$

$$\text{b) } V_2 > V_3, V_4$$

$$\text{c) } V_5 > V_2$$

Figure 3 represents the main signals involved in the max-decision mechanism:

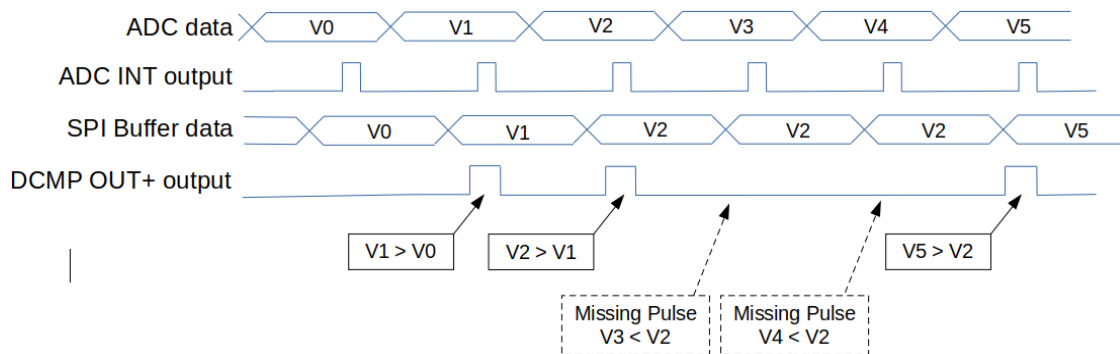


Figure 3: Example of ADC, SPI, and DCMP Timing Diagram

Since data is eventually clocked into the SPI buffer register synchronously with INT pulses, a comparison window exists where the SPI buffer content is compared with the next ADC conversion result. This particular timing results in the generation of OUT+ pulses at the DCMP output. We can take advantage of these pulses to load new values into the SPI buffer register.

As apparent from the SPI buffer data line of the preceding Figure, the SPI register always contains, time by time, the greatest value among the 8 inputs and it is updated only when a bigger value is detected by the DCMP module (referring to the DCMP OUT+ output line of the plot, the missing pulses cause V2 to remain latched in the register until compared with V5).

6.1 Resolving Deadlock

If the implemented logic would be just as described above, it is clear that we would bump into a deadlock situation: the system is capable to detect only voltages higher than the one corresponding to what is stored into the SPI buffer register. This is also valid in case this voltage would decrease and then another input, until now lower than that, becomes the highest: it would never be detected.

This situation is better explained in Figure 4 where only 3 input voltages are present for the sake of clarity:

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<i>Loop Iteration</i>	<i>0</i>	<i>1</i>	<i>2</i>	<i>3</i>
<i>V1</i>	0.5V	0.4V	0.4V	0.4V
<i>V2</i>	0.3V	0.3V	0.3V	0.3V
<i>V3</i>	0.6V	0.6V	0.2V	0.2V
<i>SPI Buffer Register</i>	V3	V3	V3	V3
<i>Correct SPI Buffer Register</i>	V3	V3	V1	V1

Figure 4: Example of a Deadlock Situation

At the time of iteration 2, V3 drops and V1 is the actual max voltage. But the DCMP module does not provide a pulse because the data stored into the SPI buffer register (corresponding to 0.6 V) is bigger than that corresponding to V1 (0.4 V).

The system then behaves as an “absolute” max finder and does not update the output correctly.

A nice way to overcome this problem is to force reloading the data into the SPI Buffer Register when the system completes a full polling cycle of all channels.

In fact, if the voltage at that input is still the highest, nothing changes and the control safely goes on (referring to [Figure 4](#) above, this is the case of Loop Iterations 0 and 1). On the other hand, if the voltage at that input by chance lowers to a value less than another input, then reloading the value gives the possibility to the DCMP module to produce an OUT+ pulse when comparing it with the new max value (this is the case of Loop Iterations 2 and 3).

A piece of logic circuit is necessary to overcome the problem. It must generate a clock signal to the SPI component when the loop reaches the actual max input, thus forcing a re-load of its updated data word into the SPI Buffer Register. This will be discussed in [Sections 7.2](#) and [7.6](#) below.

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7 Device Configuration

The SLG46620G has two Matrix blocks, as depicted in Figure 2. The following Figures show the respective device configurations.

7.1 Matrix0 Circuit

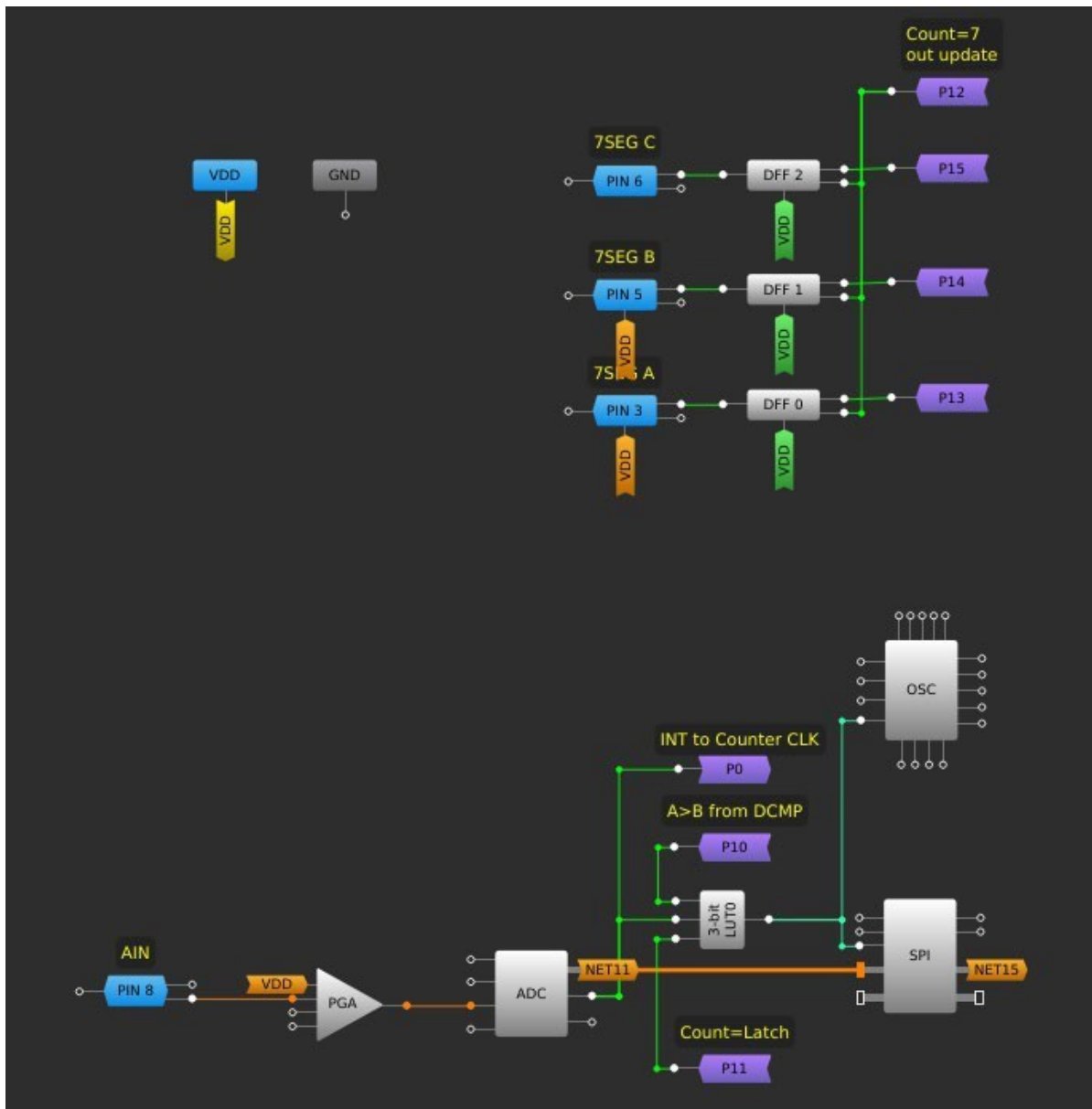


Figure 5: Matrix0 Circuitry of the SLG46620G

The upper portion of the circuit is the “Loop Register” realized with 3 DFFs (DFF0, DFF1, and DFF2). It is refreshed after every loop of the input multiplexer to send to a 7-segment display driver the binary number of the “winner”, that is the input with highest voltage in the last scan. Both the clock to the DFFs and the data comes from the logic implemented in Matrix1 through, respectively, port P12, P13, P14, and P15.

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The lower part is the analog front end with input at Pin 8 and PGA with gain x1. The ADC INT output goes both to SPI's clocking logic and to Matrix1 via port P0, where it will serve as the clock signal for the counter implemented.

ADC and SPI parallel data outputs are respectively labeled NET11 and NET15 to be connected to the DCMP component in Matrix1.

7.2 SPI Clocking Logic

As pointed out before in the "Logic Implementation" section, the SPI Buffer Register is updated every time that a comparison between the actual stored value and the new ADC conversion data generates a pulse at the DCMP OUT+ output.

Signal integrity is ensured if this signal is AND-ed with the ADC INT output. This avoids any spike and false triggering.

We have also underlined that to skip deadlock situations, the SPI Buffer must be updated when the loop reaches the actual winner data.

Three signals then are in the game for proper SPI clocking:

1. ADC INT output (LUT0-IN1)
2. DCMP OUT+ output (LUT0-IN0 via port P10)
3. Count equals Latch signal (LUT0-IN2 via port P11)

The first two are AND-ed and both OR-ed with the latter in LUT0, whose implementation is configured as in [Figure 6](#):

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3-bit LUT0

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

Defined by user

Regular shape

Figure 6: LUT0 as SPI CLK Logic

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7.3 Matrix0 Components Properties

The following Figures show the remaining components property windows belonging to Matrix0:

PGA

Power on signal: Power on

Gain: x1

ADC mode: Single-end

Connections

Channel selector: VDD

IN+ Channel 1: PIN 8

IN+ Channel 2: None

IN- Channel: None

External output: Disable

Apply

Figure 7: PGA Properties

ADC

Mode: Single-end

Vref: Internal 1.2 V

Force analog part: Enable

Analog part speed: 100 kHz

Clock for ADC divide by: 1

ADC data sync. with SPI clock: Disable

PWM & ADC clock source: EXT. CLK2

Sample rate: N/D [Formula](#)

Connections

Serial data: Disable (Matrix <-:)

Information

ADC start time [\(Summary\)](#)

Min, us	Typ, us	Max, us
-	-	-

Power ctrl. settings

Apply

Figure 8: ADC Properties

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SPI	
Mode:	ADC buffer
Clock phase (CPHA):	0
Clock polarity (CPOL):	0
Byte selection:	[15:0]
ADC data sync with SPI clock:	Disable
PWM data sync with SPI clock:	Disable
FSM data sync with SPI clock:	Disable
Connections	
PAR input data source:	ADC
Serial data:	Disable (Matrix <:-)

Figure 9: SPI Properties

OSC	
LF OSC	RC OSC
RING OSC	
RC OSC power mode:	Force power on
RC OSC frequency:	25 kHz
RC matrix power down:	Disable
RC clock predivider by:	1
'OUT0' second divider by:	1
Clock selector:	EXT. CLK2

Figure 10: OSC Properties

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7.4 Matrix1 Circuit

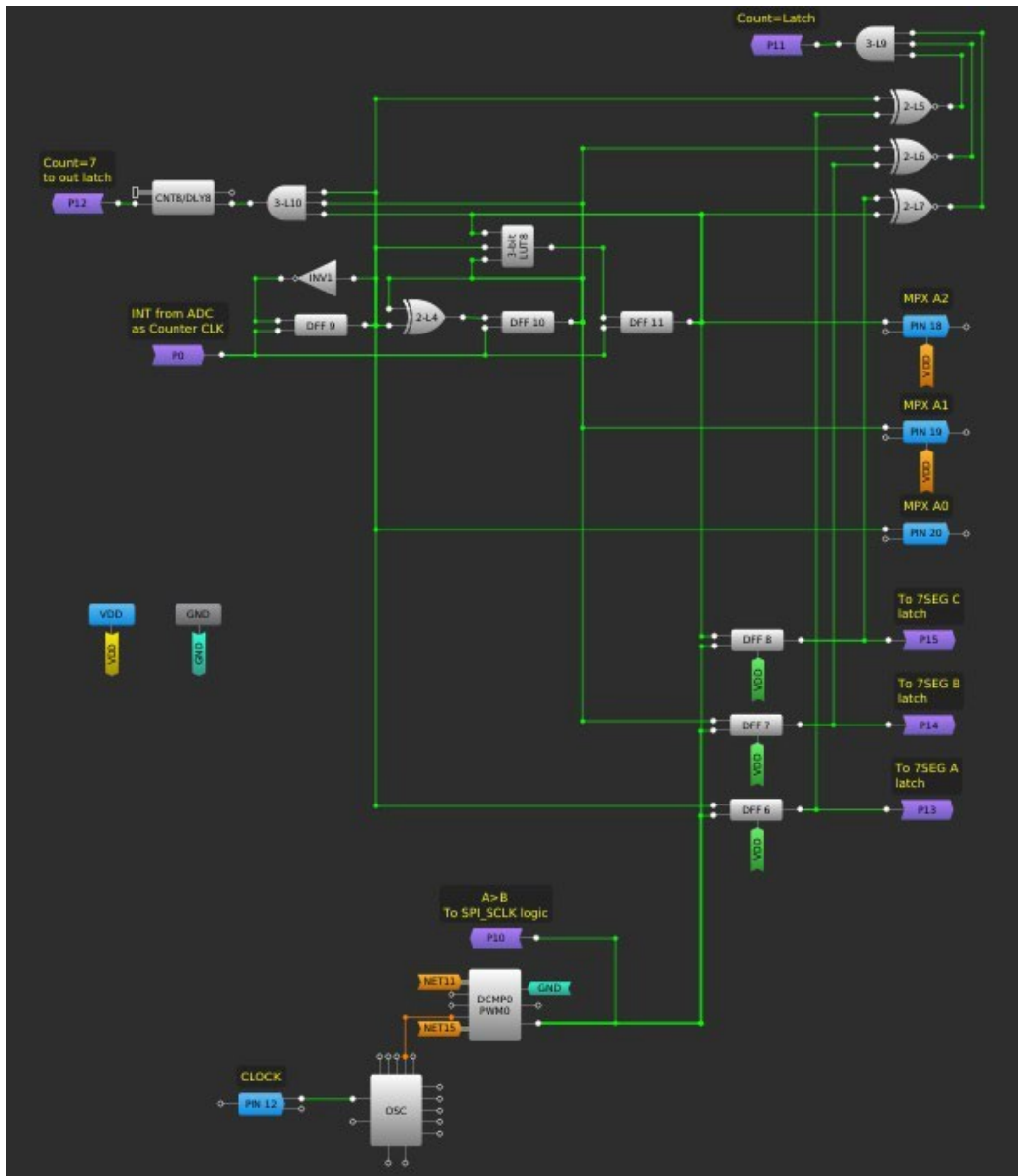


Figure 11: Matrix1 Circuitry of the SLG46620G

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7.5 3-bit Binary Counter

The upper part of the circuit contains logic elements, mainly a 3-bit binary counter clocked by the ADC INT output, as already discussed. This counter is implemented with a quite “standard” schematic:

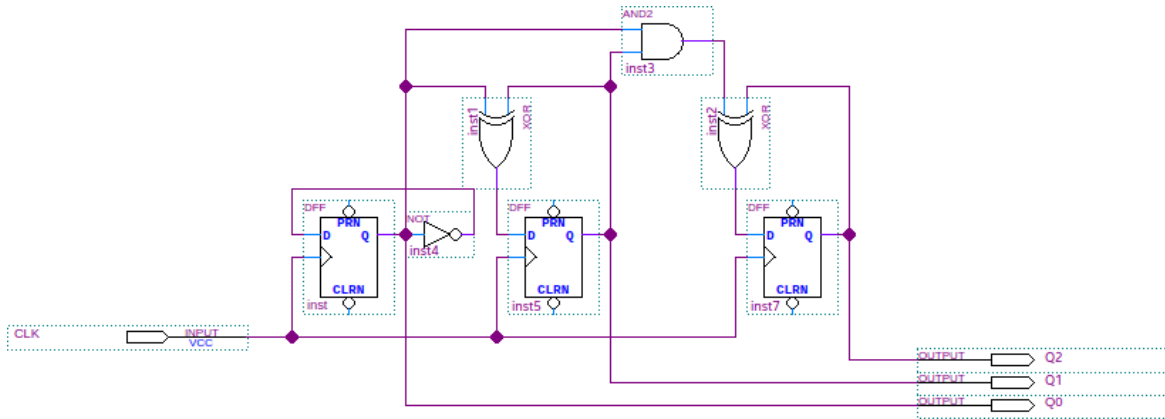


Figure 12: Circuit Used to Implement a 3-bit Binary Counter in the GreenPAK IC

This counter is realized in our design by means of Flip-Flops DFF9, DFF10, DFF11 and INV1, LUT4, LUT8. The DFF9 output is the LSB while DFF11 is the MSB:

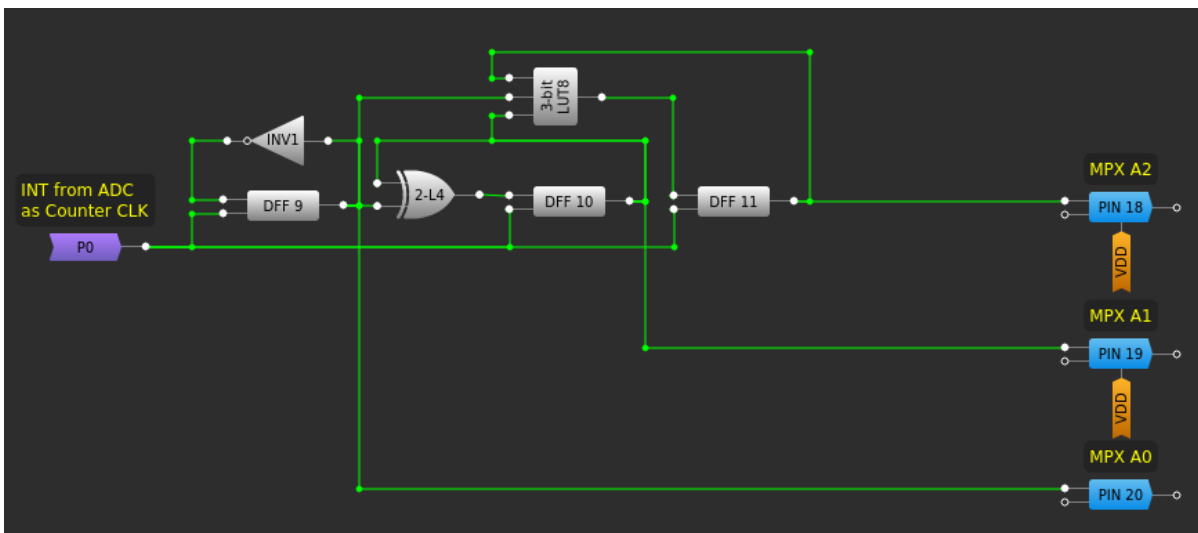


Figure 13: GreenPAK Implementation of a 3-bit Binary Counter

LUT4 is configured as a XOR while LUT8 performs the AND-XOR logic of Figure 12.

Counter outputs go to three digital output pins to address the external Analog Multiplexer.

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3-bit LUT8				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 14: LUT8 Logic

LUT10 decodes the counter's code when a scan is complete and feeds a pulse to Matrix0 via DLY8 and port P12. This is simply accomplished by AND-ing the counter's outputs, thus decoding number 7 dec (0b111 binary, end of loop).

7.6 3-bit Compare Logic

Figure 15 shows the circuit used to detect when the loop is iterating at the current "winner" address. In this case, as already discussed, a digital pulse should force a re-load of the current ADC result to solve a possible deadlock situation.

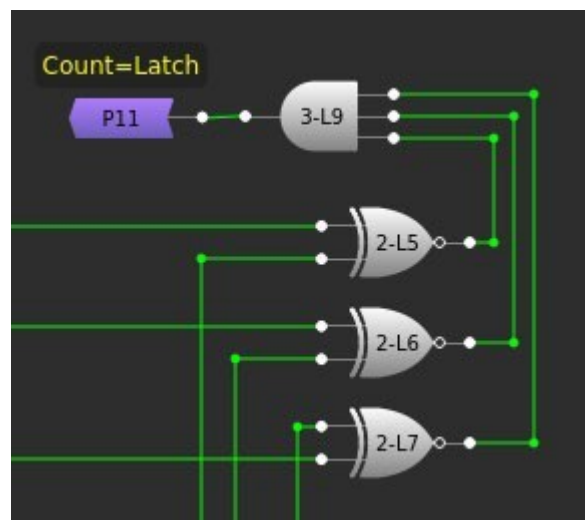


Figure 15: Counter-Register Comparison Logic Circuit

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The “winner” address is stored in the temporary register of Matrix1 (see below), while the current address is output by the binary counter.

XNOR gates provide a true (logic 1 or ‘high’) output when both inputs are equal. AND-ing this signal for all bits (LUT9) gives us a pulse when both binary codes are the same. Details about XOR gates as a parity checker can be found in Ref. [9].

The ‘Counter-equals-Latch’ signal is passed to Matrix0 via port P11.

7.7 Digital Compare Logic and Temporary Register

The lower part of Figure 11 (highlighted in Figure 16) shows the DCMP block, the decision-making part of this design:

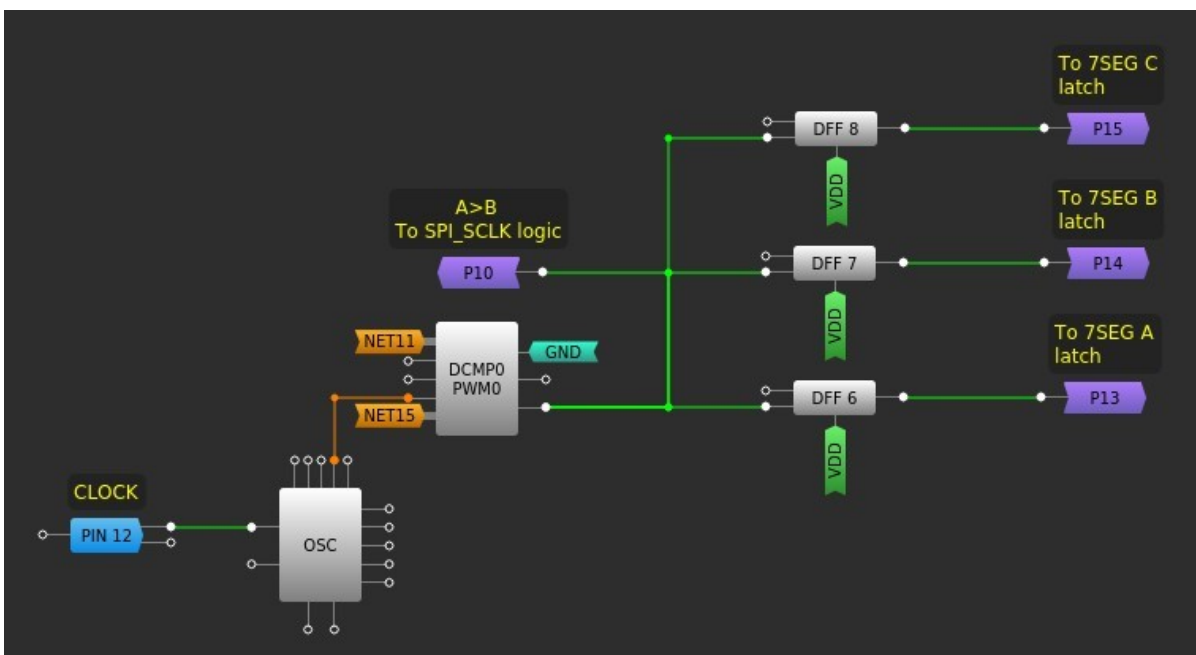


Figure 16: Digital Compare Module and Temporary Register

DFF6, 7, and 8 form a 3-bit register to store the temporary input number “winner” while the loop is running. Input to the Flip-Flops are the 3-bit binary counter outputs, as visible in the global Matrix1 circuit of Figure 11, here skipped for the sake of clarity.

Outputs of this register cannot drive directly the 7-segment display because the value stored here changes during a scan and should be considered ‘valid’ only at the end of the scan itself.

For this reason, the temporary register outputs connect to the Matrix0’s Loop Register via inter-matrix ports P13, P14, and P15.

It is important to observe in Figure 16 that the temporary register is clocked by the DCMP OUT+ output when the ADC-SPI registers comparison results in a new max found.

The same OUT+ signal is passed to Matrix0, SPI CLK Logic, via port P10.

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7.8 Matrix1 Components Properties

The following Figures show the components property windows belonging to Matrix1:

DFF/LATCH6

Mode:

nSET/nRESET option:

Initial polarity:

Q output polarity:

Information

Normal operation

D	CK	Q(t)	nQ(t)
0	↑	0	1
0	↓	t - 1	t - 1
1	↑	1	0
1	↓	t - 1	t - 1

t - 1 - previous state;
nRESET = 0 => Q = 0; nQ = 1;
nRESET = 1 => normal operation;
nSET = 0 => Q = 1; nQ = 0;
nSET = 1 => normal operation;

Figure 17: DFF Properties, Valid for All DFFs Used

DCMP0/PWM0

DCMP/PWM power register:

Function selection:

PD sync to clock:

Clock source:

Clock invert:

PWM & ADC clock source :

PWM data sync with SPI clock:

Duty cycle:

PWM deadband time:

Register 0: MTRX SEL: (0:0) [↗](#)

Register 1: MTRX SEL: (0:1) [↗](#)

Register 2: MTRX SEL: (1:0) [↗](#)

Register 3: MTRX SEL: (1:1) [↗](#)

Connections

IN+ selector:

IN- selector:

Figure 18: DCMP Module Properties

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OSC		
LF OSC	RC OSC	RING OSC
RC OSC power mode:	Force power on	▼
RC OSC frequency:	25 kHz	▼
RC matrix power down:	Disable	▼
RC clock predivider by:	1	▼
'OUT0' second divider by:	1	▼
Clock selector:	EXT. CLK2	▼

Figure 19: OSC Module Properties

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8 Results

To test the implementation, an evaluation board prototype has been constructed, where the 8 analog input voltages are obtained by a series of resistor dividers with TrimPots (as shown in [Figure 20](#)):

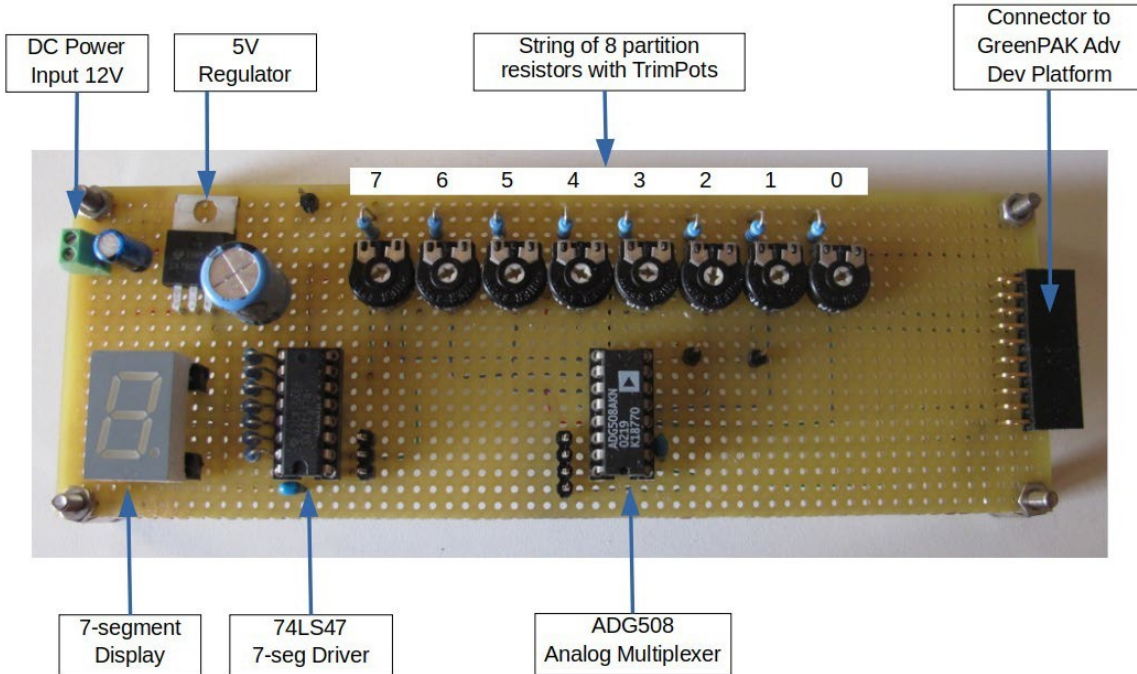


Figure 20: Evaluation Board Prototype of the Max V Finder Design

The multiplexer used is an ADG508, a part that can operate with single supply (12 V).

The 7-segment display driver is a 74LS47. It decodes a parallel input word and directly drives a common-anode 7-segment display.

The evaluation board has a 2x10 right-angle connector to plug directly into a GreenPAK Advanced Development Platform at its expansion connector:

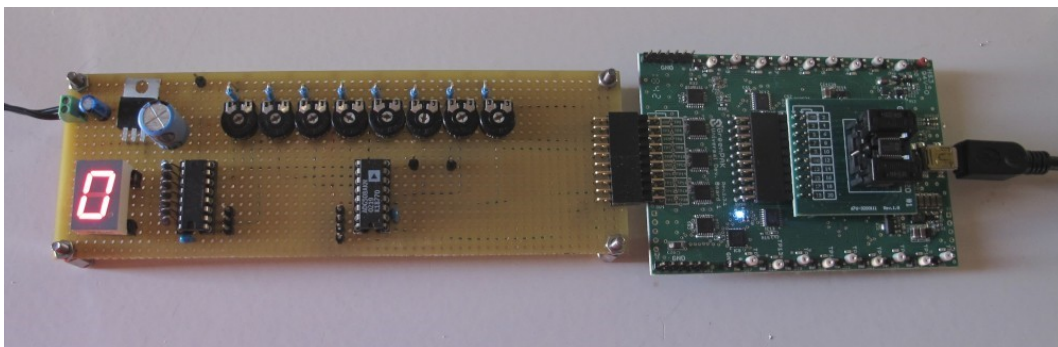


Figure 21: Evaluation Board Connected to GreenPAK Advanced Development Platform

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The conjunction with the GreenPAK Advanced Development Platform makes it very simple to take measurements of the signals for a rapid check. For example, [Figure 22](#) shows a set of signals (respectively CLOCK, ADC INT output, and DCMP OUT+ output) as captured by a HP 54620A Logic Analyzer. Waveforms are triggered by a rising edge of OUT+ signal (on the scope labeled as 'A>B'), hence this is a waveform capture when a new max Voltage is detected among the analog inputs. In fact, it was obtained by rotating one of the TrimPots of the Evaluation Board to increase the corresponding voltage:

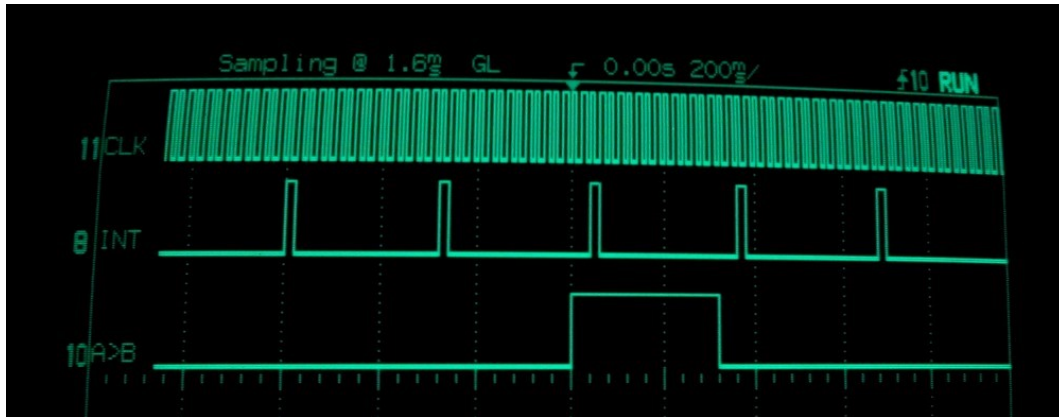


Figure 22: Typical Logic Waveforms at the Detection of Max Voltage

[Figure 23](#) shows the schematic of the Evaluation Board:

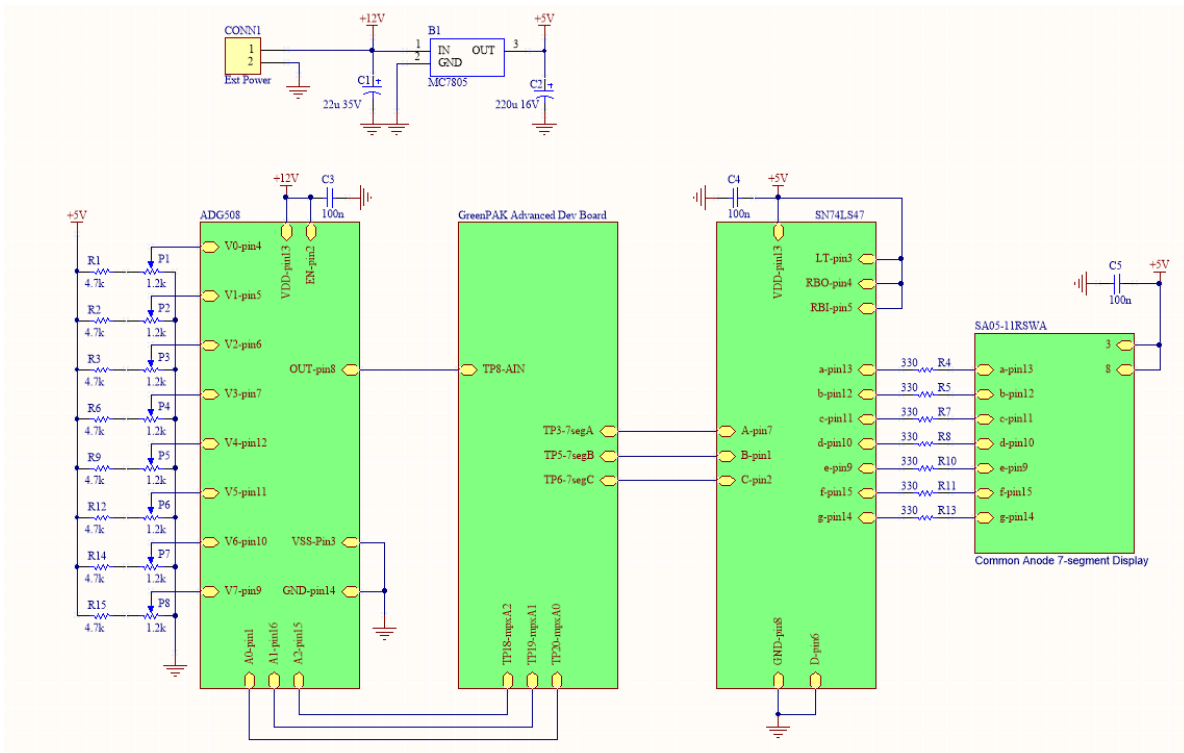


Figure 23: Schematic Diagram of the Evaluation Board

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9 Conclusion

In this application note, we implemented an eight-channel max (or min) voltage finder to be used as a common addition to multi-channel control systems. The presented approach exploits advanced features of the GreenPAK components and shows how it is possible to integrate in one single chip analog and digital functions. Several commercial IC's can be replaced with Dialog GreenPAKs so that the application size and cost can be reduced.

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Revision History

Revision	Date	Description
1.0	17-May-2019	Initial Version

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