Application Note

GreenFET Load Switches: Thermal Considerations for PCB Layout

AN-CM-289

Abstract

This document describes the importance of PCB design with the GreenFET load switches to achieve desired thermal performance. Corresponding calculations and thermal images are provided.

GreenFET Load Switches: Thermal Considerations for PCB Layout

Contents

Figures

1 Terms and Definitions

IC	Integrated Circuit
PCB	Printed Circuit Board

2 References

[1] SLG59H1302C, Datasheet
[2] SLG59H1006V, Datasheet
[3] SLG59M301V, Datasheet
[4] SLG59M1527V, Datasheet
[5] SLG59M1717V, Datasheet
[6] SLG59M1748C, Datasheet
[7] SLG59M1557V, Datasheet
[8] AN-1068, GreenFET and High Voltage GreenFET Load Switch Basics, Application Note

Authors: Andrii Hrypa and Petro Zeykan

3 Introduction

Typically, semiconductors become smaller and pack more functionality/performance per unit area. In the case of semiconductors that are dedicated for load switching, package size is very critical for maximum package power dissipation. Generally speaking, high package power dissipation means the IC generates more heat, and thus its internal temperature increases. Continuous high internal temperature operation can dramatically reduce an IC's long-term reliability, and methods to decrease power dissipation or transfer heat out of the device should be considered. In load switching applications, high-power dissipation may be caused by delivering high load currents (transient or steady-state), non-optimized PCB design, incorrectly selected load switch configuration, or all of the above.

One possible way to improve package heat dissipation is to use a heatsink. Heatsinks are generally made of metals such as aluminum and they are relatively inexpensive to implement. Heatsinks with large surface area have better heat transfer, which reduces an IC's junction temperature. However, this method is not always acceptable because it is not always possible to mount a heatsink on top of an IC. Another way to improve heat transfer on a PCB is to add thermal vias. There are two types of thermal vias. The first and most effective one is a hole drilled through the PCB in the middle of the IC's footprint and filled with a high thermal conductivity metal, such as copper. The second type is thermal vias located around the IC. The heat transfers through thermal vias from the top to the bottom surface of a PCB, which provides greater surface area for heat dissipation. This method may not always be acceptable because for very small packages and WLCSPs (Wafer-level Chip-scale Packages), there is no way to add thermal vias. IC junction temperature can also be reduced by increasing the area of the interconnect traces and contact pads, often manufactured with copper. This method is typically most acceptable in terms of heat transfer and cost. To calculate the amount of package power dissipation and to create proper PCB design, thermal resistance, junction-to-ambient (θ_{JA}) is typically used and often specified in IC datasheets. This application note describes how the surface area of input and output copper traces/contact pads affects the θ_{JA} of representative GreenFET load switches.

4 Thermal Effects and Junction Temperature

The basic principles of thermal study are analogous to electrical behavior. To compare thermal and electrical domains, let's identify the main parameters. Heat is equivalent to the electrical current, temperature is equivalent to the voltage, and thermal resistance is equivalent to the electrical resistance (as shown in Figure 1).

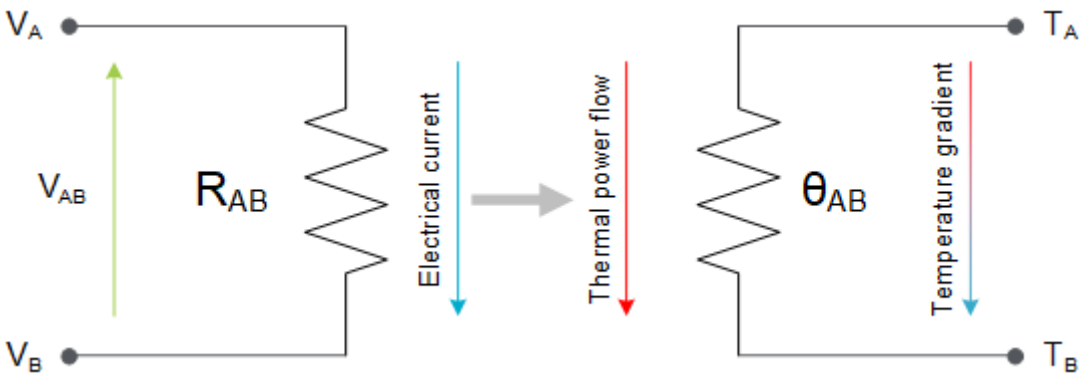


Figure 1. Analogy Between Electrical and Thermal Systems

Each domain is characterized by two main physical parameters. In the electrical domain, current and electrical potential are the main parameters. The current, I, represents the flow of charge carriers moving from a Point A with electrical potential V_A to a Point B with V_B through a path with electrical

resistance R. The difference between them is indicated as V_A-V_B and the relationship between these parameters is represented by the Ohm's law:

$$\Delta V_{AB} = V_A - V_B = I \cdot R_{AB}$$

Similarly, in the thermal domain, P represents heat flow from a place with temperature T_A to another place with temperature T_B. The resistance that impedes the flow is indicated as θ_{AB}. While the relationship in the thermal domain is represented by Fourier's law, a similar relationship to that in the electrical domain can be summarized as:

$$\Delta T_{AB} = T_A - T_B = P \cdot \theta_{AB}$$

Transferring this concept to semiconductor devices, a simplified IC thermal model can be derived. One such model is illustrated in Figure 2, where T_A is the ambient temperature; T_C is the case temperature; T_J signifies junction temperature; T_B represents PCB temperature; θ_{JC} is the junction-to-case thermal resistance; θ_{CA} is the thermal resistance between case and ambient; θ_{JB} is the junction to PCB thermal resistance; θ_{BA} is the thermal resistance between PCB and ambient; and lastly θ_{JA} is the junction-to-ambient thermal resistance.

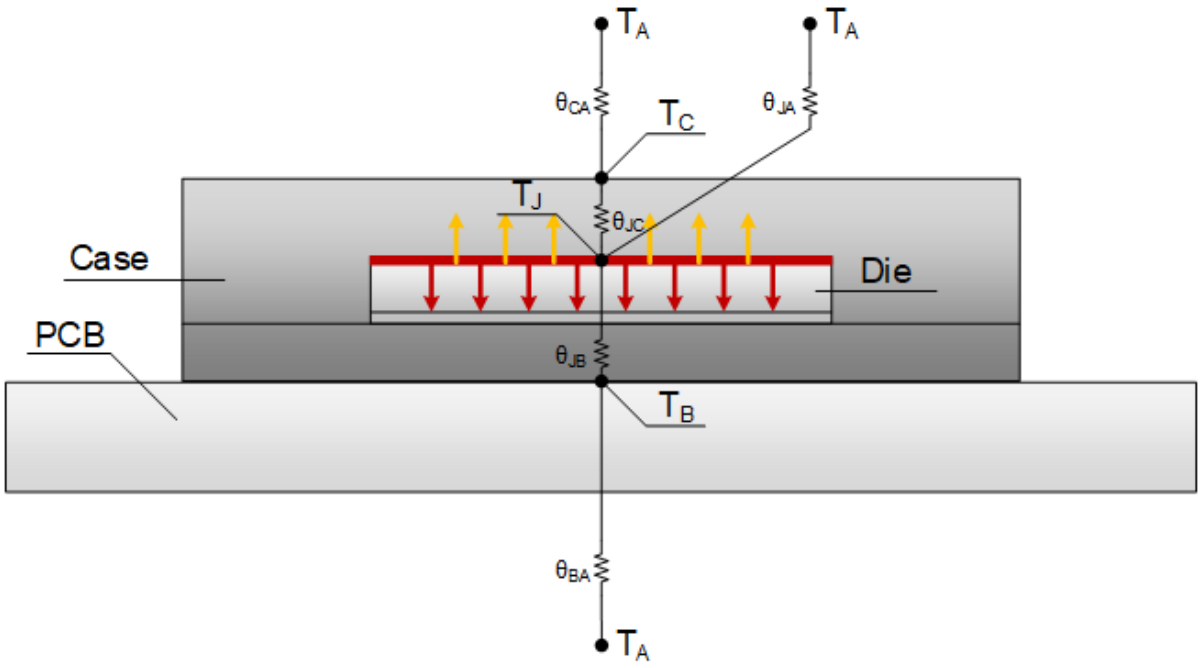


Figure 2. A Simplified Chip Thermal Model

Since thermal conductivity of the IC's package is very low, the heat generated by the silicon die mostly flows through the back side of the IC where the conductivity of the copper is higher. The power generated within the die changes the junction temperature, increasing it according to the thermal resistances and capacitances of the layers involved, from the silicon to the package back side (red arrows in Figure 2).

The term "junction temperature" represents the highest operating temperature of the actual semiconductor in an electronic device. A simplified model is to assume that die's temperature is uniform across its top surface. Across a large die, the model ignores the fact that x-axis and y-axis thermal gradients always exist and can be quite large during high power conditions.

5 The Concept of θ_{JA} Measurements as applied to the GreenFET Load Switches

In the GreenFET load switches, the main component that dissipates most of the heat is the internal n-channel or p-channel power MOSFET. It is well known that the RDS_{ON} of any MOSFET depends on junction temperature. The higher the junction temperature, the larger the MOSFET's RDS_{ON}. When speaking about MOSFETs like a group of thousands of tiny power FET cells connected in parallel, the thermal path between the cells is good, because they are all located on the same die. When the current through a small group of cells increases, those cells heat up. This leads to an increasing of those cells' resistivity, which in turn makes the current flow more through neighboring cells. As a result, thermal gradients decrease, and localized hot spots are minimized. This process is an important physical principle that allows reliable functionality of a parallel array of cells. Considering the above, it can be assumed that the whole die's surface has the same temperature.

To determine the actual θ_{JA}, the temperature difference between an IC's junction temperature, T_J, and the ambient temperature, T_A, is required. To arrive at the IC's junction temperature, it is necessary to have a thermal sensor inside the IC. To measure θ_{JA} with respect to the GreenFET load switches, an RDS_{ON} vs. T_A dependency is used. For this purpose, the GreenFET load switch is inserted into a controlled temperature chamber that allows precise control of the ambient temperature T_A. To avoid IC self-heating, a small amount of current is applied while measuring the RDS_{ON} parameter. Keeping the IC at each temperature for approximately 5 minutes and avoiding any self-heating allows the IC's die temperature to be close to the preset ambient temperature. Having established an RDS_{ON} versus ambient temperature dependence, the data can be plotted on a chart (Figure 3). Using this chart, an equation for approximating junction temperature can be determined:

$$T_J = f(\mathrm{RDS_{ON}})$$

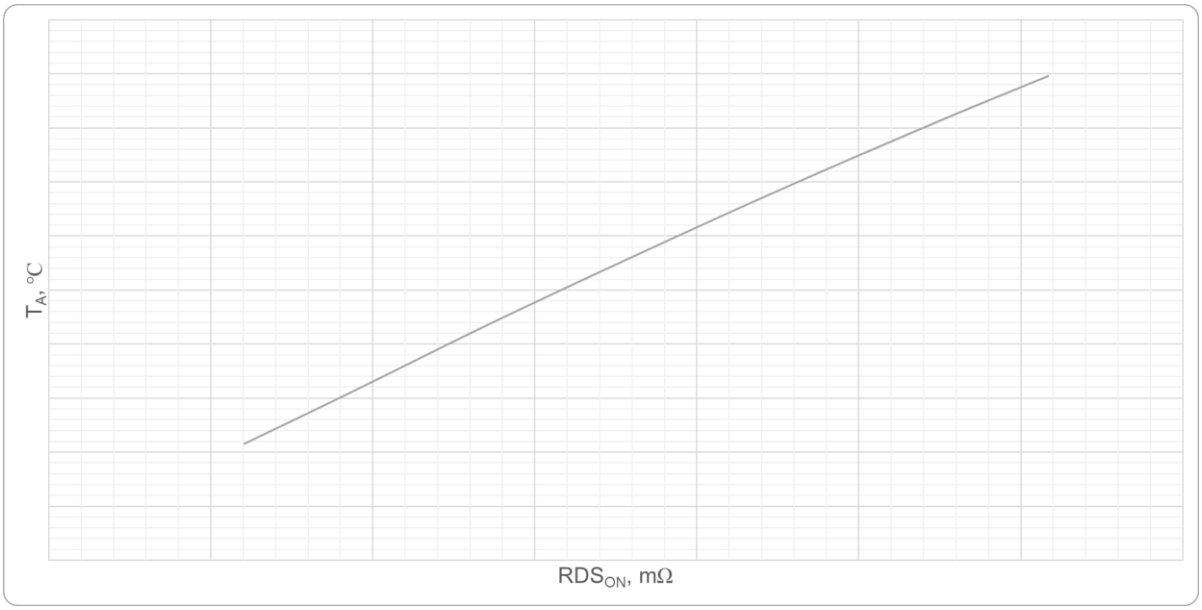


Figure 3. Plotting RDS_{ON} vs. T_A to Obtain Junction Temperature

The next step is to measure the RDS_{ON} versus load current (or I_{DS}) at a fixed ambient temperature. To do this, the IC is held at each particular load current for approximately 5 minutes and then the MOSFET's RDS_{ON} is measured. Using the $T_J = f(\mathrm{RDS_{ON}})$ equation from above, the junction temperature for each RDS_{ON} resistance is calculated. Now, a $\Delta T = T_J - T_A$ temperature differential and package power dissipation of the IC for each load current are calculated and the corresponding curve is plotted as shown in Figure 4.

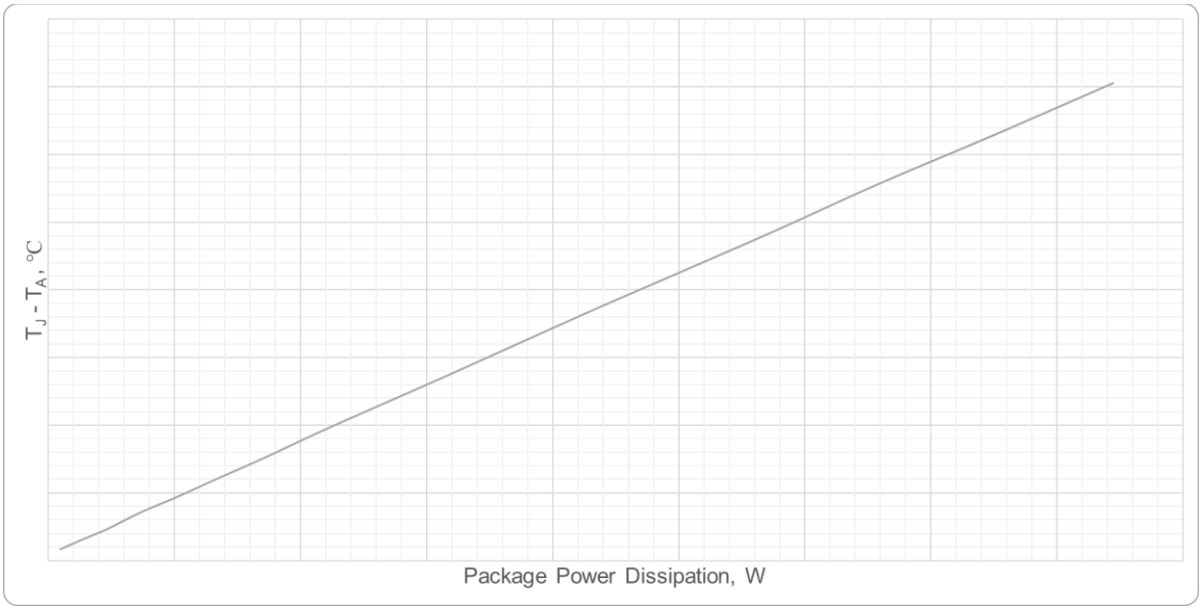


Figure 4. Plotting of Package Power Dissipation vs. ΔT to Obtain Thermal Resistance

Using a linear approximation, an equation like $\Delta T = P \cdot x + b$ can be applied. Taking into consideration that $\Delta T = T_J - T_A = P \cdot \theta_{JA}$, it can be affirmed that linear coefficient x (the slope of the line) in our approximation corresponds to an IC's thermal resistance.

As mentioned before, thermal resistance is affected by ambient conditions, PCB design, and other factors. In this application note, three PCB designs were used to obtain θ_{JA}: 0 in^2, 0.25 in^2, and 0.5 in^2 under each input and output trace. Also, the corresponding thermal distribution for each PCB is provided. For θ_{JA} measurements, an ambient T_A = 50 °C was used. For the thermal distribution test, the ambient temperature was T_A = 25 °C. In each of the three designs, the load switch's PCB dimensions were 6.3 cm x 6.3 cm (2.5 in x 2.5 in) physical dimensions. In this application note, a Type-A PCB is a PCB design with IC footprints and traces only, and a Type-B PCB is a PCB design with copper pads under the power terminals.

6 Case #1: The SLG59H1302C in a 5 mm^2, 28-Lead WLCSP

The SLG59H1302C is a 130 V surge-protected, 28 V tolerant power splitter with two high-current switches and a 0.1 A capable LDO in 28-ball WLCSP. With independent control for each channel, the SLG59H1302C contains a 6 A capable, 12 mΩ nFET switch for the BUS-to-OUT path and a reverse-blocking 6 A capable, 24 mΩ nFET switch for the BUS-to-SYS path. An internal, “always ON” LDO is 0.1 A capable and can be used to supply power to downstream devices when the BUS terminal voltage is higher than 2.7 V. The SLG59H1302C is fully specified over the industrial -40 °C to 85 °C temperature range.

In this example, the BUS-to-SYS conduction path is evaluated. In this case, Type-A and Type-B PCBs were created where the Type-B PCB has 0.5 in^2 copper area under the power traces. Both PCBs are presented in Figure 5.

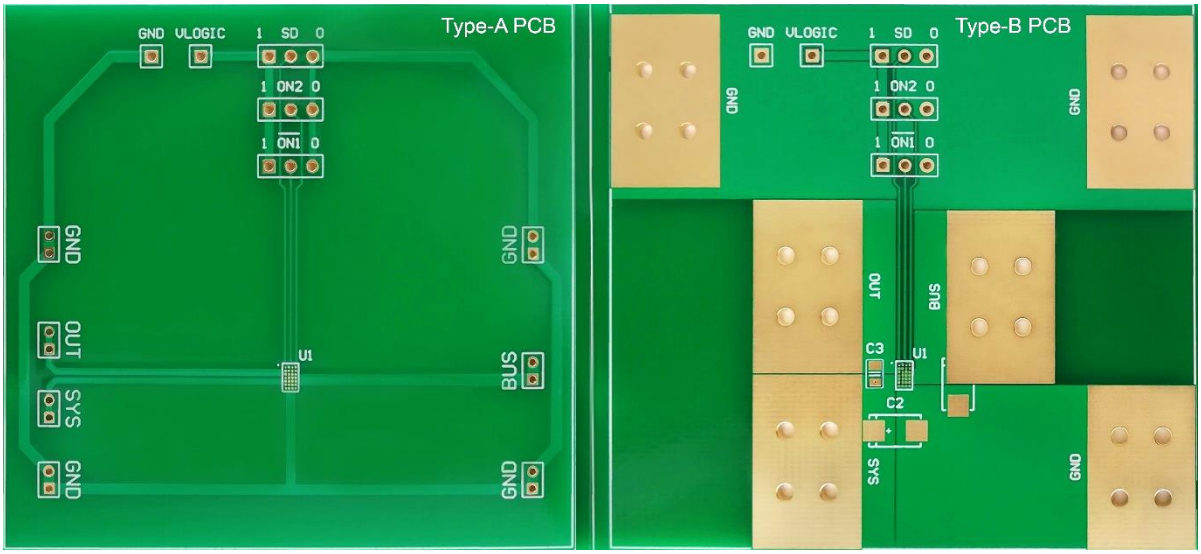


Figure 5. Type-A (left) and Type-B (right) PCB Evaluation Boards for θ_{JA} Measurements of the SLG59H1302C in a 5 mm², 28-Lead WLCSP Package

Thermal resistance is calculated using a technique which is described in Section 5. The resulting graph is illustrated in Figure 6.

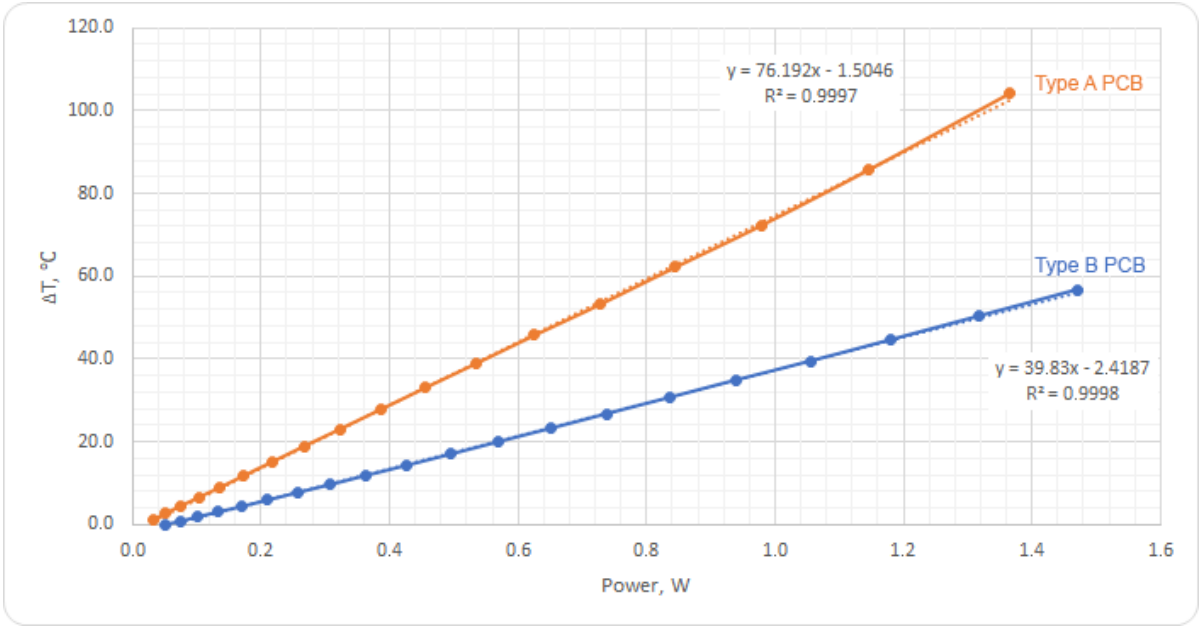


Figure 6. Package Power Dissipation vs. Temperature Difference for the SLG59H1302C in a 5 mm², 28-Lead WLCSP Package

From graph above, θ_{JA} values for both types of PCBs are obtained from the slope of the line equations. Thus, the θ_{JA} of 5 mm², 28-Lead WLCSP Package mounted on a Type-A PCB is 76.2 ℃/W and, for the same IC mounted on a Type-B PCB, θ_{JA} is 39.8 ℃/W. Obviously, an IC mounted on PCB with higher thermal resistance will heat more under the same load conditions. This result is well correlated to the thermal images in Figure 7. and Figure 8.

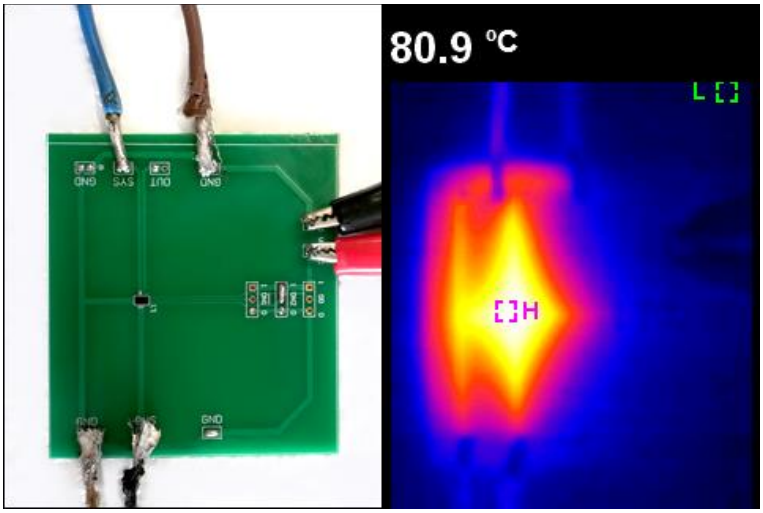


Figure 7. Visible (left) and Thermal (Right) Images of the SLG59H1302C in a 5 mm², 28-Lead WLCSP Mounted on a Type-A PCB.T_A = 25 °C, V_{BUS} = 5 V, I_{LOAD} = 4 A.

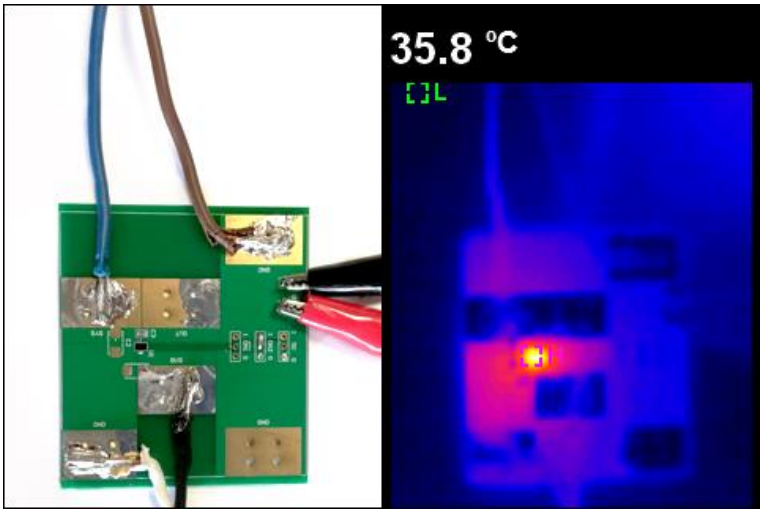


Figure 8. Visible (left) and Thermal (right) Images of the SLG59H1302C in a 5 mm², 28-Lead WLCSP Mounted on a Type-B PCB.T_A = 25 °C, V_{BUS} = 5 V, I_{LOAD} = 4 A.

Applying a 6 A load current triggers the IC's over-temperature protection when mounted on a Type-A PCB. In the case where the IC is mounted on a Type-B PCB, the IC's die temperature increases to 47.2 ℃.

7 Case #2: The SLG59H1006V in a 4.8 mm², 18-Lead STQFN Package

The SLG59H1006V is a high-performance, self-powered 13.1 mΩ NMOS load switch designed for all 4.5 V to 22 V power rails up to 5 A. Using a proprietary MOSFET design, the SLG59H1006V achieves a stable 13.1 mΩ RDS_{ON} across a wide input voltage range. In combining novel FET design and copper pillar interconnects, the SLG59H1006V package also exhibits a low thermal resistance

for high-current operation. Designed to operate over a -40 °C to 85 °C range, the SLG59H1006V is available in a low thermal resistance 1.6 x 3.0 mm package.

Type-A and Type-B PCB designs created for this package type are illustrated in Figure 9. With respect to the Type-B PCB the copper contact area under each VIN and VOUT terminal was 0.5 in^2.

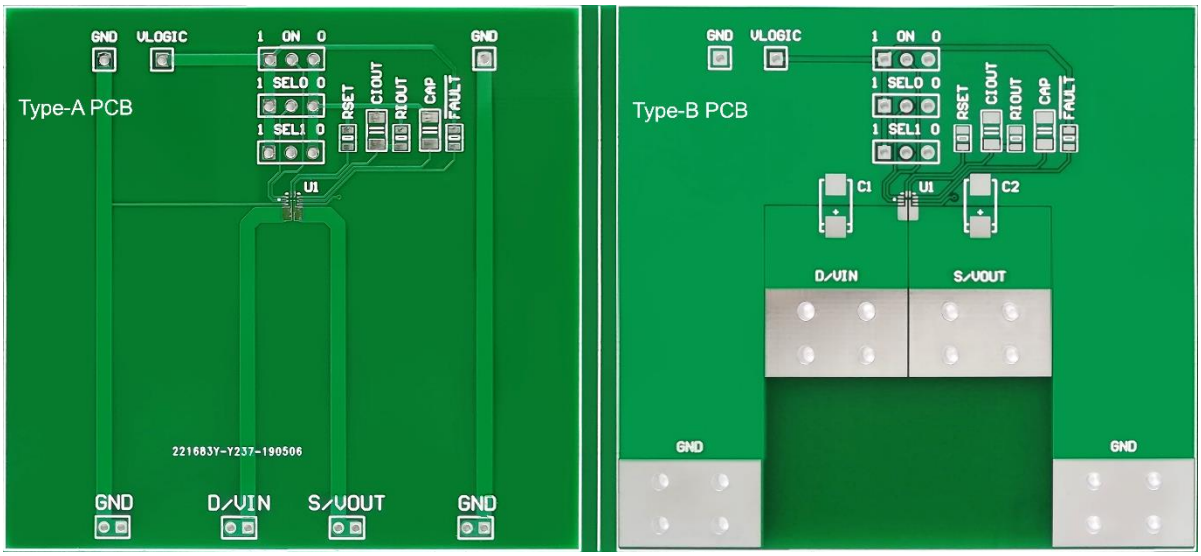


Figure 9. Type-A (left) and Type-B (right) PCB Evaluation Boards for θ_{JA} Measurements of the SLG59H1006V in a 4.8 mm^2, 18-Lead STQFN Package

Plotting power dissipation vs. temperature difference, shown in Figure 10, the thermal resistances for Type-A and Type-B PCBs for the SLG59H1006V's 18-Lead STQFN Package can be obtained.

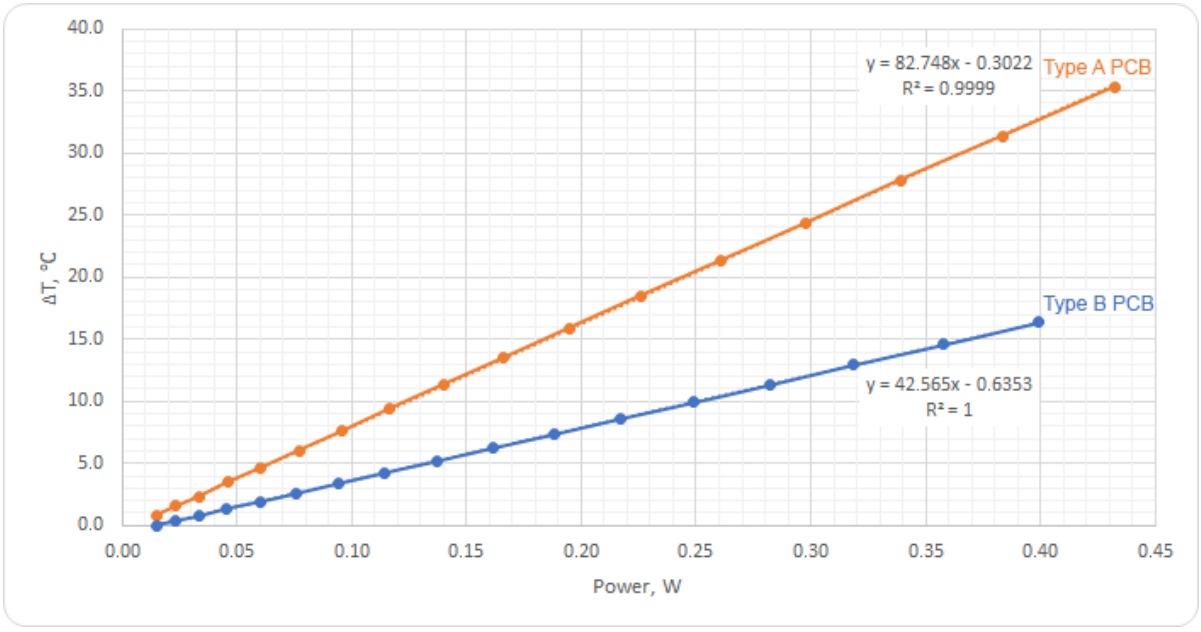


Figure 10. Package Power Dissipation vs. Temperature Difference for the SLG59H1006V in a 4.8 mm^2, 18-Lead STQFN Package

From Figure 10, SLG59H1006V's θ_{JA} when mounted onto a Type-A PCB is 82.7 °C/W. When mounted on a Type-B PCB, its thermal resistance becomes 42.6 °C/W. Before thermal distribution

measurements were taken, the load condition was applied for at least 5 minutes. Visible and thermal spectrum images for the SLG59H1006V when mounted on Type-A and Type-B PCBs are shown in Figure 11 and Figure 12.

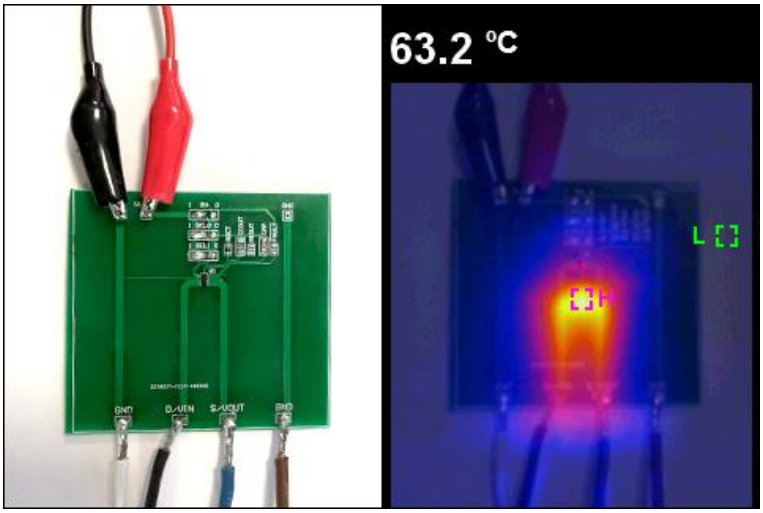


Figure 11. Visible (left) and Thermal (right) Images of the SLG59H1006V in a 4.8 mm², 18-Lead STQFN Package mounted on a Type-A PCB. T_A = 25 °C, V_{IN} = 22 V, I_{LOAD} = 5 A.

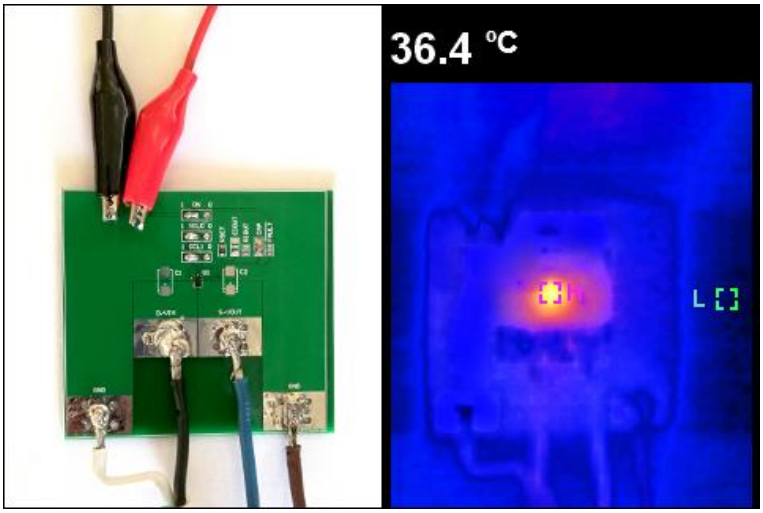


Figure 12. Visible (left) and Thermal (right) Images of the SLG59H1006V in a 4.8 mm², 18-Lead STQFN Package Mounted on a Type-B PCB. T_A = 25 °C, V_{IN} = 22 V, I_{LOAD} = 5 A.

As can be noticed, increasing the copper area for each VIN and VOUT pads leads to better thermal dissipation and, as a result, to lower the GreenFET load switches temperature. The IC temperature reduces from 63.2 ℃ to 36.4 ℃.

8 Case #3: The SLG59M301V in a 3 mm², 8-Lead TDFN Package

The SLG59M301V is a high performance 8.5 mΩ, 4 A single-channel nFET load switch which can operate with a 2.5 V to 5.5 V V_{DD} supply to switch power rails from as low as 0.85 V up to the supply voltage. Fully specified over the -40 °C to 85 °C temperature range, the SLG59M301V is packaged in a space-efficient, low thermal resistance, TDFN package.

With respect to the Type-B PCB the copper contact area under each Drain and Source terminal was 0.5 in^2. Type-A and Type-B PCBs are illustrated in Figure 13.

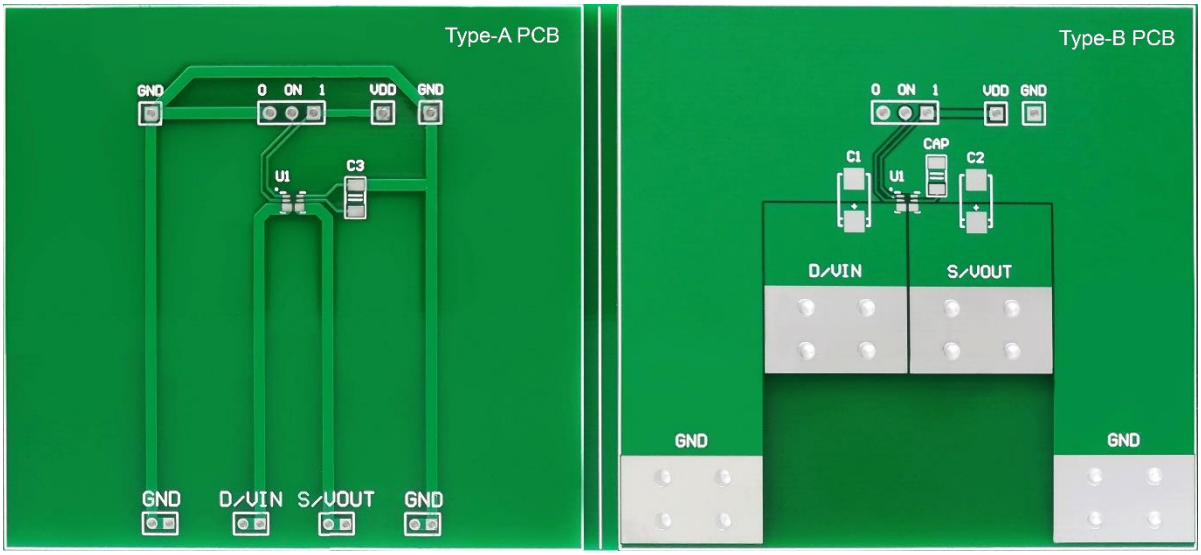


Figure 13. Type-A (left) and Type-B (right) PCB Evaluation Boards for θ_{JA} Measurements of the SLG59M301V in a 3 mm^2, 8-Lead TDFN Package

Using the technique already in use, a package power dissipation vs. ΔT dependence was built and is shown in Figure 14.

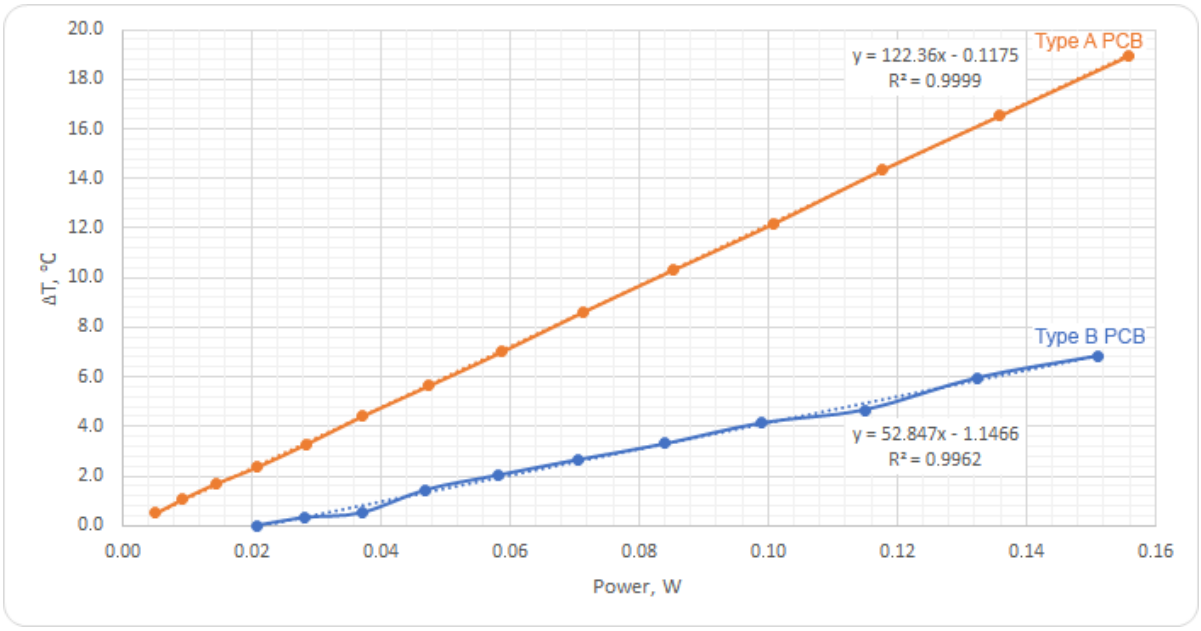


Figure 14. Package Power Dissipation vs. Temperature difference for the SLG59M301V in a 3 mm^2, 8-Lead TDFN Package

After curve fitting, the SLG59M301V's thermal resistances for both types of PCBs can be obtained. For the Type-A PCB design, θ_{JA} is 122.4 °C/W and, for Type-B PCB, θ_{JA} is 52.8 °C/W.

Corresponding visible and thermal spectrum images for both PCBs are presented in Figure 15 and Figure 16.

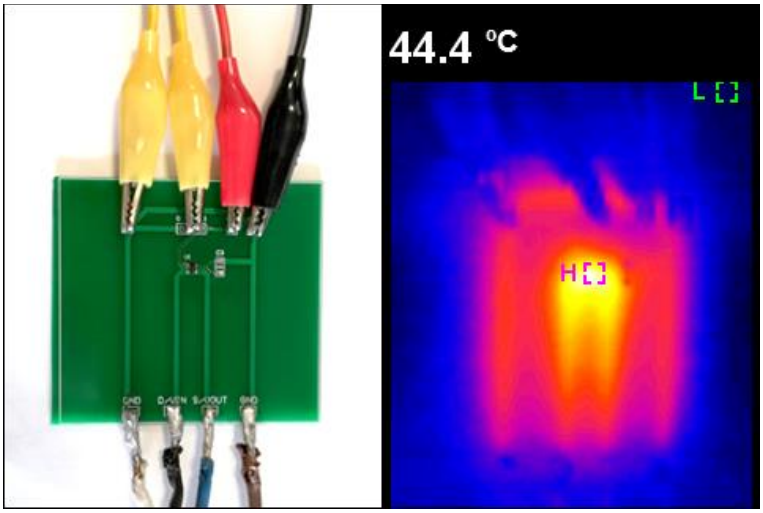


Figure 15. Visible (left) and Thermal (right) Images of the SLG59M301V in a 3 mm², 8-Lead TDFN Package Mounted on a Type-A PCB. T_A = 25 °C, V_{DD} = V_{IN} = 5.5 V, I_{LOAD} = 4 A.

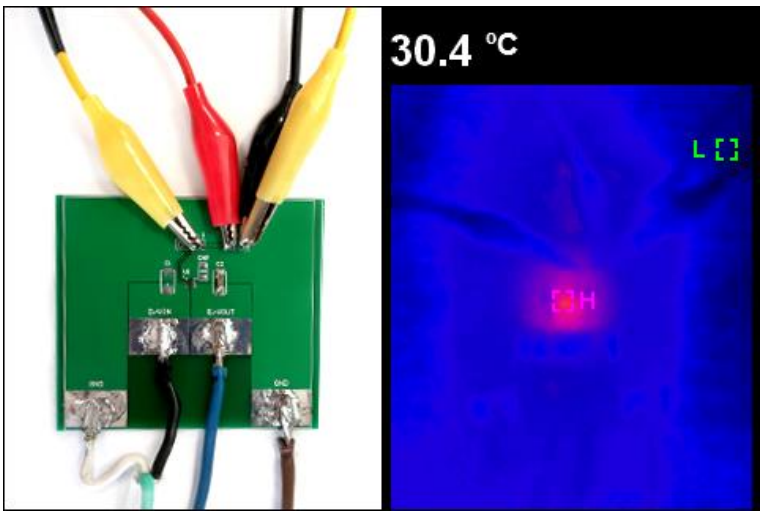


Figure 16. Visible (left) and Thermal (right) Images of the SLG59M301V in a 3 mm², 8-Lead TDFN Package Mounted on a Type-B PCB. T_A = 25 °C, V_{DD} = V_{IN} = 5.5 V, I_{LOAD} = 4 A.

As can be observed, the IC temperature decreases from 44.4 ℃ to 30.4 ℃.

9 Case #4: The SLG59M1568V in a 3 mm², 14-Lead STDFN Package

The SLG59M1568V is designed for load switching applications. It comes with one 9 A rated MOSFET switched on by the ON control pin. The appropriate PCBs have been created and illustrated in Figure 17.

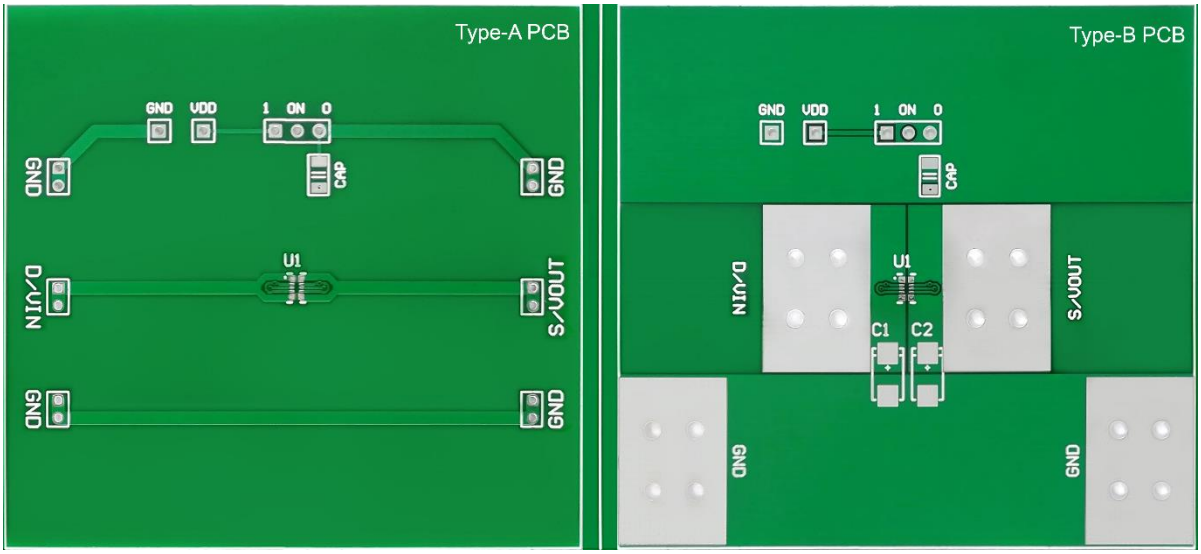


Figure 17. Type-A (left) and Type-B (right) PCB Evaluation Boards for θ_{JA} Measurements of the SLG59M1568V in a 3 mm², 14-Lead STDFN Package

From Figure 18, the SLG59M1568V's 3 mm², 14-lead STDFN's thermal resistance when mounted on a Type-A PCB is 125 ℃/W and when mounted on a Type-B PCB is 51.4 ℃/W.

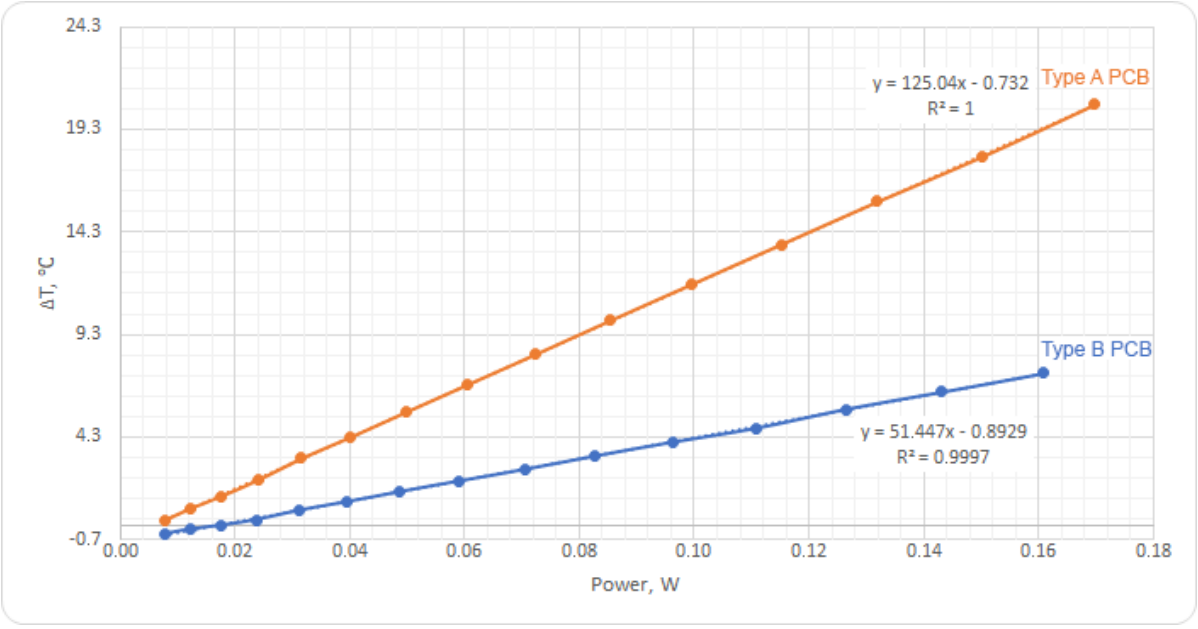


Figure 18. Package Power Dissipation vs. Temperature Difference for the SLG59M1568V in a 3 mm², 14-Lead STDFN Package

As can be observed from its thermal image (shown in Figure 19), the STDFN's case temperature rises to 71.7 ℃ when using the Type-A PCB. For the Type-B PCB, the case temperature rises to 35.5 ℃ (Figure 20).

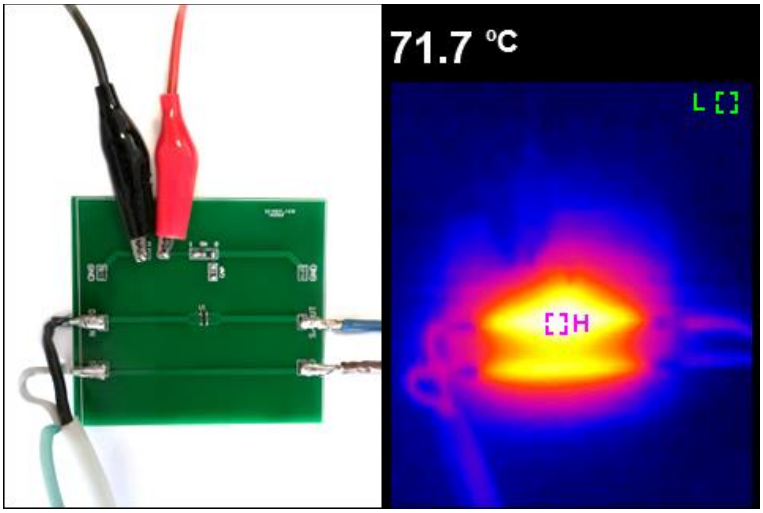


Figure 19. Visible (left) and Thermal (right) images of the SLG59M1568V in a 3 mm², 14-Lead STDFN Package mounted on a Type-A PCB. T_A = 25 °C, V_{IN} = 5 V, I_{LOAD} = 6.5 A.

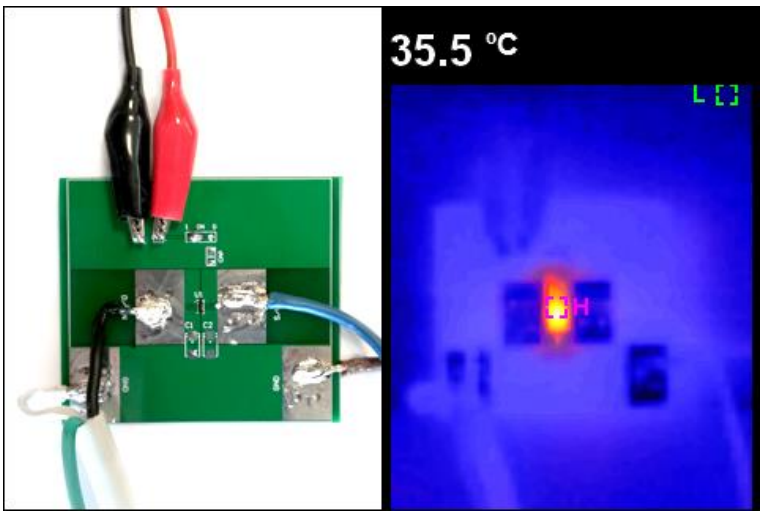


Figure 20. Visible (left) and Thermal (right) Images of the SLG59M1568V in a 3 mm²,14-Lead STDFN Package Mounted on a Type-B PCB. T_A = 25 °C, V_{IN} = 5 V, I_{LOAD} = 6.5 A.

Applying 9 A of I_{LOAD} forces this IC into overtemperature protection in the case of type-A PCB and for type-B PCB, the IC temperature rises to 41.1 ℃.

10 Case #5: The SLG59M1717V in a 4 mm², 16-Lead STQFN Package

Operating from a 3.0 V to 5.5 V power supply and fully specified over the -40 °C to 85 °C Industrial temperature range, the SLG59M1717V is a high-performance 4 mΩ, 5 A single-channel nFET load switch designed for all 0.8 V to 5.5 V load switch applications. The SLG59M1717V features adjustable inrush current control which is achieved by adjusting the V_{OUT} slew rate with an external capacitor. Using a proprietary MOSFET design, the SLG59M1717V achieves a stable 4 mΩ RDS_{ON} across a wide input/supply voltage range. The SLG59M1717V also incorporates resistor-adjustable current limiting as well as thermal protection.

Type-A and Type-B PCBs designed for this GreenFET load switch are illustrated in Figure 21.

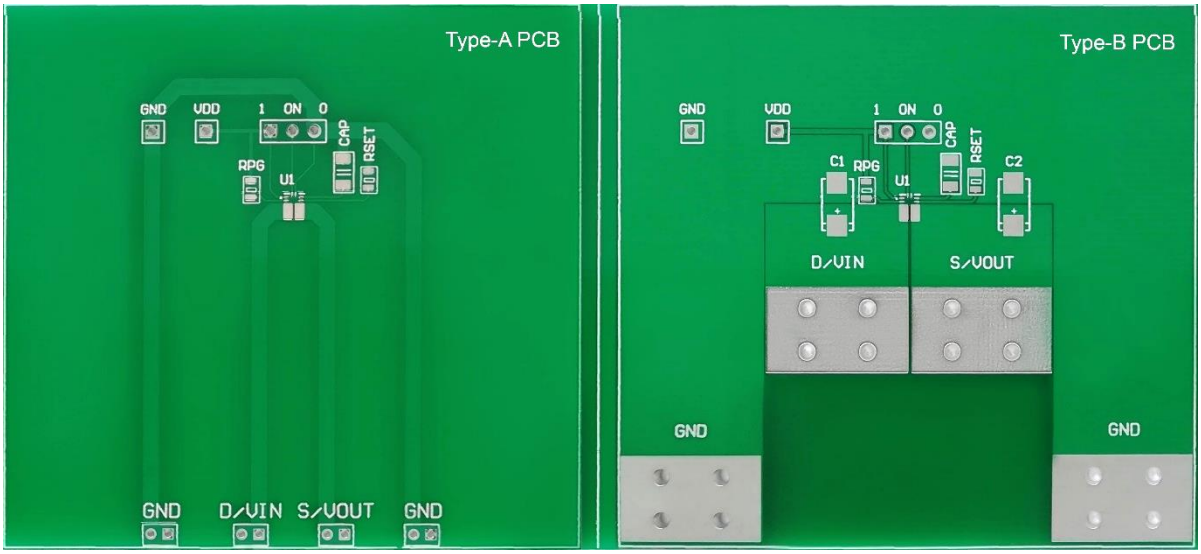


Figure 21. Type-A (left) and Type-B (right) PCB Evaluation boards for θ_{JA} Measurements of the SLG59M1717V in a 4 mm², 16-Lead STQFN Package

For both Type-A and Type-B PCBs, the STQFN's thermal resistance can be obtained from Figure 22. For the SLG59M1717V's STQFN package, the thermal resistance is 148.1 ℃/W for Type-A PCB, and 45.3 ℃/W for Type-B PCB.

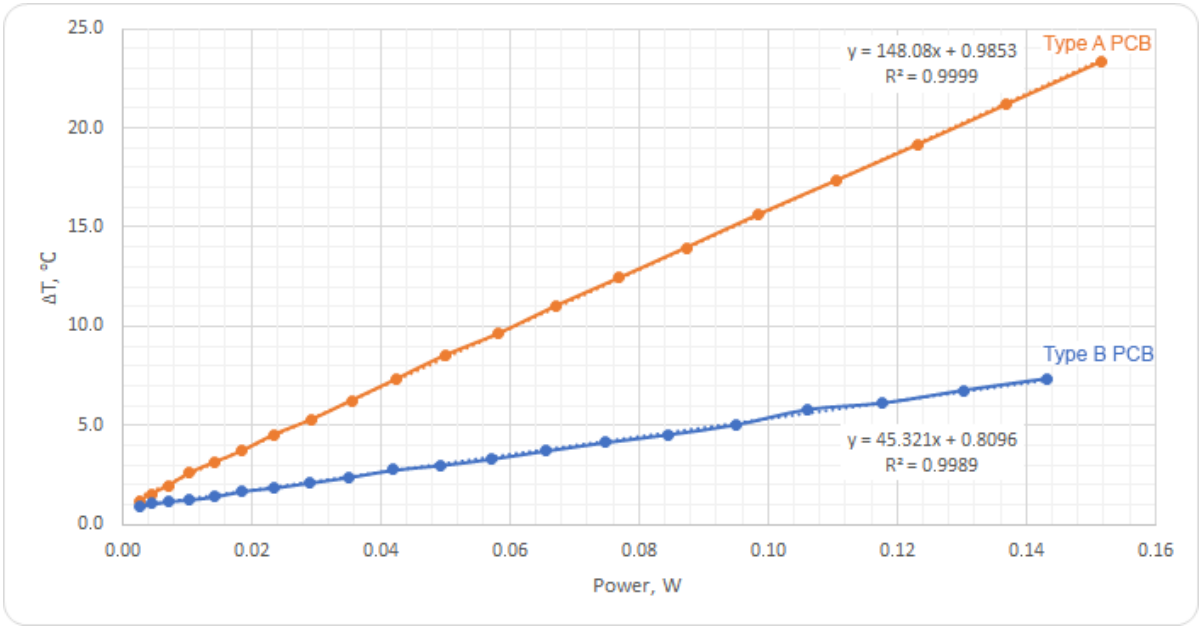


Figure 22. Package Power Dissipation vs. Temperature Difference for the SLG59M1717V in a 4 mm², 16-Lead STQFN Package.

With respect to the Type-A PCB design, the 148.1 ℃/W thermal resistance causes the case temperature to rise to 48.4 ℃ under 5 A load at 5.5 V of input voltage (Figure 23).

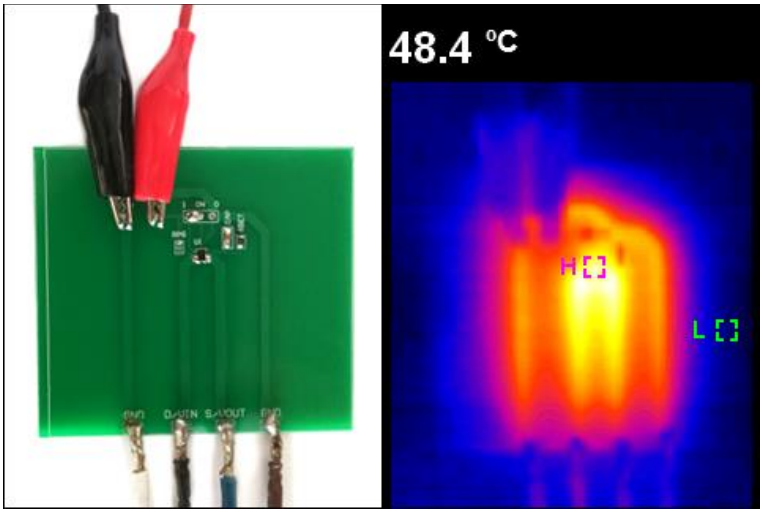


Figure 23. Visible (left) and Thermal (right) Images of the SLG59M1717V in a 4 mm², 16-Lead STQFN Package Mounted on a Type-A PCB. T_A = 25 °C, V_{DD} = V_{IN} = 5.5 V, I_{LOAD} = 5 A.

With respect to the Type-B PCB design, the 45.3 °C/W thermal resistance causes the case temperature to rise to 29.8 °C under the same load condition (Figure 24).

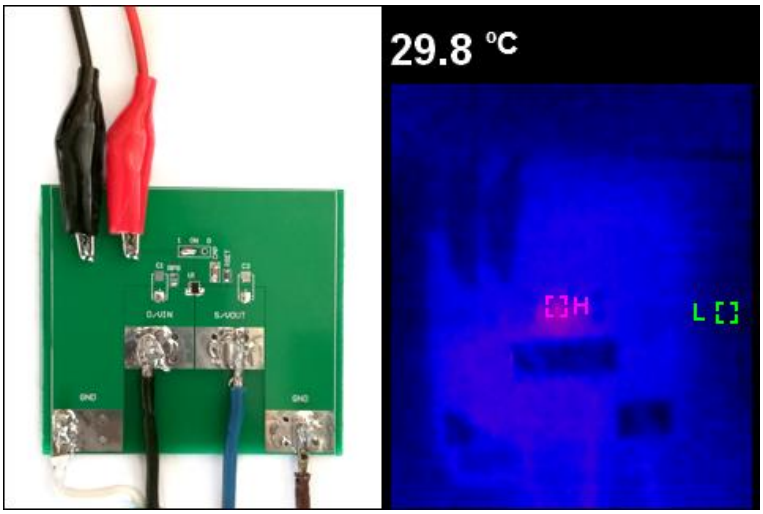


Figure 24. Visible (left) and Thermal (right) Images of the SLG59M1717V in a 4 mm², 16-Lead STQFN Package Mounted on a Type-B PCB. T_A = 25 °C, V_{DD} = V_{IN} = 5.5 V, I_{LOAD} = 5 A.

11 Case #6: The SLG59M1748C in a 0.64 mm², 4-Pin WLCSP

Operating from a 1.6 V to 5 V power supply, the SLG59M1748C is a self-powered, high-performance, 36 mΩ pFET load switch designed for high-side load switching applications up to 2.2 A.

Since this GreenFET load switch is very small (a 0.8 mm x 0.8 mm WLCSP), its Type-B PCB has only 0.25 in² copper contact pads for each VIN and VOUT terminals (as shown in Figure 25).

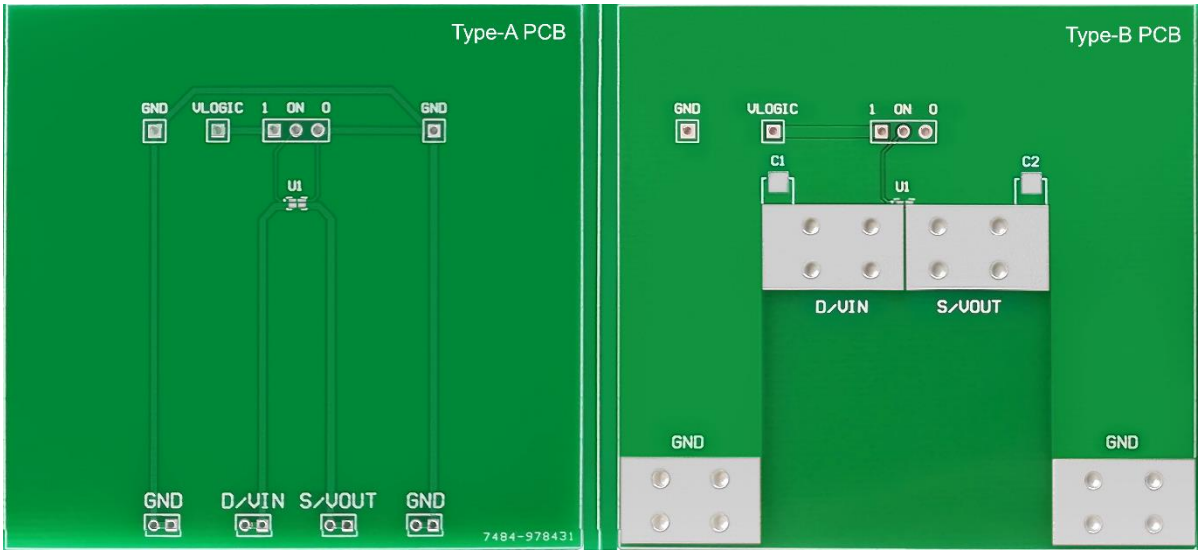


Figure 25. Type-A (left) and Type-B (right) PCB Evaluation Boards for θ_{JA} Measurements of the SLG59M1748C in a 0.64 mm², 4-Pin WLCSP Package

After curve fitting (as shown in Figure 26), the WLCSP's thermal resistances can be obtained. With respect to a Type-A PCB design, the WLCSP's thermal resistance is 198.4 ℃/W. When the WLCSP is mounted on a Type-B PCB, the thermal resistance becomes 99.7 ℃/W.

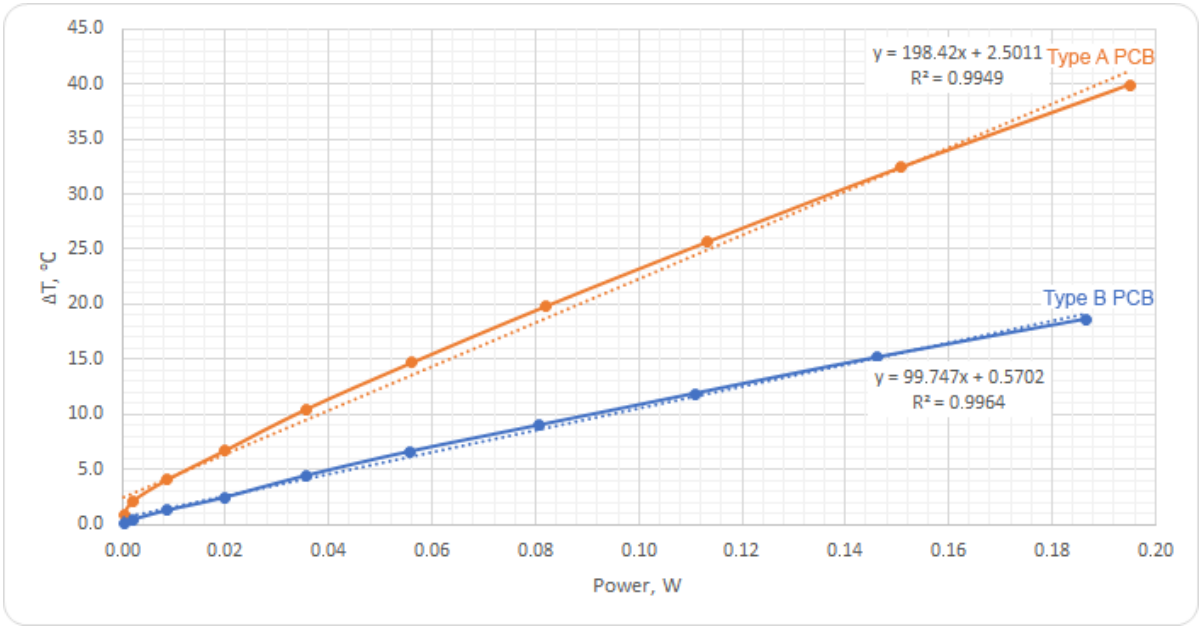


Figure 26. Package Power Dissipation vs. Temperature Difference for the SLG59M1748C in a 0.64 mm², 4-Pin WLCSP Package

With a 2.2 A load at V_{IN} = 5 V, the WLCSP's die temperature when the GreenFET load switch is mounted on a Type-A PCB rises to almost 50 ℃. (as shown in Figure 27)

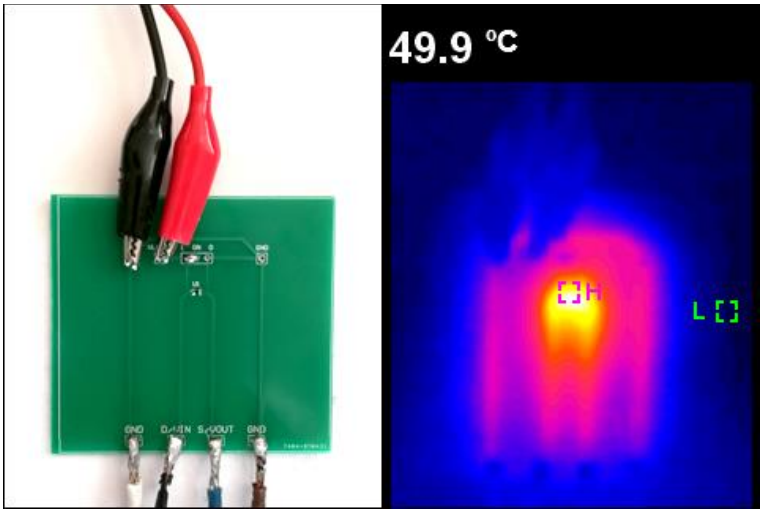


Figure 27. Visible (left) and Thermal (Right) Images of the SLG59M1748C in a 0.64 mm², 4-Pin WLCSP Package Mounted on a Type-A PCB. T_A = 25 °C, V_{IN} = 5 V, I_{LOAD} = 2.2 A.

Operating under the same load conditions, the WLCSP's die temperature when the GreenFET load switch is mounted on a Type-B PCB rises to 29 ℃ (Figure 28).

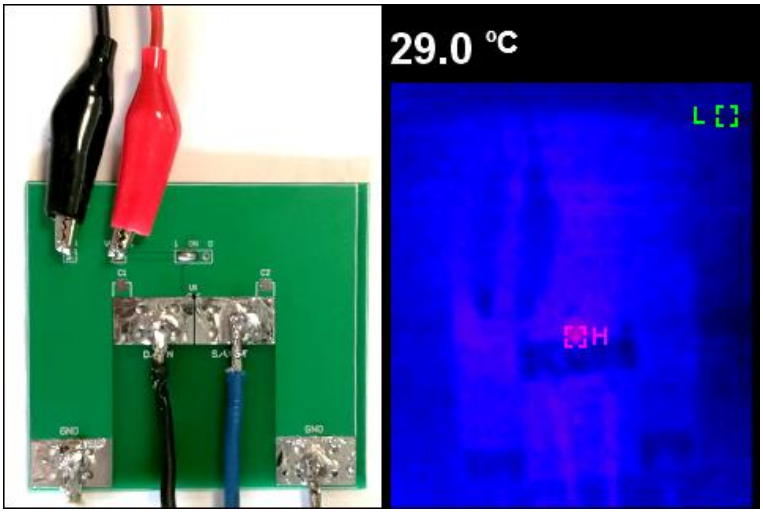


Figure 28. Visible (left) and Thermal (Right) Images of the SLG59M1748C in a 0.64 mm², 4-Pin WLCSP Package Mounted on a Type-B PCB. T_A = 25 °C, V_{IN} = 5 V, I_{LOAD} = 2.2 A.

12 Case #7: The SLG59M1557V in a 1 mm², 4-Lead STDFN Package

The SLG59M1557V is designed for load switching applications with ultra-low quiescent current. The part comes with one 28.5 mΩ 1.0 A rated P-channel MOSFET controlled by a single ON control pin. The product is packaged in an ultra-small 1.0 x 1.0 mm package.

Figure 29 shows the PCBs which have been created to test this type of packages. For the Type-B PCB design, the copper contacts pads were 0.25 in² under each VIN and VOUT terminals.

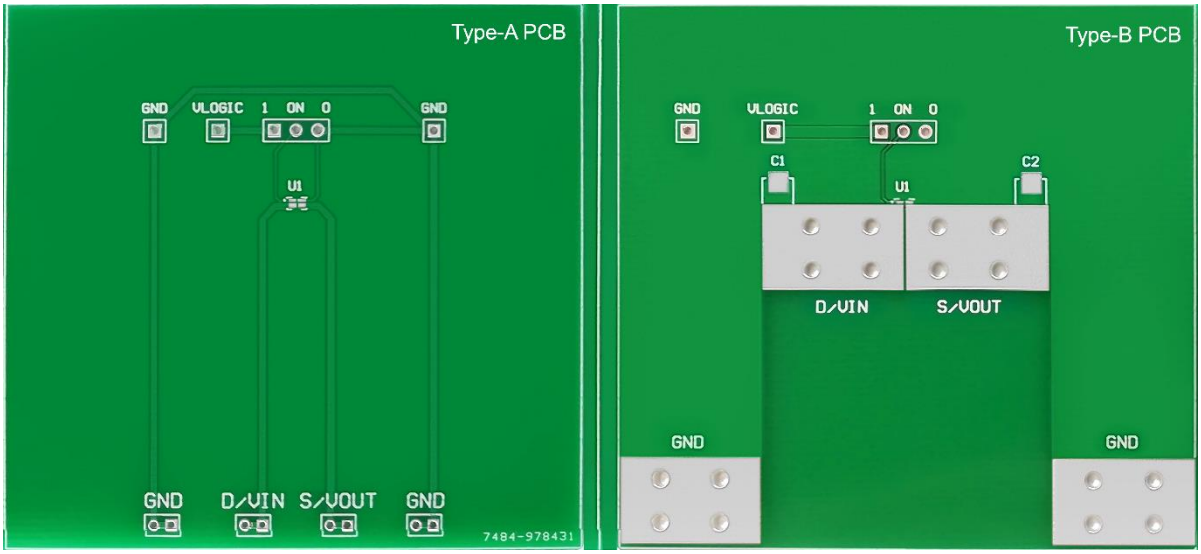


Figure 29. Type-A (left) and Type-B (right) PCB Evaluation Boards for θ_{JA} Measurements of the SLG59M1557V in a 1 mm², 4-Lead STDFN Package

Based on the results obtained using these PCBs, thermal resistances were calculated after curve fitting was performed (as shown in Figure 30). With respect to Type-A PCB design, the SLG59M1557V's STDFN package thermal resistance was 218.5 °C/W. For the Type-B PCB design, the thermal resistance measured 99.1 °C/W.

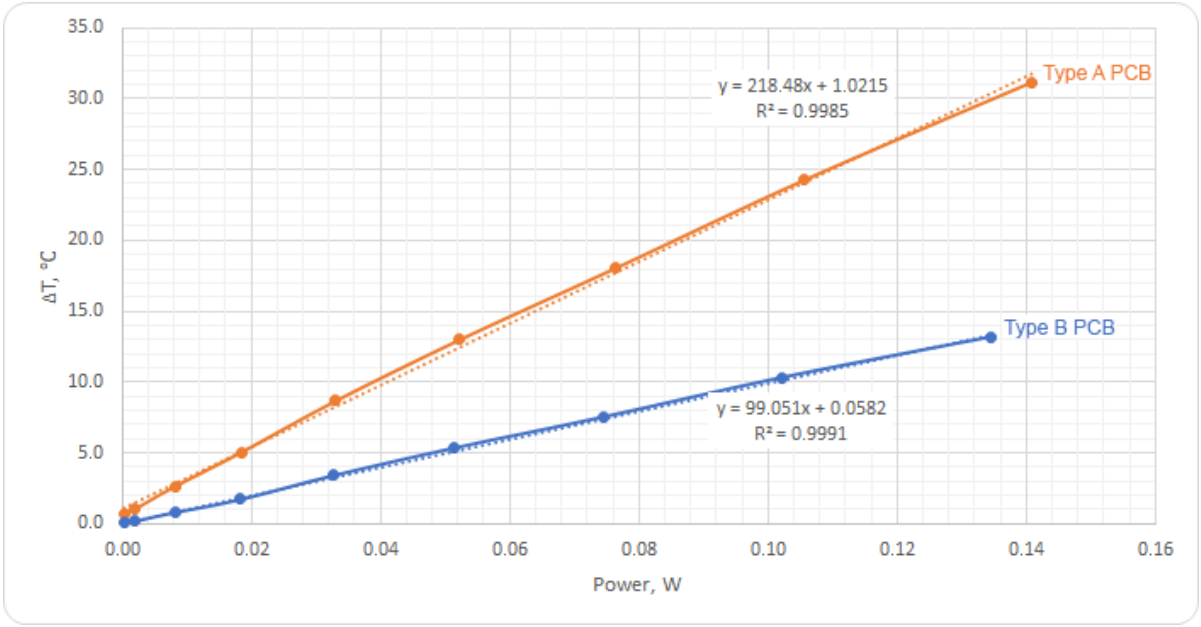


Figure 30. Package Power Dissipation vs. Temperature Difference for the SLG59M1557V in a 1 mm², 4-Lead STDFN Package

Under a 1 A load current at V_{IN} = 5 V, the visible and thermal spectrum images of the SLG59M1557V are shown in Figure 31 and Figure 32.

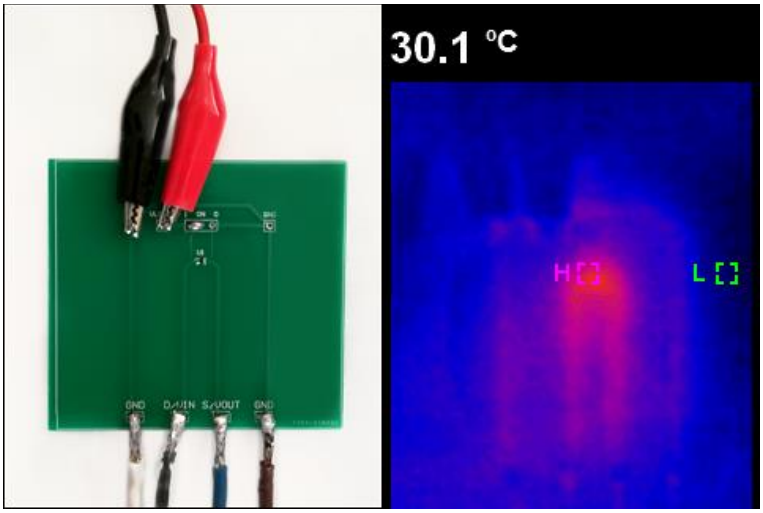


Figure 31. Visible (left) and Thermal (Right) Images of the SLG59M1557V in a 1 mm², 4-Lead STDFN Package Mounted on a Type-A PCB. T_A = 25 °C, V_{IN} = 5 V, I_{LOAD} = 1 A.

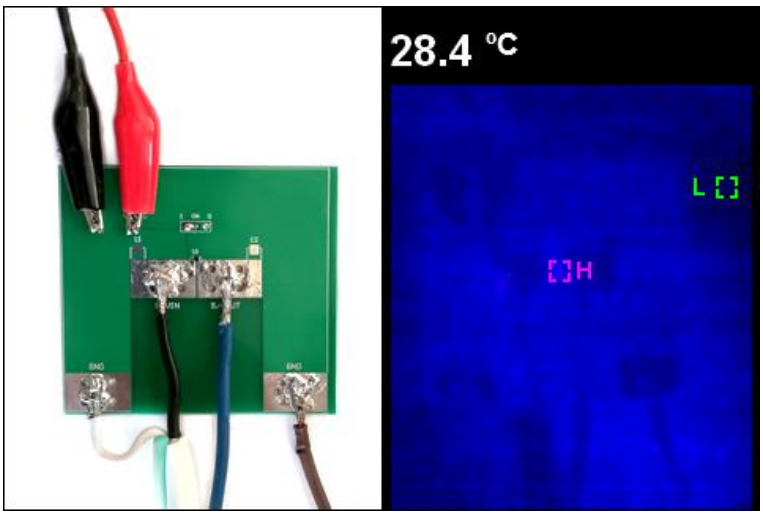
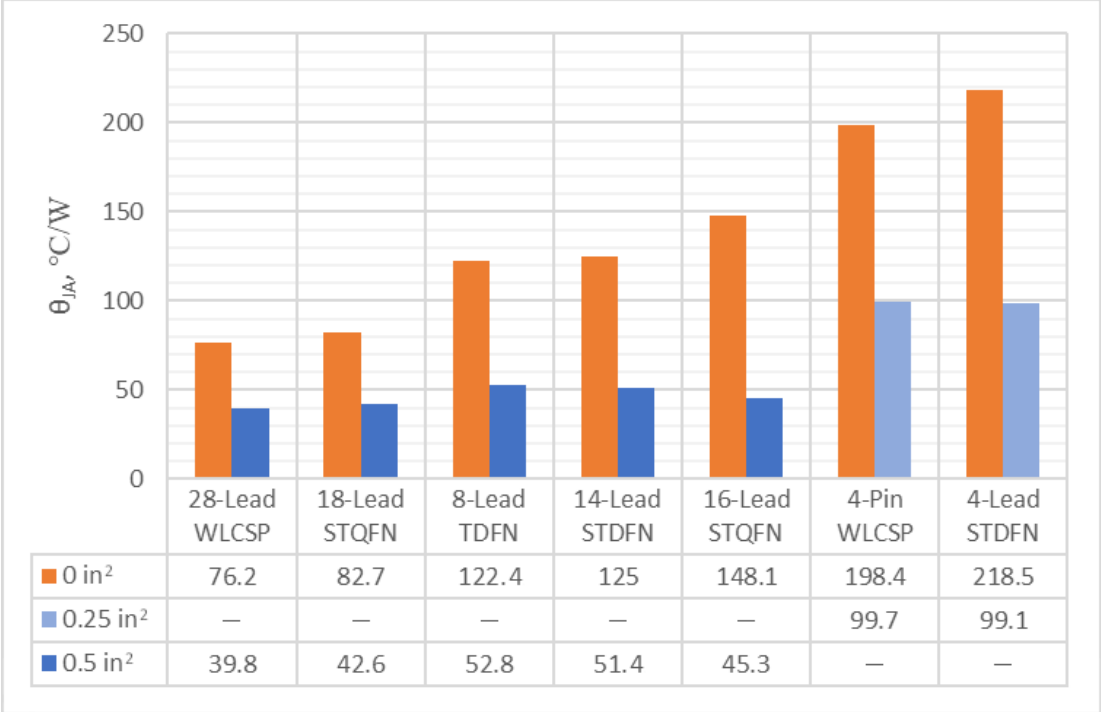


Figure 32. Visible (left) and Thermal (right) Images of the SLG59M1557V in a 1 mm², 4-Lead STDFN Package Mounted on a Type-B PCB. T_A = 25 °C, V_{IN} = 5 V, I_{LOAD} = 1 A.

A chart summarizing the results that include the comparisons of thermal resistance for different packages and copper contact areas under each input and output power pins is presented in Figure 33.



	28-Lead WLCSP	18-Lead STQFN	8-Lead TDFN	14-Lead STDFN	16-Lead STQFN	4-Pin WLCSP	4-Lead STDFN
0 in²	76.2	82.7	122.4	125	148.1	198.4	218.5
0.25 in²	—	—	—	—	—	99.7	99.1
0.5 in²	39.8	42.6	52.8	51.4	45.3	—	—

Figure 33. Thermal Resistance vs. Package Type and Polygon Area

13 Conclusions

Thermal resistance is one of the most important parameters that determines the long-term reliability of semiconductor devices. It determines what the IC (case) temperature would be under a specific load condition. Thermal resistance depends on ambient conditions (including air flow) and circuit board design. This application note shows that PCBs with larger copper contact pads underneath the power terminals are much better at dissipating heat. Increasing metal contact areas at the terminals decreases the package/PCB thermal resistance. This maintains device reliability and longevity due to reduced IC junction temperature. A good practice to minimize PCB area is to divide metallization among different PCB layers. Thus, in 2-layer PCB to obtain 0.5 in^2 area under VIN and VOUT pins, it is possible to need only 0.25 in^2 on top and bottom layers connected by vias. The thermal result will be approximately the same, and the total PCB area will be smaller.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.