Application Note

Analog Front End for Heart Rate Monitor

AN-CM-307

Abstract

This application note describes the design procedure of an analog front end for a heart rate monitor. The circuit utilizes a commonly used technique of measuring the green light reflected from skin. A unique Auto-Trim feature of the SLG47004 allows achieving stable circuit operation in various conditions. The application note also contains test results of a hardware prototype.

This application note comes complete with design files which can be found in the References section

Contents

Figures

1 Terms and Definitions

AFE	Analog front end
ECG	Electrocardiogram
HR	Heart rate
IC	Integrated circuit
OpAmp	Operational amplifier
S&H	Sample and hold
TIA	Transimpedance amplifier

2 References

For related documents and software, please visit:

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Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the AnalogPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-307 Analog Front End for Heart Rate Monitor.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG47004, Datasheet

Author: Vladyslav Kozlov

3 Introduction

Heart rate is one of the critical vital signs in humans. The monitoring and tracking of heart rate (HR) is a relatively simple task for modern electronics. That's why modern wearable devices like smartwatches and activity trackers widely utilize a HR monitoring function. In addition, such devices can detect possible diseases like tachycardia (fast HR), bradycardia (slow HR), arrhythmia (often changed HR), and others.

Also, HR monitors are widely used in sports. With the help of an HR measurement, athletes can define appropriate load and rest intervals.

4 Heart Rate Monitoring Techniques

There are several different techniques of how heart rate can be monitored. All these techniques use different types of signals.

4.1 Phonocardiography

This technique uses the sound signal produced by opening and closing of heart valves. As a rule, the signal is filtered and processed with the help of DSP. After proper filtering, it's possible to detect not only heart rate, but also abnormalities of the heart.

4.2 Pressure Sensing Technique

This technique utilizes a signal from a piezo sensor attached to one of the defined places on the human body, for example, on the wrist. Contraction and relaxation of the heart cause a corresponding change of pressure in the blood vessels.

4.3 Electrocardiography

This technique is based on the measurement of the electric field produced by the heart. There must be two or more electrodes placed on specific points of the human body. Graphic representation of ECG consists of six peaks and valleys called P, Q, R, S, T, and U. The heart rate is measured by averaging RR interval between two R peaks (Figure 1) over a defined period (for example, 15, 30, or 60 seconds).

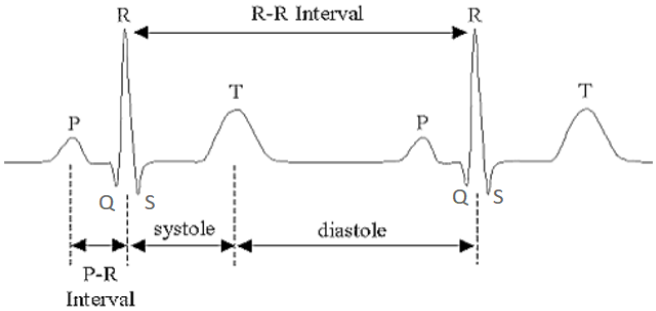

Figure 1: Typical ECG of Healthy Heart

4.4 Photoplethysmography

This technique is based on the measurement of the volume variations of light reflected from the skin. When light emitted from a LED passes through a blood vessel, the received light has pulsations that correspond to heartbeat. Typically, a green or infrared LED is used as a light source because of the characteristic of bloods' absorption to light with specific wavelengths. This technique is the most common way of heart rate monitoring in wearables.

The most appropriate wavelength of green light for photoplethysmography is in the range from 540 nm to 570 nm. But as a rule, the LEDs with 530 nm are used, due to the high value of luminous intensity.

5 Proposed Design of Analog Front End

The proposed analog front-end circuit is shown in Figure 2.

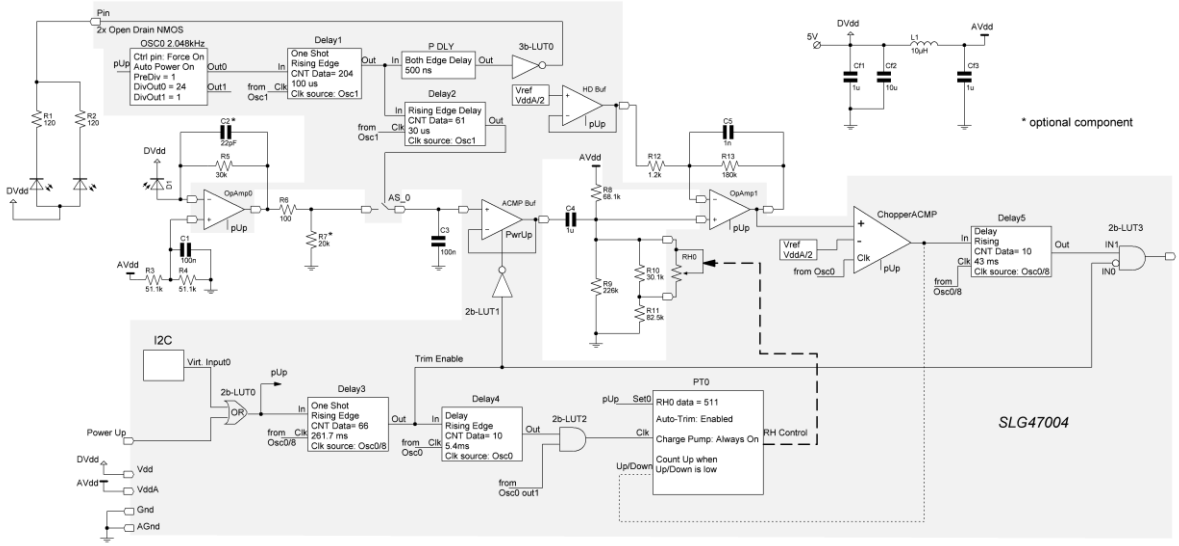

Figure 2: Analog Front-End Schematic

The circuit consists of the following parts: LED driver, transimpedance amplifier (TIA), sample and hold circuit, high pass filter, offset correction circuit, biased non-inverting amplifier, analog comparator with digital filter, and analog power supply filter. The structure of the proposed design is shown in Figure 3.

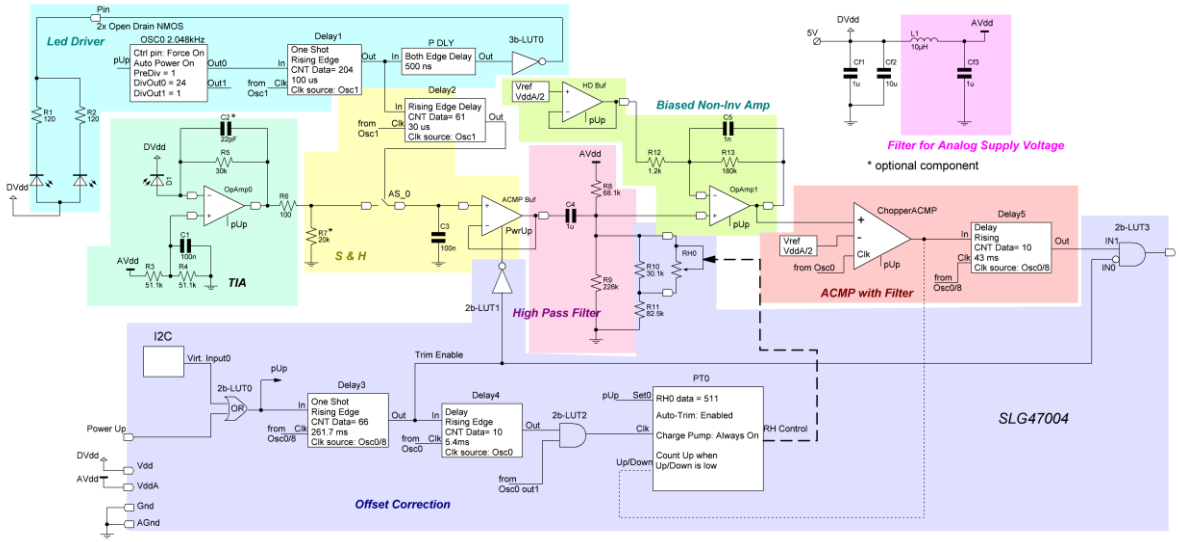

Figure 3: Analog Front End Structure

5.1.1 LED Driver

The LED driver periodically turns on/off two green LEDs. The period is 11.7 ms (85.3 Hz). Turn on time duration is 100 us. So, the duty cycle is 0.1/11.7 = 0.85 %. The operating current through each LED is 12.5 mA, giving 25 mA through one pin of the SLG47004. The average current through the pin is 213 µA.

5.1.2 Transimpedance Amplifier

In this example the TIA operates in photovoltaic mode to convert small photodiode current to voltage. The photodiode part number is BPW34. It's possible to use other LEDs or photodiode, but in that case gain resistor R5 must be changed to provide an appropriate voltage level at the output.

Optional capacitor C2 increases the stability of the TIA. It's recommended to place C2 in case of stability issues of the TIA stage. The value of C2 can be calculated using the following formula:

$$C_f = \sqrt{\frac{(C_D + C_{CM} + C_{Diff})}{2\pi \cdot GBWP \cdot R_f}}$$

where C_D, C_{CM}, C_{Diff} - are diode capacitance, common-mode operational amplifier capacitance, and differential mode operational amplifier capacitance;

GBWP - is gain-bandwidth product of operational amplifier;

R_f - is the feedback resistor.

According to the datasheet, amplifiers of the SLG47004 have $C_{CM} = 7$ pf and $C_{Diff} = 8$ pF. Capacitance of photodiode $C_D = 40$ pF. GBWP = 512 kHz (setting) and Rf = 30 kΩ. So $C_f = 23.9$ pF or 22 pF (nearest standard value).

5.1.3 Sample and Hold Circuit

The S&H circuit consists of an analog switch, capacitor, and buffer. Sampling begins after 30 us pause when LEDs are turned on, see Figure 15. During the pause, the output of the OpAmp is stabilized. When the analog switch is opened (sampling phase), the sampling capacitor C3 is charged to the voltage level at OpAmp0 output. The duration of the sampling time is 70 us.

During the hold phase the analog switch is closed. The sampling capacitor is disconnected from OpAmp0.

The buffer (ACMP buffer) eliminates the effect of the high pass filter on the sampling capacitor.

5.1.4 High Pass Filter

The first order high pass filter has a cutoff frequency of 2.3 Hz. The DC component of the signal after that filter is $V_{DD}/2$ V.

5.1.5 Offset Correction Circuit

The correction of amplifier and buffer offset voltages is implemented by changing the resistance of one branch of the voltage divider (R9, R10, R11, and digital rheostat RH0). The configuration of the divider gives the ability to trim the system with 100 mV accuracy (worst case) of the output voltage. The divider can be simplified if high accuracy isn't required.

5.1.6 Biased Non-Inverting Amplifier

The non-inverting amplifier has a gain of 151 and a bias voltage of $V_{DD}/2$ (2.5 V for V_{DD} = 5 V).

5.1.7 Analog Comparator with Digital Filter

Digital filtering of the signal is performed by Delay5, configured as rising edge delay.

5.1.8 Analog Power Supply Filter and Grounding Considerations

A common practice for mixed-signal circuits is to provide analog supply voltage filtered from the noise generated by the digital part of the schematic. In the current project this is done with the help of an L-C filter.

Special care must be taken when routing the ground traces. Analog and digital grounds should be connected at one point. The resistance of the trace from the common ground to the power supply source should be as minimal as possible. Also, it's recommended to use a power supply source with low output impedance.

6 Internal Blocks Configuration

6.1 OpAmp0 and OpAmp1 Configurations

OpAmp configurations are shown in Figure 4.

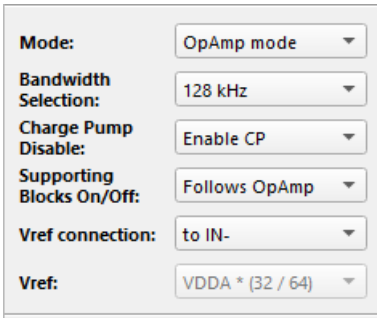

Figure 4: Operational Amplifier 0, 1 Settings

6.2 Chopper ACMP Configuration

Chopper ACMP configuration is shown in Figure 5.

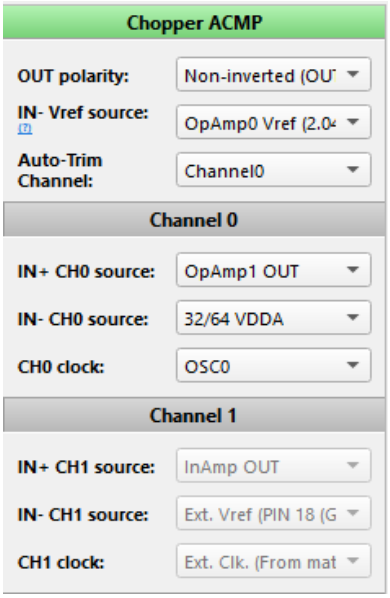

Figure 5: Chopper ACMP Settings

6.3 HD Buffer Configuration

HD Buffer shares the internal voltage reference with OpAmp0 macrocell. Note that in the current project internal Vref is disconnected from the OpAmp0. The power-up source for HD Buffer is the connection matrix signal. The HD Buffer and OpAmp0 Vref configurations are shown in Figure 6.

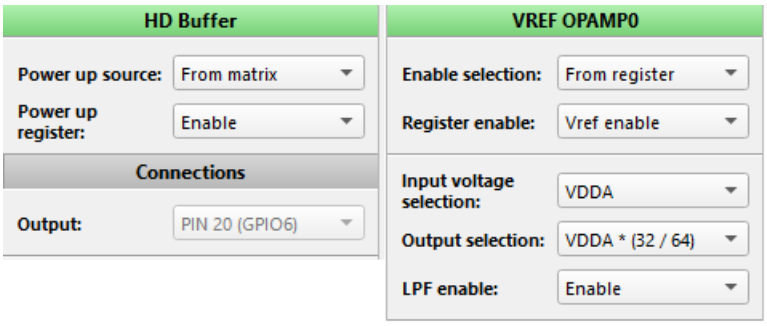

Figure 6: HD Buffer and OpAmp0 Vref Settings

6.4 ACMP Buffer Configuration

To use ACMP buffer as a voltage follower, the ACMP1 and Vref1 macrocells should be configured as shown in Figure 7:

Figure 7: ACMP1L and Vref1 Settings

6.5 Oscillators Configurations

Oscillator1 uses default settings. Oscillator0 configuration is shown in Figure 8.

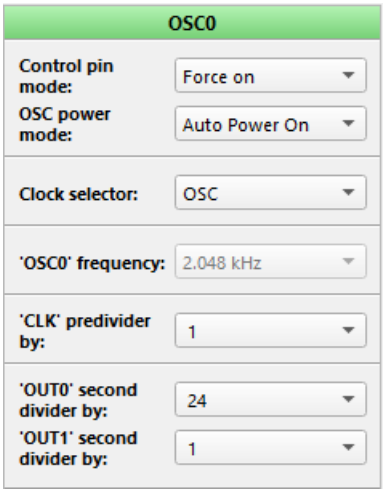

Figure 8: Oscillator0 Settings

6.6 Delay Macrocells Configurations

Delay configurations are shown in Figure 9.

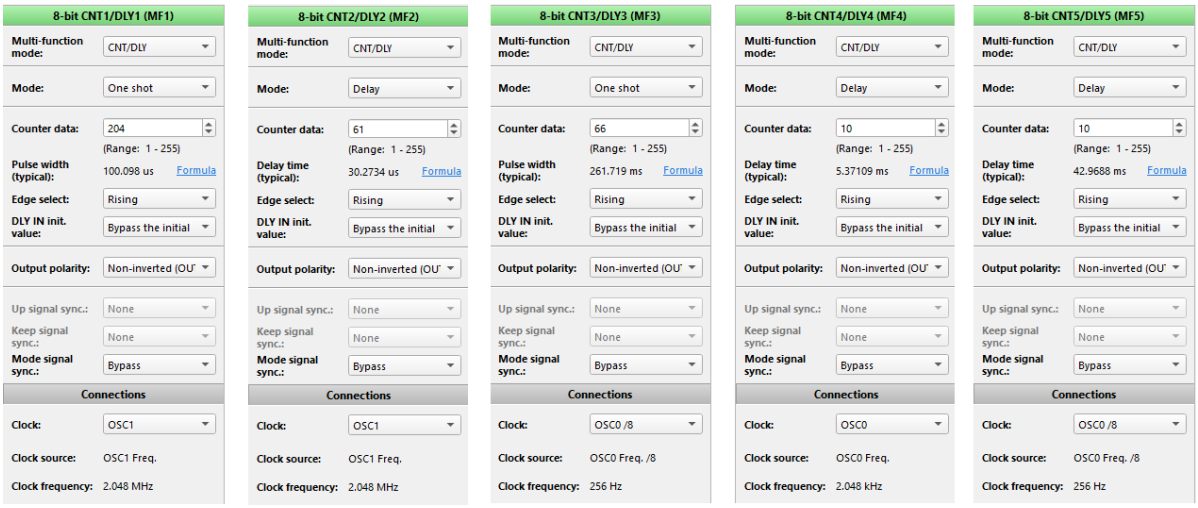

Figure 9: Delay Macrocells Settings

6.7 P DLY Configuration

P DLY configuration is shown in Figure 10.

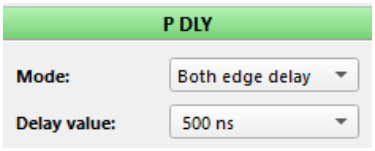

Figure 10: P DLY Settings

6.8 LUTs Configurations

LUTs configurations are shown in Figure 11.

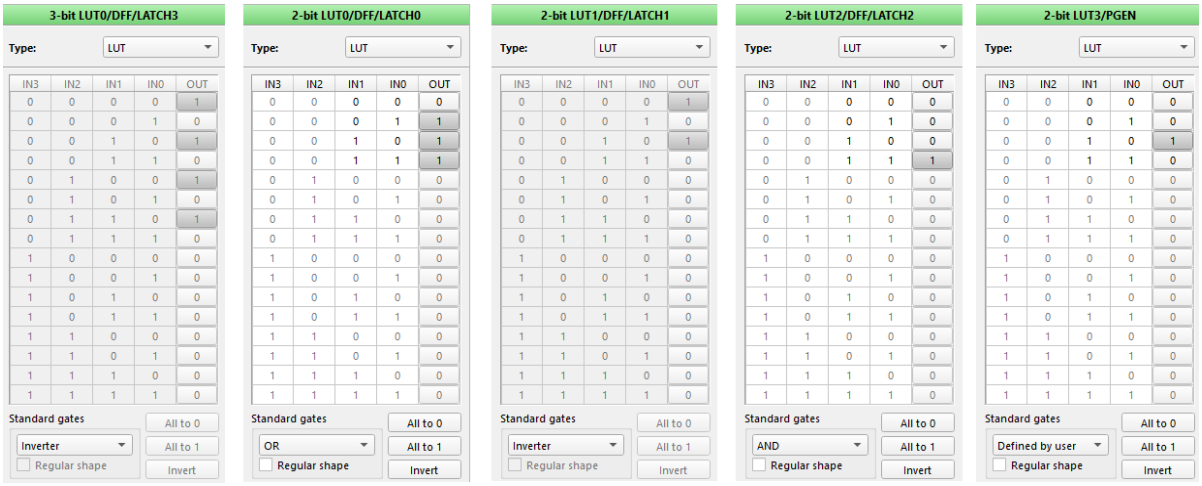

Figure 11: LUTs Settings

6.9 Digital Rheostat 0 Configuration

Digital Rheostat 0 configuration is shown in Figure 12.

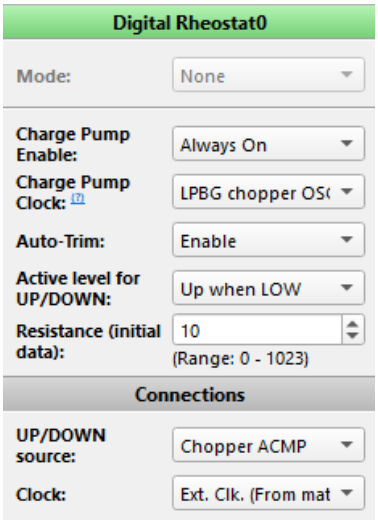

Figure 12: Digital Rheostat 0 Settings

6.10 Analog Switch 1 Configuration

Analog Switch 1 configuration is shown in Figure 13.

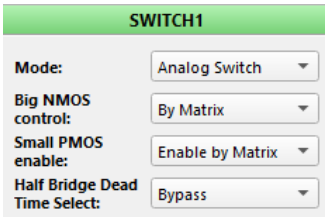

Figure 13: Analog Switch 1 Settings

6.11 I²C Macrocell Configuration

I²C macrocell uses default configurations.

6.12 GPIOs Configurations

GPIOs configurations are shown in Figure 14.

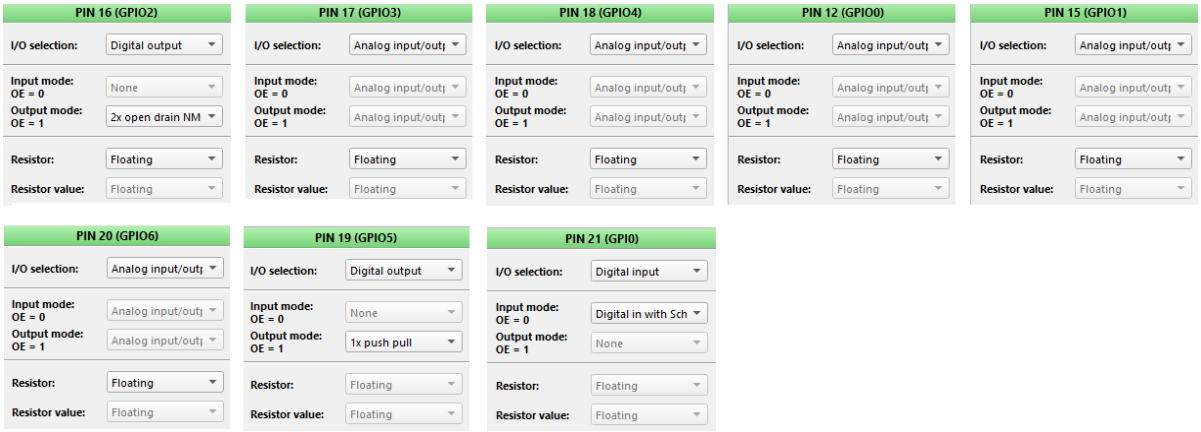

Figure 14: GPIOs Settings

7 Normal Operation Mode

The analog front-end starts operating either when the voltage at power-up input (GPI0) becomes high level or when I²C master sets I²C Virtual Input0 to 1.

The Auto-Trim process begins every time after a short delay (Delay4 time = 5.4 ms) when power-up input (I²C Virt. Input0) becomes high. The maximum duration of the Auto-Trim process is 512(rheostat_code)/2048(kHz_clock) = 250 ms.

During the calibration procedure the analog switch is turned off and the resistance of the high pass filter divider is being changed until the voltage at the inverting input of Chopper ACMP (Vref=AV_{DD}/2) isn't equal to the voltage at the non-inverting input of Chopper ACMP (OpAmp1 output).

After the Auto-Trim process is done AFE begins to sense heart rate. LEDs are turned on 85 times per second during short intervals (100 us). The sample and hold circuit takes samples when LEDs are turned on after a pause of 30 us, see Figure 15. The sample and hold principle greatly minimizes the average current consumed by the LEDs.

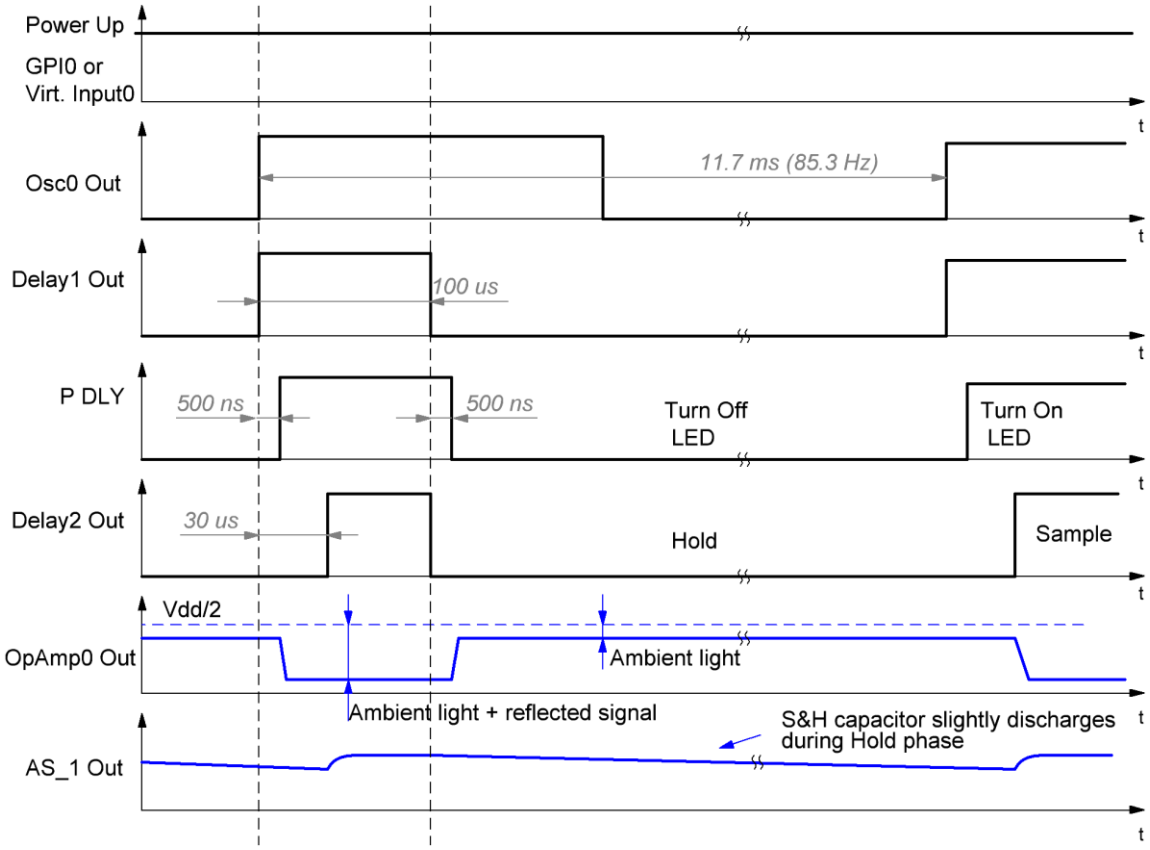

Figure 15: Sample and Hold Phases During Normal Operation Mode

8 Software Simulation and Hardware Prototype Testing

Figure 16 and Figure 17 show the simulation results of the first four seconds of AFE operation. The sensor (photodiode) is modeled as a sine voltage source with 10 mV amplitude. As shown in Figure 17, the desired point of trim (V_{DD}/2) is reached 114 ms after start of the Auto-Trim process. Then the Auto-Trim system continues to operate and to switch the rheostat near the desired trim point until internal Set signal is released.

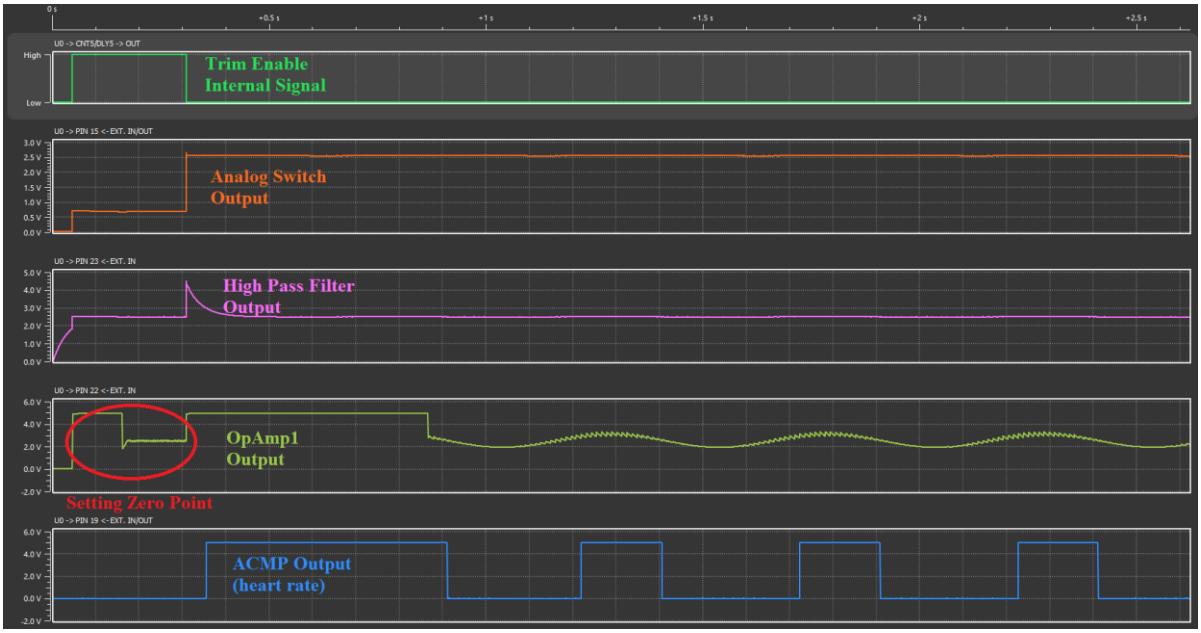

Figure 16: Simulation Results of the First Four Seconds of Operation

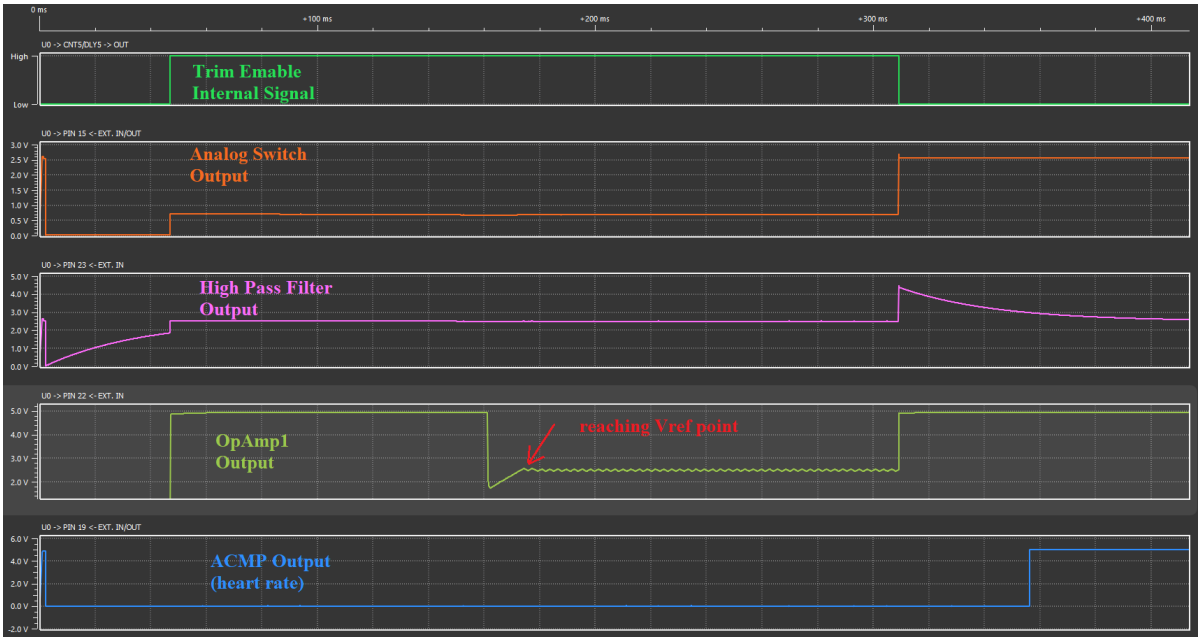

Figure 17: Simulation Results of the Auto-Trim Process

The waveforms of the hardware prototype testing are shown in Figure 18.

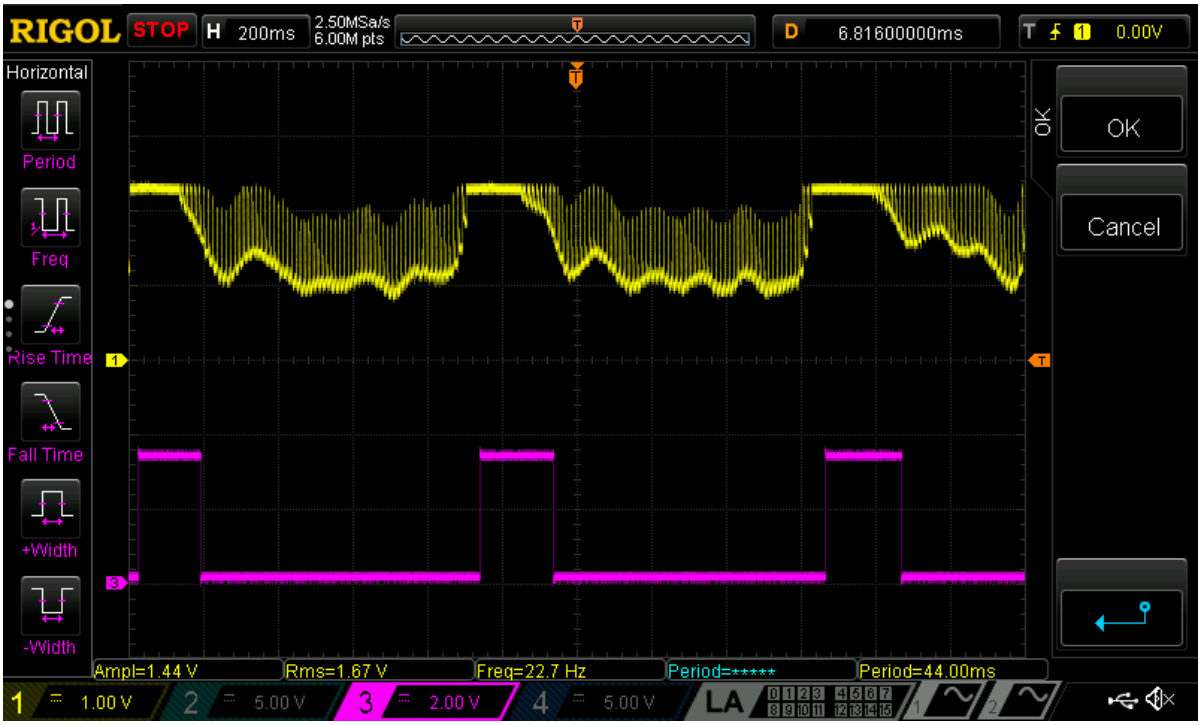

Figure 18: Analog (Yellow) and Digital (Pink) Output Signals of AFE Applied to Finger

The frequency of pulses at the digital output (Figure 18) is f_{output} = 1.063 Hz. This frequency corresponds to the heart rate of (f_{output}*60) = 64 beats per minute.

The short voltage spikes on the analog output signal are caused by the LED's turn on/off. These spikes don't affect digital output signal since they are filtered by digital filter inside the SLG47004. If needed, these spikes can be also filtered by 1st order RC low pass filter placed at the OpAmp1 output.

The saturation region of the analog output signal is caused by the HD Buffer. This buffer has limited current sink capability. But this limitation of HD Buffer doesn't affect the digital output signal.

9 Conclusions

The proposed heart rate monitor is based on measuring light reflected from skin. Both signal processing and LED control are performed by a single SLG47004 IC. Additional sample and hold circuitry allows greatly reduced current consumption.

The performance of the heart rate monitor highly depends on the optical system setup: the direction of light from LEDs, the wavelength of LEDs, the distance and angle between LEDs and photodiode, and others. Also, the measurements are affected by ambient light and small movements of the sensor.

If the heart rate signal is relatively small, like a signal from the human wrist, additional software signal processing might be required.

Revision History

Revision	Date	Description
1.0	03-Nov-2020	Initial Version

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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