# **Application Note**

# LED Strip Effects Generator Using SLG46811V AN-CM-325

## Abstract

This application note describes the design procedure of a serial data pattern generator for making visual effects with a chain of WS2812B addressable RGB LEDs, using the SLG46811V and its EPG 92-byte ROM module. This note also contains test results of the hardware prototype.

The application note comes complete with design files which can be found in the References section.



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#### LED Strip Effects Generator Using SLG46811V

## **1** Terms and Definitions

DFF	D Flip-Flop
EPG	Extended Pattern Generator
IC	Integrated Circuit
LUT	Look-Up Table
LED	Light Emitting Diode
NVM	Non-Volatile Memory
RGB	Red Green Blue
Vcc	Voltage common collector, power supply pin

## 2 References

For related documents and software, please visit:

#### https://www.dialog-semiconductor.com/products/greenpak

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

- [1] GreenPAK Designer Software, Software Download and User Guide
- [2] AN-CM-325 LED Strip Effects Generator Using SLG46811V.gp, GreenPAK Design File
- [3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
- [4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
- [5] SLG46811, Datasheet
- [6] GreenPAK Cookbook

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## 3 Introduction

The WS2812B is a popular intelligent RGB LED with a driver and a proprietary digital serial protocol for control. It is widely used to make LED strips for visual decorative effects or even to make simple LED screens. In this application note, we will introduce a basic design using the SLG46811 that will make a visual effect of running colors along the LED strip. 64 LEDs are soldered in a chain (an 8x8 matrix is used).

## 4 Address LED Controlling Techniques

There are several different techniques for controlling WS2812 LED strips. Different types of MCUs are used to implement these techniques. We are introducing a new way to program an LED strip using a configurable logic IC with NVM memory, the SLG46811 IC.

#### 4.1 Hardware Protocol

The WS2812B is a 5050-component package with a control circuit, drivers, and RGB LED. It also has signal reshaping and amplification circuit. Data is sent in a serial manner using a single pin from transmitter to receiver. Each LED is the transmitter of a signal received from the previous LED.

For programing LEDs, a serial bitstream of logical 0s and 1s should be transformed into pulse width modulated voltage levels (see Figure 1). The LEDs have a built-in signal form reshaping circuit, as they transmit a data sequence from the previous LED to the next one. After wave reshaping, they send all data to the next driver, ensuring waveform distortion will not accumulate. The timings are described in Figure 2.

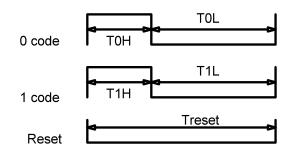


Figure 1. PWM LED protocol

Data transfer time (TH+TL=1.25us+-600ns)

тон	0 code, high voltage time	0.35 us	+-150ns
T1H	1 code, high voltage time	0.7us	+-150ns
TOL	0 code, low voltage time	0.8us	+-150ns
T1L	1 code, low voltage time	0.6us	+-150ns
Reset	Low voltage time	Above 50us	

#### Figure 2. Time Diagram of 0 and 1 Coded Signals

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#### 4.2 Details of Color Forming

Each pixel of the three primary colors can have 256 brightness steps, completing a 16,777,216 color display with a scan frequency no less than 400 Hz.

#### 4.3 Software Protocol

The RGB color code has 3 bytes received one after another, each byte coding 256 digits of the brightness of each LED. First the green byte is sent, then the red, then the blue (see Figure 3).

G	G	G	G	G	G	G	G	R	R	R	R	R	R	R	R	В	В	В	В	В	В	В	В
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

#### Figure 3: LED Data Protocol

After receiving 3 RGB bytes, the LED controller repeats all the consecutive data received from an input pin to a data output pin.

When the low-level signal is held throughout the period > 50 us, all the received data is latched and displayed by the LEDs.

#### 4.4 Proposed Electrical Connection

A signal pin should never have a higher voltage than Vcc. It is recommended to connect a resistor from data out pin 6 of the SLG46811 to an LED data input pin.

It is also recommended to connect all the LED Vcc pins and the SLG46811 Vcc pin in parallel to preserve this condition. A small capacitor (100 nF) is required across each LED Vcc-GND pin (see Figure 4).

The simplified GreenPAK configuration scheme is shown in Figure 5.

The simplified GreenPAK design structure of the SLG46811 pattern generator as configured by GreenPAK Designer is shown in Figure 6.

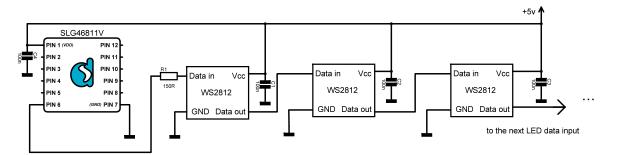


Figure 4. General Electrical Schematic



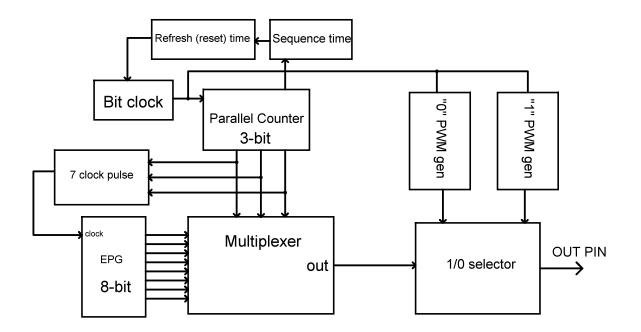


Figure 5. GreenPAK Design Structure

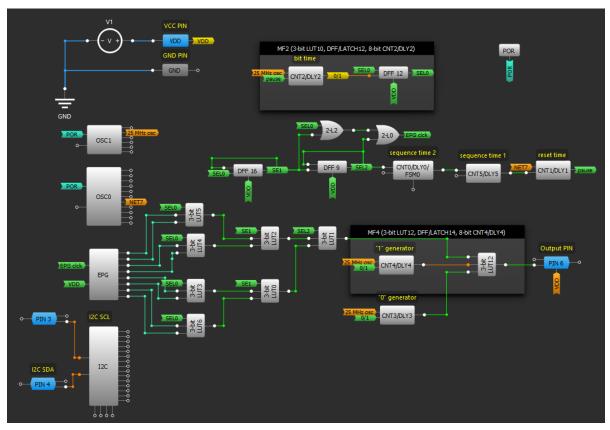


Figure 6. GreenPAK Designer Configuration

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# 5 Internal Block Configuration

The proposed pattern generator is based on the SLG46811 IC. The internal oscillators OSC0 and OSC1 are configured to output 2.048kHz/8=256Hz and 25MHz respectively (see Figure 7).

Properties		×	Properties		
	OSC0			OSC1	
Control pin mode:	Power down	•	Control pin		
Power down input:	Disable	-	mode: Power down	Force on	_
OSC power mode:	Auto Power On	-	input:	Disable	
Clock selector:	OSC	•	OSC power mode:	Force Power On	
'OSCO' frequency:	2.048 kHz	•	Clock selector:	OSC	•
'CLK' predivider by:	1	•	'OSC1' frequency:	25 MHz	,
'OUT0' second divider by:	1	•	'CLK' predivider by:	1	-
'OUT1' second divider by:	1	-	-		
Info	ormation		'OUT' second divider by:	1	1
Frequency					
Clock output confi	guration:		Start with delay:	Enable	
RC OSC Output	Value				
OUTO	OSC0 Freq.		Info	rmation	
	obcorreq.		mite	mation	
OUT1	OSCO Freq.			mation	
OUT1 CLK			Frequency		
	OSC0 Freq.		Frequency Clock output config	guration:	
СГК	OSC0 Freq. OSC0 Freq.		Frequency Clock output config RC OSC Output	guration: Value	
CLK CLK /2	OSCO Freq. OSCO Freq. OSCO Freq. /2		Frequency Clock output config	guration:	
CLK /2 CLK /4	OSC0 Freq. OSC0 Freq. OSC0 Freq. /2 OSC0 Freq. /4		Frequency Clock output config RC OSC Output	guration: Value	
CLK CLK /2 CLK /4 CLK /8	OSCO Freq. OSCO Freq. OSCO Freq. /2 OSCO Freq. /4 OSCO Freq. /8		Frequency Clock output config RC OSC Output OUT	uration: Value OSC1 Freq.	
CLK CLK /2 CLK /4 CLK /8 CLK /12	OSCO Freq. OSCO Freq. OSCO Freq. /2 OSCO Freq. /4 OSCO Freq. /8 OSCO Freq. /12		Frequency Clock output config RC OSC Output OUT CLK /4 CLK /8	Unation: Value OSC1 Freq. OSC1 Freq. /4 OSC1 Freq. /8	
CLK CLK /2 CLK /4 CLK /8 CLK /12 CLK /24	OSCO Freq. OSCO Freq. /2 OSCO Freq. /2 OSCO Freq. /4 OSCO Freq. /8 OSCO Freq. /12 OSCO Freq. /24		Frequency Clock output config RC OSC Output OUT CLK /4	Uration: Value OSC1 Freq. OSC1 Freq. /4	

Figure 7. Oscillator Settings

#### 5.1.1 "Zero and One" Code Generator

To form a PWM with a fixed high-level time, the 8-bit CNT3 and CNT4 counter blocks are configured for 280ns and 880ns high-level period time. CNT2 is used to form a total 1.24us one shot time. DFF12, DFF16, and DFF9 counts to 8 bits forming a byte impulse. CNT0 and CNT5 together count up to 279 bytes, which fills all the LEDs with information bits from the EPG plus an extra 3 bytes to create a shift effect. For example, 92 bytes from the EPG are sent three times in a row (92\*3=279 bytes) including 3 bytes extra to make the shift effect. Each LED takes 3 bytes from a bitstream, thus 93 LEDs can be addressed. CNT1 generates a reset pause for latching all the transmitted bytes into LEDs and represents a limit of display refresh rate (which limits the visual velocity of a string movement). CNT1's 15ms delay time will result in 66 frames per second.

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#### 5.2 Multiplexing a Bitstream

The 3-bit LUT0-LUT6 form a multiplexer, which transforms a byte from the EPG to serial bits for output.

All multiplexer LUTs have the same configuration setting shown in Figure 8.

Properties (§										
3-bit LUT0/DFF/LATCH2										
Type:										
IN3	IN2	IN1	IN0	OUT						
0	0	0	0	0						
0	0	0	1	1						
0	0	1	0	0						
0	0	1	1	1						
0	1	0	0	0						
0	1	0	1	0						
0	1	1	0	1						
0	1	1	1	1						
1	0	0	0	0						
1	0	0	1	0						
1	0	1	0	0						
1	0	1	1	0						
1	1	0	0	0						
1	1	0	1	0						
1	1	1	0	0						
1	1	1	1	0						
Standard	d gates		AI	l to 0						
Define	ed by use	er 🔻	AI	l to 1						
Reg	gular sha	ipe	I	wert						
0	5	9	App	ly						

Figure 8. Multiplexer Settings for 3-bit LUT0-LUT6

DFF9, DFF16, and DFF12 form a 3-bit parallel counter, which addresses the multiplexer. The address is reset every byte pulse through reset inputs. The DFFs are all configured as a D flip-flop with inverted output, as shown in Figure 9.

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Properties			×	Properties			×	Properties			×
	DFF/LAT	CH12 (MF2	)	4-	bit LUT(	)/DFF/LATCH	116	3-bit LU	r7/dff/l	ATCH9/Shif	t Regist
Mode:		DFF	•	Type:		DFF / LATCH	-	Type:		DFF / LATCH	
nSET/nRESET			Mode:		DFF	•	Mode:		DFF	•	
Initial High			Second Q	select:	Q of first DF	F 🔻	nSET/nRE option:	SET	nRESET	•	
polarity: Q output				nSET/nRE option:	SET	nRESET 💌		Initial polarity:		High   High  Low level  High	
polarity:		Inverted (no	-1	Initial pol	arity:	High	•	Q output polarity: Active level for RST/SET:			
	Info	rmation		Q output polarity:		Inverted (no	<b>ک</b> م				
Normal op	eration			Active lev RST/SET:	el for	Low level	-		Info	ormation	
D	CLK	Q(t)	nQ(t)		Infe	ormation		Normal operation			
0	t	0	1	Normal operation			D	СЦК	Q(t)	nO(t)	
0	Ļ	t - 1	t-1	D	СЦК	Q(t)	nQ(t)	0	t	0	1
1	t	1	0	0	t	0	1	0		t-1	t-1
· · ·		· ·		0	Ļ	t - 1	t - 1	1	t	1	0
1	4	t - 1	t - 1	1	t	1	0	1		t-1	t-1
t - 1 - previ nRESET = (				1	4	t - 1	t - 1	t - 1 - prev	•		1-1
		ng = 1; nal operatio	n:	t - 1 - prev		e; 0; nQ = 1;				e; 0; nQ = 1;	
nSET = 0 =			.,	nRESET =	1 => nor	mal operation	n;			mal operatio	n;
nSET = 1 =	$nSET = 0 \Rightarrow Q = 1; nQ = 0;$ $nSET = 1 \Rightarrow normal operation;$			nSET = 0 => Q = 1; nQ = 0; nSET = 1 => normal operation;							
Apply									pply		

Figure 9. DFF Configuration

Propertie	s			×							
3-bit LUT12 (MF4)											
IN3	IN2	IN1	IN0	OUT							
0	0	0	0	0							
0	0	0	1	1							
0	0	1	0	0							
0	0	1	1	1							
0	1	0	0	0							
0	1	0	1	0							
0	1	1	0	1							
0	1	1	1	1							
1	0	0	0	0							
1	0	0	1	0							
1	0	1	0	0							
1	0	1	1	0							
1	1	0	0	0							
1	1	0	1	0							
1	1	1	0	0							
1	1	1	1	0							
Standar	d gates		AI	l to 0							
Defin	ed by us	er 🔻	A	I to 1							
Re	gular sha	ape	In	wert							
	5	Ð	Арр	ly							

Figure 10. 3-bit LUT12 Configuration

The 3-bit LUT12 selects which 0 or 1 PWM pulse to pass through to the output pin 6. The design has DFF15 configured to work as an edge detector. The configuration is shown in Figure 10.

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#### 5.2.1 EPG Configuration

The extended pattern generator (EPG) is configured for an overflow action: after all 92 bytes are clocked out, the generator is reset to the byte 0 (see Figure 11). In this design we are addressing 61 LEDs, so we are clocking the EPG two times in a row. It would be ideal to address 92 LEDs to clock the EPG 3 times. In this case, CNT0 should be configured for 276 clocks (3\*92) plus 3 bytes for a shift (running string effect), thus reaching 279 in total. Entering the sequence into the EPG, users should keep in mind that 90 bytes from the generator would address 30 LEDs and the 91-92 bytes will go to the 31st LED only for green and red color bytes. The next "overflowed" first byte from the EPG will go to the blue byte of the 31st LED. So the 31st LED will have a shift of 1 byte compared to the first run of the EPG. We have to program a sequence into the EPG to make a color shift.

#### The programmed EPG bytes are:

 $(0,0,\overline{8},0,\overline{0},16,0,0,24,0,0,\overline{3}2,0,0,40,0,0,48,0,0,56,0,0,64,0,0,72,0,0,80,0,0,88,0,0,96,0,0,104,0,0,112,0,0,128,0,0,136,0,0,142,0,0,150,0,0,158,0,0,164,0,0,172,0,0,180,0,0,188,0,0,196,0,0,204,0,0,212,0,0,220,0,0,228,0,0,236,0,0)$ 

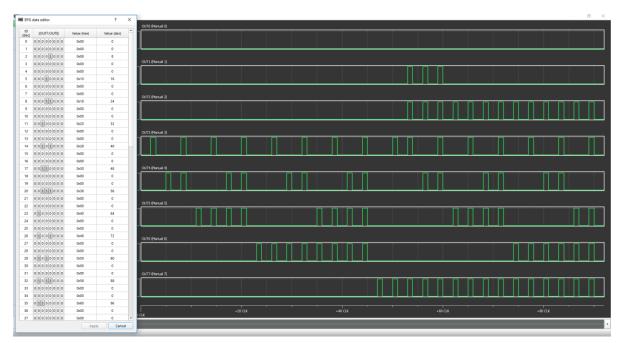


Figure 11. EPG Configuration

# 6 Tuning

#### 6.1 Address LED Data Timings

There are many different modifications and manufacturers' standards of the WS2812B LED that can differ in data timings. The best way to figure out what period of 0s and 1s you should use is to set up the SLG46811 IC in emulation mode with typical settings, connect the LED chain, and measure timings retranslated from the next LED using an oscilloscope. Use those measurements to set up the CNT3, CNT4, and CNT2 counters as zero bit width time, one bit time, and bit period respectively.

## 6.2 LED Count Tuning

If you want to have a greater number of LEDs than 93, you have to add 3 to the counter value of CNT0 (2 is for 93 LEDs, 5 will give you 186 LEDs, 8 will give you 279 LEDs, and so on).

# 7 Normal Operation Mode

After tuning the timings and programming the EPG with the desired sequence, the SLG46811 is ready for operation. Its timing diagram is shown in Figure 13.

The oscilloscope waveform is shown in Figure 14.

The working prototype series of photos is shown in Figure 15.

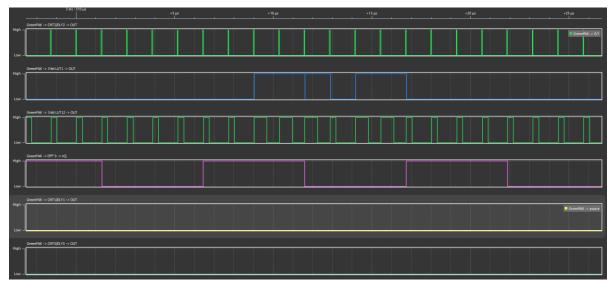


Figure 12. Software Simulated Timing Diagram 1

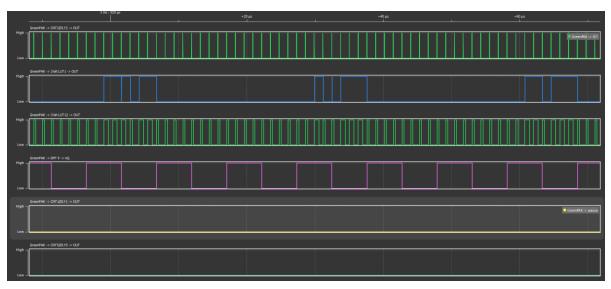


Figure 13. Software Simulated Timing Diagram 2

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Figure 14. Oscilloscope Output Pin Waveform

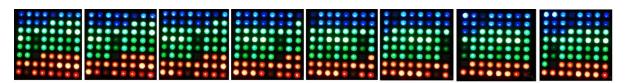


Figure 15. Working Prototype; Sequential Photos

# 8 Conclusion

The proposed pattern generator using the SLG46811 in conjunction with a chain of WS2812B LEDs can deliver a "running string" of colors for a decorative visual effect.

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# **Revision History**

Revision	Date	Description
1.0	08-Oct-2021	Initial version

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