Application Note

16-bit Sigma-Delta ADC

AN-CM-328

Abstract

This application note describes the implementation and testing of a 16-bit sigma-delta analog-to-digital converter (ADC) based on the SLG47004 IC. The design requires few internal analog and digital resources, so the ADC can be integrated with other projects inside one SLG47004.
This application note comes complete with design files which can be found in the References section.

Contents

Figures

Tables

1 Terms and Definitions

ACMP — Analog comparator
ADC — Analog-to-digital converter
DAC — Digital-to-analog converter
IC — Integrated circuit
Opamp — Operational amplifier
ΣΔ ADC — Sigma-delta ADC

2 References

For related documents and software, please visit:

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Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide
[2] AN-CM-328 16-bit Sigma-Delta ADC.gp, GreenPAK Design File
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[5] SLG47004, Datasheet

Author: Vladyslav Kozlov

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3   Introduction

The growing availability of digital ICs like microcontrollers, microprocessors, and field-programmable gate arrays (FPGAs) allows developers to use complex digital processing techniques rather than analog signal conditioning. For this reason, analog-to-digital converters (ADCs) are a widely-used component of mixed-signal circuits.

There are many types of ADCs: successive-approximation ADCs, sigma-delta (ΣΔ) ADCs, direct-conversion ADCs, capacitor charge/discharge-based ADCs, ADCs with voltage-to-frequency converters, and others. All these ADCs provide different accuracy characteristics, sampling rate limitations, and cost.

In this application note, we'll design a ΣΔ ADC.

4   Sigma-Delta ADCs

The main components of a 1st order ΣΔ ADC are:

● Integrator

● Comparator

● 1-bit digital-to-analog converter (DAC)

● Digital filter

The simplified schematic of a 1st order ΣΔ ADC is shown in Figure 1.
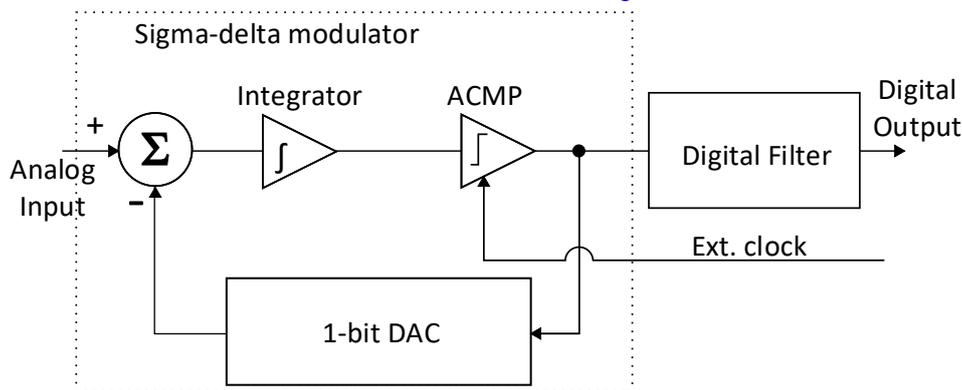
Figure 1: Basic Schematic of ΣΔ ADC.

The operating principle of a ΣΔ ADC is based on the periodic balancing of the charge of the integrator's capacitor. The integrator changes its output linearly until it crosses a threshold. When the threshold is crossed, the comparator changes the state of a 1-bit DAC to the opposite state. This forces the integrator to change its output in the opposite direction (up or down depending on the DAC output). The process then repeats. The comparator must change the DAC state synchronously using external clock pulses. See Figure 2.
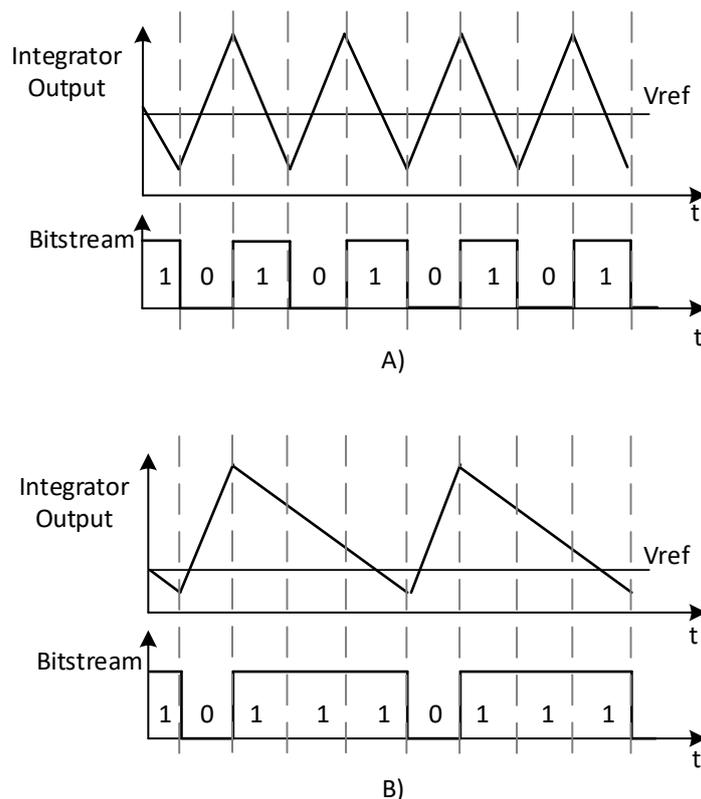
Figure 2: ΣΔ ADC Waveforms for (A) Vin= Vdd/2 and (B) and Vin=Vdd*3/4.

A ΣΔ ADC can be treated as a low-resolution ADC during one integrator period. To get a high-resolution result, the data from several periods must be averaged. This inherent oversampling and averaging allows the ΣΔ ADC to greatly minimize noise and get high-resolution data (up to 24 noise-free bits for modern ΣΔ ADCs).

The bitstream (the output of the synchronous comparator) is input to a digital filter. The typical filter is a moving average low pass sinc1, sinc3, or sinc5 filter.

5   SLG47004-Based ΣΔ ADC Structure

The simplified structure of the GreenPAK project is shown in Figure 3. An integrator based on Opamp0 adds the input signal and the signal from the 1-bit DAC. The reference voltage for the integrator and the comparator is Vdd/2. Note that the digital rheostat divider can be used instead of the internal VddA/2 reference to compensate for the offset of Opamp0 (Figure 4). The ADC reference voltage is ADC_Vref=Vdd=VddA. The 1-bit DAC is a GPIO configured as a 1x push-pull output pin. The 16-bit counter operates as an accumulator that counts the number of clock pulses wherein the ACMP output is high. The counting period for the 16-bit counter is 65536 pulses of the oscillator. A low level Power Up signal turns off Opamp0, ACMP, and the oscillator. This significantly reduces the power consumption of the SLG47004 when the ADC isn't used.

The ADC result is stored in the current counter value registers of 16-bit CNT0 (register bytes CBh, CCh). The result can be read via I2C interface.

If the Power Up input is high, the rising edge at the Start Conversion input starts the sampling procedure. The InProgress/Idle output can be monitored to define the end of the conversion. To start a new sampling procedure, the rising edge should be reapplied to the Start Conversion input. The sampling rate of the ADC is 1.95 samples per second.

16-bit Sigma-Delta ADC

The GreenPAK Designer project of the ΣΔ ADC is shown in Figure 5. The hardware prototype waveforms are shown in Figure 6.
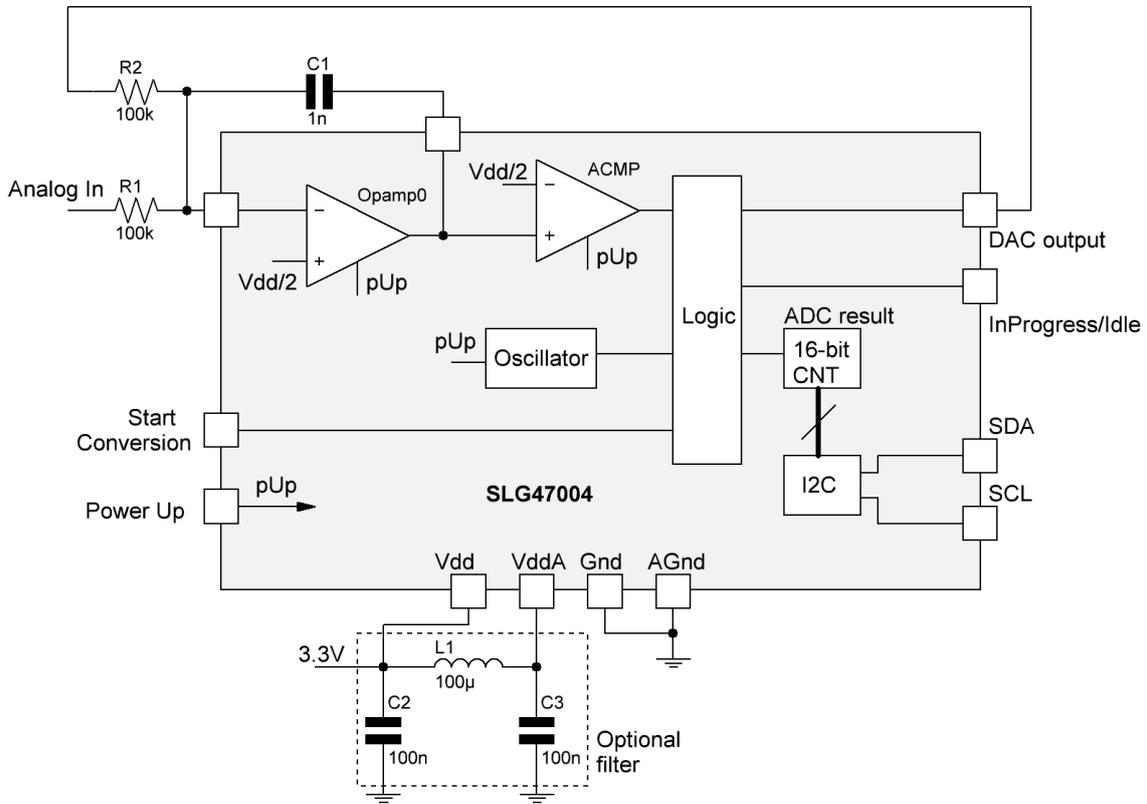
Figure 3: Simplified Structure of the ΣΔ ADC Based on the SLG47004
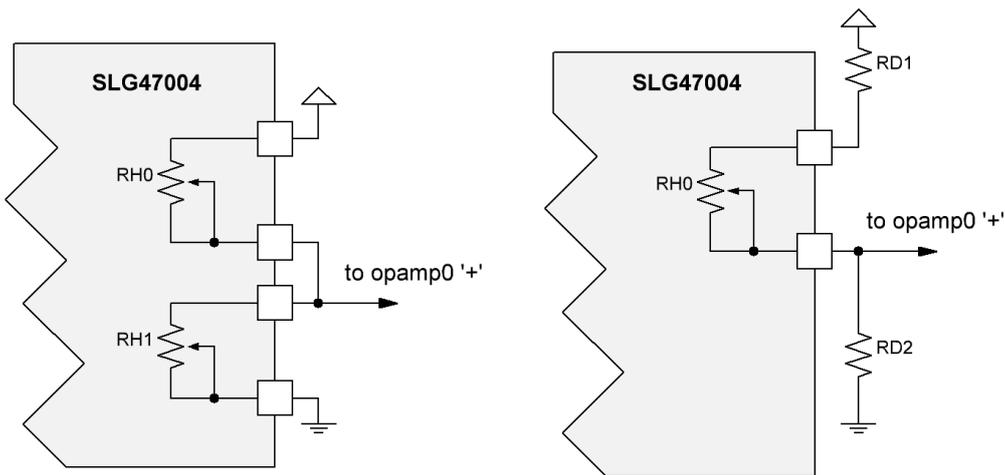
Figure 4: Optional Connection of Digital Rheostats to Adjust the Reference Voltage of Opamp0
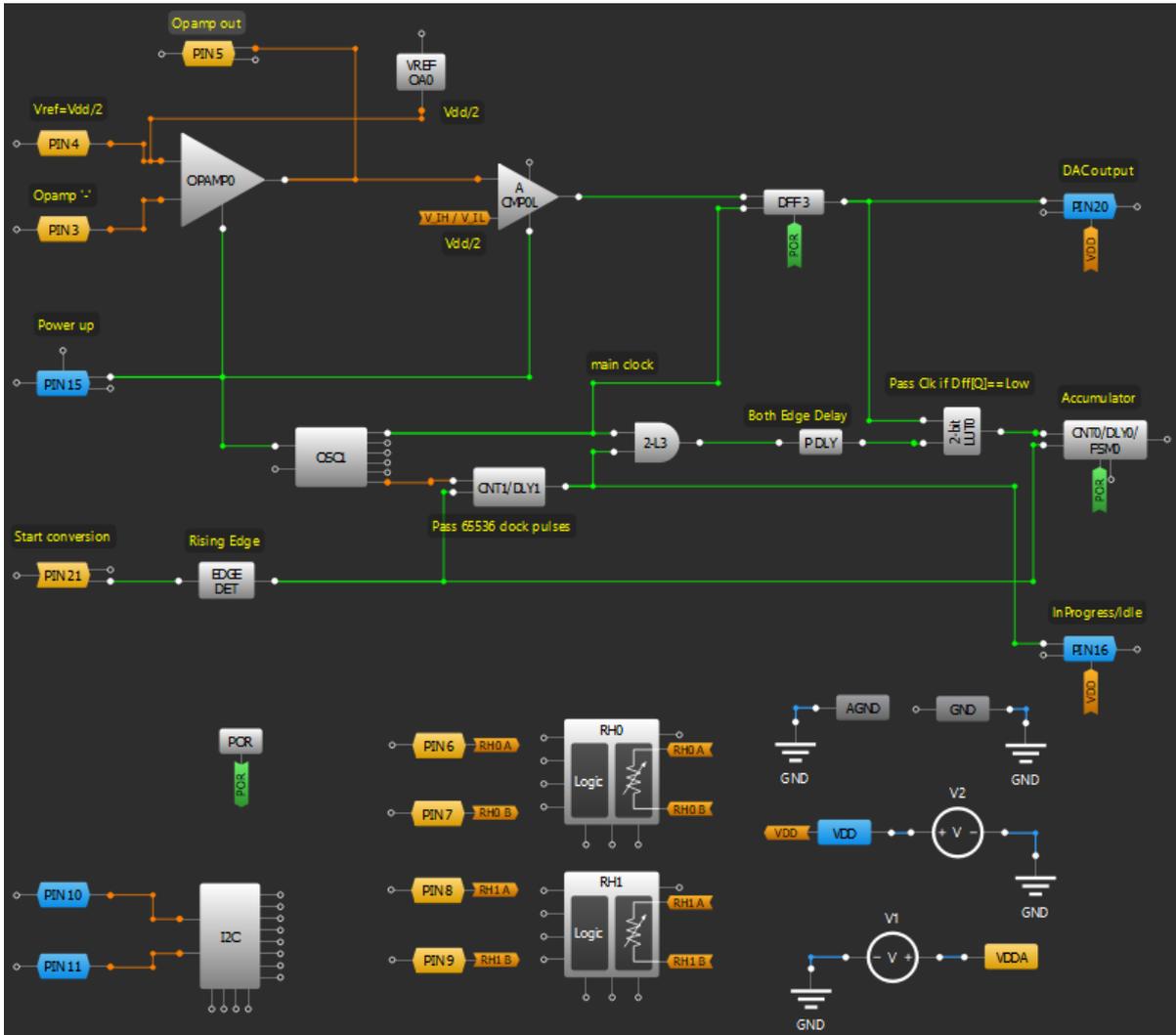
Figure 5: GreenPAK Designer Project of the ΣΔ ADC Based on the SLG47004
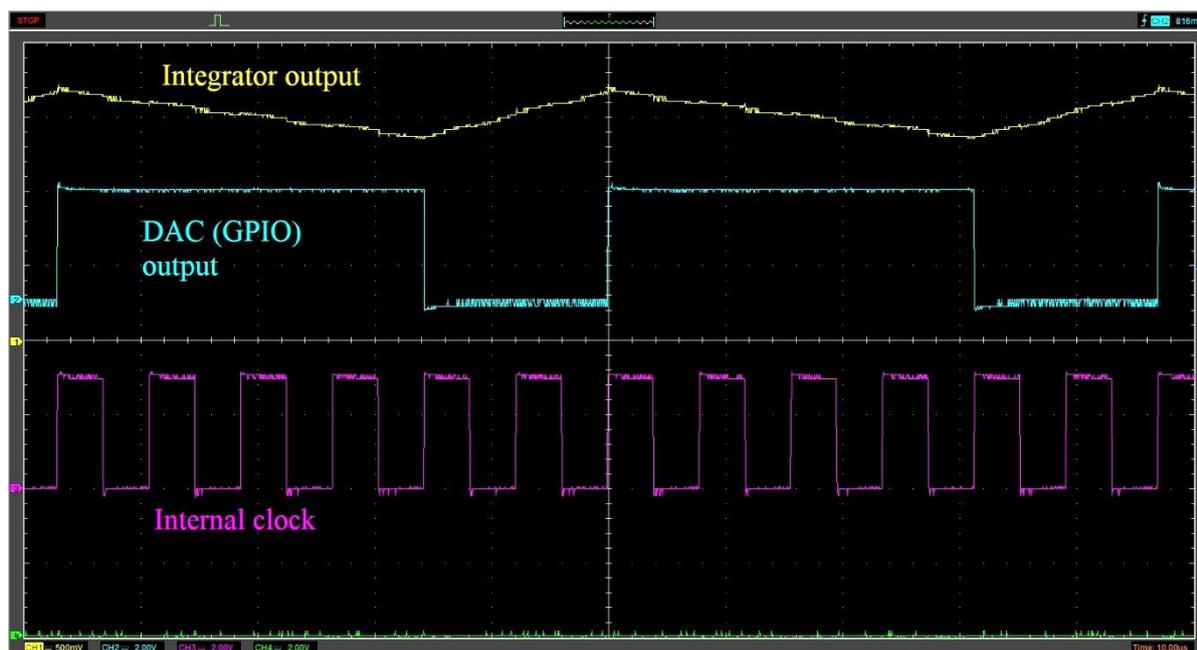
Figure 6: Hardware Prototype Waveforms for Vin=1.0V, ADC_Vref=Vdd=3.0V

6 Accuracy Characteristics

To estimate the accuracy characteristics of the ADC, an external 24-bit ΣΔ ADC was used. The external ADC was configured to operate in 16-bit mode at 1ksps, averaging 128 samples. The SLG47004 and external ADC used the same voltage reverence of 3V. For the SLG47004, Vdd=VddA=ADC_Vref. The SLG47004 uses the rheostat divider to provide reference to Opamp0. The code for both digital rheostats is 1023. Table 1, Table 2, and Figure 7 show the comparison results.

Table 1: Comparison of Results of External Etalon ADC and SLG47004-based ΣΔ ADC

#	DAC setting (Vin), mV	Etalon ADC, dec	ADC SLG47004, dec	Error between Etalon ADC data and SLG47004 data, %	Difference between Etalon ADC data and SLG47004 data, LSB
1	25	567	578	1.940%	11
2	250	5522	5533	0.199%	11
3	500	10948	10959	0.100%	11
4	750	16434	16445	0.067%	11
5	1000	21889	21898	0.041%	9
6	1250	27347	27356	0.033%	9
7	1500	32803	32811	0.024%	8
8	1750	38287	38294	0.018%	7
9	2000	43711	43720	0.021%	9
10	2250	49199	49207	0.016%	8
11	2500	54657	54663	0.011%	6
12	2700	59015	59021	0.010%	6

#	DAC setting (Vin), mV	Etalon ADC, dec	ADC SLG47004, dec	Error between Etalon ADC data and SLG47004 data, %	Difference between Etalon ADC data and SLG47004 data, LSB
13	2900	64472	64477	0.008%	5

Table 2: Linearity Assessment of the SLG47004-based ΣΔ ADC

#	ADC SLG47004 data, dec	Approximated line, LSB	ADC SLG47004 Data vs Approximated line, %	INL, LSB
1	578	578.6563	0.1134%	0.6563
2	5533	5533.1608	0.0029%	0.1608
3	10959	10958.6182	-0.0035%	-0.3818
4	16445	16444.0696	-0.0057%	-0.9304
5	21898	21898.5241	0.0024%	0.5241
6	27356	27355.9783	-0.0001%	-0.0217
7	32811	32811.4327	0.0013%	0.4327
8	38294	38294.8843	0.0023%	0.8843
9	43720	43718.3419	-0.0038%	-1.6581
10	49207	49205.7931	-0.0025%	-1.2069
11	54663	54663.2473	0.0005%	0.2473
12	59021	59020.8115	-0.0003%	-0.1885
13	64477	64477.2658	0.0004%	0.2658
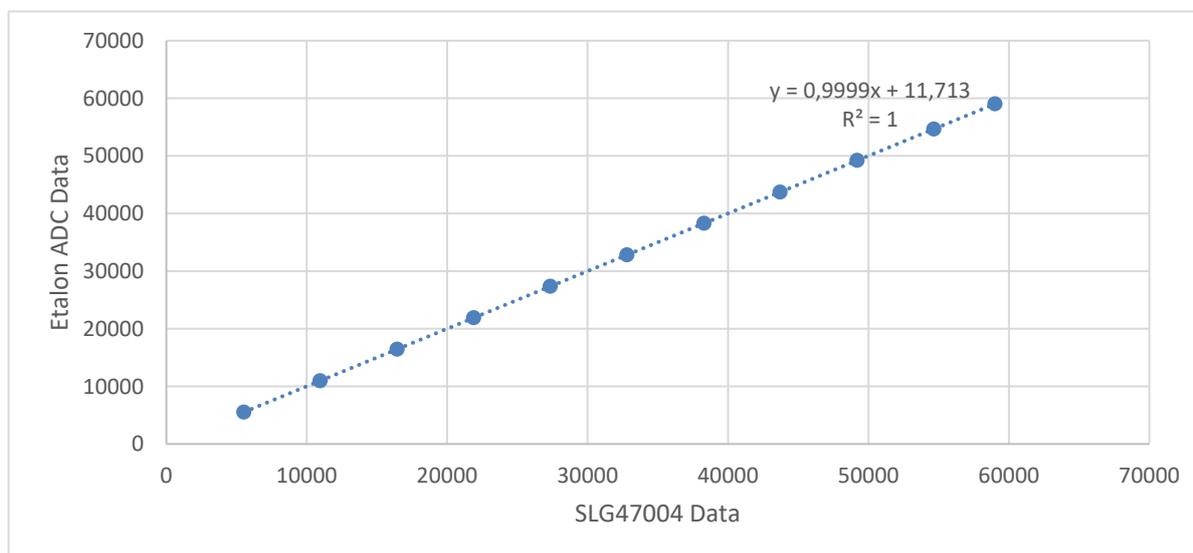
Figure 7: Comparison of Etalon ADC vs SLG47004-based ΣΔ ADC

The SLG47004-based ΣΔ ADC demonstrates good linearity (1.7 LSB max), good noise tolerance (the result deviation is 2 LSB over a sequence of samples), and small gain error (0.009% of full scale) and offset error (0.5 mV). Please note that the SLG47004-based ADC isn't calibrated, so the performance of the ADC can vary from chip to chip and can be worse than shown above. To improve the performance, the rheostat divider (Opamp0 Vref source) can be used (see Figure 4). The

calibration procedure is an adjustment of Opamp0's Vref divider output to minimize the difference between the SLG47004 data and the Etalon ADC data when the input voltage is Vin=ADC_Vref/2.

7   Conclusion

The proposed ΣΔ ADC can be used as a standalone 16-bit ADC or combined with other analog designs inside one SLG47004 IC. The internal resources needed to implement the ADC are one opamp, one ACMP, one GPIO, and a few logic components clocked by an oscillator. The proposed ΣΔ ADC has a low sampling rate (1.95sps) but good accuracy characteristics (0.5 mV offset error, 0.009% gain error, and 2 LSB max INL) and good noise immunity. The user can optionally select a higher sampling rate at the expense of accuracy.

Revision History

Revision	Date	Description
1.0	23-Nov-2021	Initial Version

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Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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