SLG5100X PMIC Power Sequencer

Content

1. References

For related documents and software, please visit:

SLG51000 - High PSRR, low noise multi-output LDO IC for advanced camera and sensor systems | Renesas

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] SLG5100X PMIC Power Sequencer.gp, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG51000 Datasheet

[6] SLG51001 Datasheet

[7] SLG51002 Datasheet

2. Introduction

The SLG51000X supply controller provides a flexible power sequencer that controls the power-up and power-down timings for the six resource enable outputs feeding the matrix interconnect.

3. Description

The timing sequence is divided into six slots, or discrete periods of time between events. There are two dedicated configurable sequences, up and down. A sequence is initiated with the trigger-up and trigger-down control signals from the matrix interconnect. The matrix interconnect provides independent power-up and power-down enable signals for each power sequencer slot, applied during power up and power down sequences respectively. It is a configurable switch that allows its output ports to be sourced from its input ports. Figure 1 represents all inputs and outputs, trigger-up and trigger-down blocks, slots and resources of matrix interconnect which can be used to control the Power sequencer in the program interface of GreenPAK designer for SLG5100X chips.

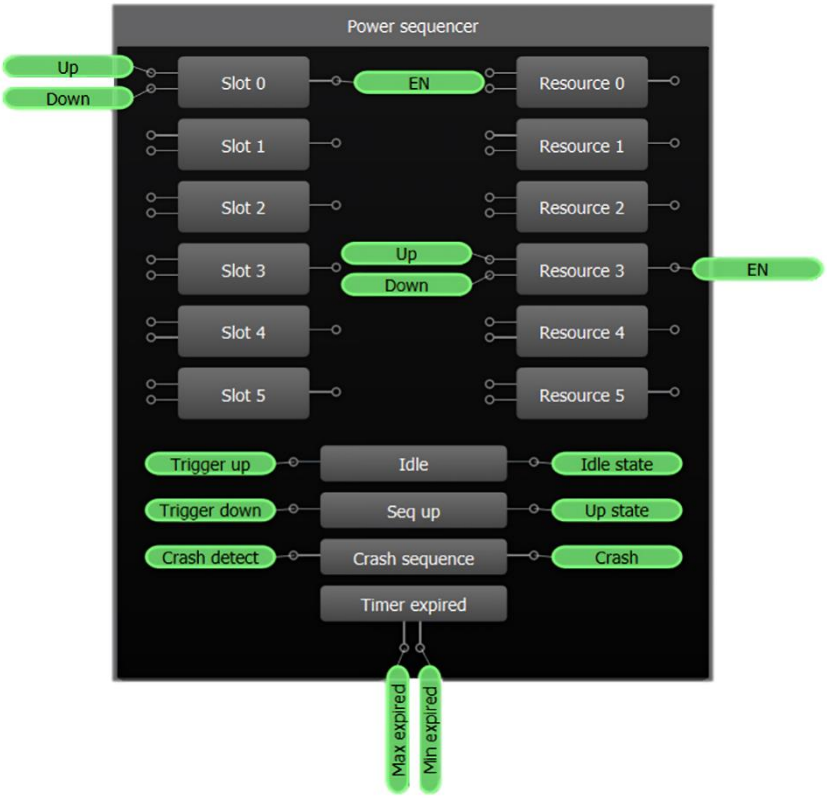


Figure 1: Power sequencer pin functions

Two dedicated configurable sequences (up and down) are initiated with the Trigger up and Trigger down (see Figure 2) control signals from the matrix interconnect. The Trigger up and Trigger down inputs are only acted upon in the Idle and Seq up states, respectively. Triggering of a power-up sequence from Idle is prevented if a Trigger down is simultaneously requested. If a Trigger down occurs during the power-up sequence (at slots 0 through 5), the sequencer will keep powering up until it reaches the Seq up state. In the Seq up state, the trigger-down signal

is then re-evaluated. In the event triggered in the Seq up state, the power sequencer crashes down to the Idle state through states PS5 to PS0. The power sequencer also provides a crash sequence which is triggered either from the main FSM error conditions or from the power sequencer's trigger-crash input from the matrix interconnect. The trigger-crash input is OTP configurable as an active-high or active-low input to the power sequencer. The crash sequence operates in the same way as a power-down sequence with the exception that only the minimum (delay) slot timer is used to control slot advancing. The power-down enable inputs from the matrix interconnect are ignored during crash sequences.

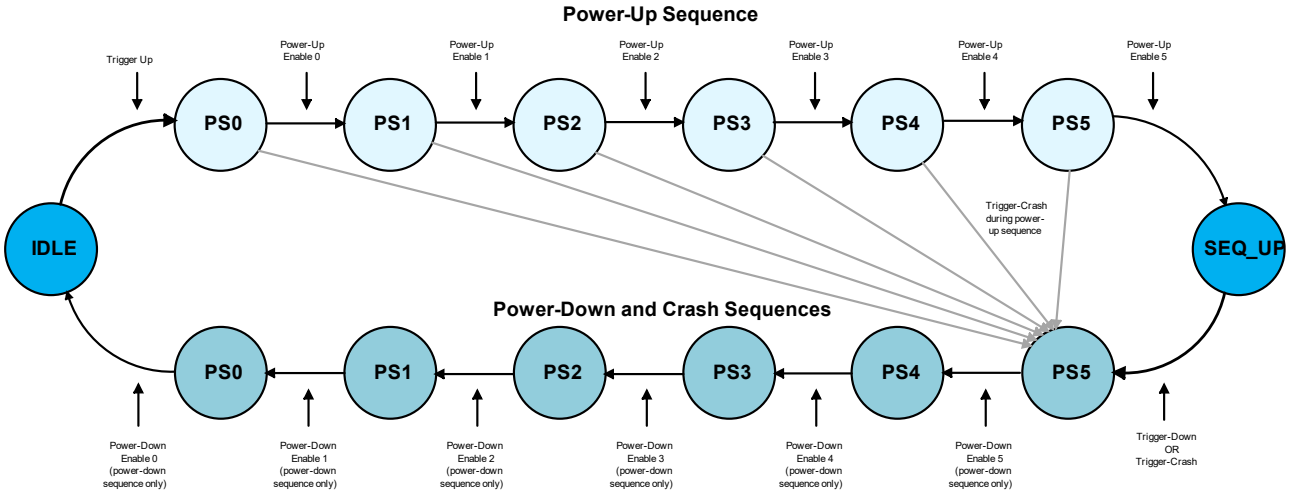
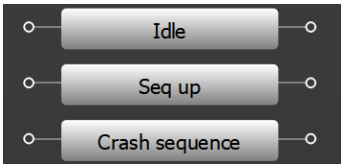
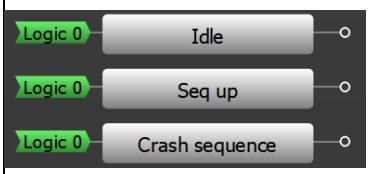
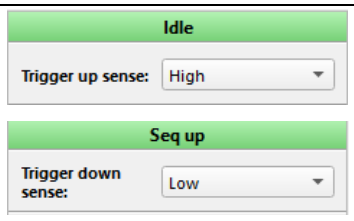


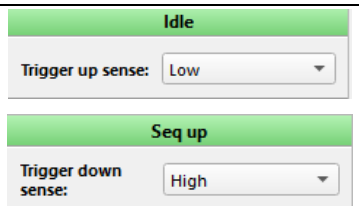
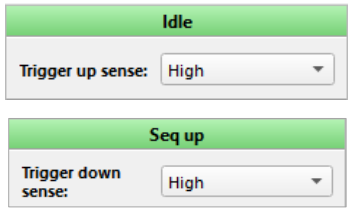
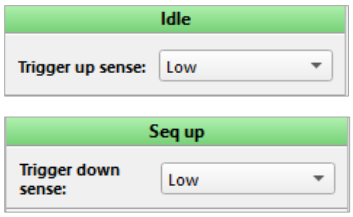
Figure 2: Power sequencer state transitions

4. Typical Power-up/down Trigger Configurations

The Power Sequencer may be triggered by Low- or High-level signals and their combinations. The table below demonstrates the Power Sequencer trigger sensitivity configuring. Flexible configurations provide possibility to use many scenarios in accordance with different requirements of source signal to trigger-up or trigger-down the Power sequencer.

Table 1: Trigger configurations

Configuration	Example	Description
With no input connections	 	In the development software for the SLG5100X, no input connections is equivalent to Logic 0.
Default		Default power-up triggered by High level from source, power-down triggered by Low.

Inverted		Inverted power-up triggered by Low level from source, power-down triggered by High.
Both high		Power-up and power-down triggered by High level from different sources.
Both low		Power-up and power-down triggered by Low level from source. Power-up starts when High is set on Seq up. It is only possible to switch state from High to Low on Seq up block for power up/down.

5. Power Sequencer in SLG5100X: Building Blocks & Timings

There are two dedicated configurable sequences, up and down. Their implementation depends on the following building blocks:

a) **Resource** output EN feeding the matrix interconnect can be independently OTP programmed to define the slot in which a transition (enable/disable) will occur within each of the power sequences.

The resources are enabled in power sequencer slot states equal to, or greater than, the programmed slot number for both power-up and power-down sequences. The resources are disabled at slot states below the programmed value.

In the Idle state, resource enable outputs to the matrix interconnect are set to 0.

For power-up slots, the resource enable signals to the matrix interconnect are set as configured at the beginning of the slot. For power-down slots, the action is processed at the end of the slot.

b) **Slot** of the power sequencer supports OTP configurable minimum and maximum duration limits that are independent for each slot in each of the power sequences.

Table 2: Selection of slot time duration limit

Enable sensitivity	Input signal	Time duration limit
High	Logic 1	Min time
High	Logic 0	Max time
Low	Logic 1	Max time
Low	Logic 0	Min time

Figure 3 shows an example applying the min time duration limit both for the power up and power down sequence.

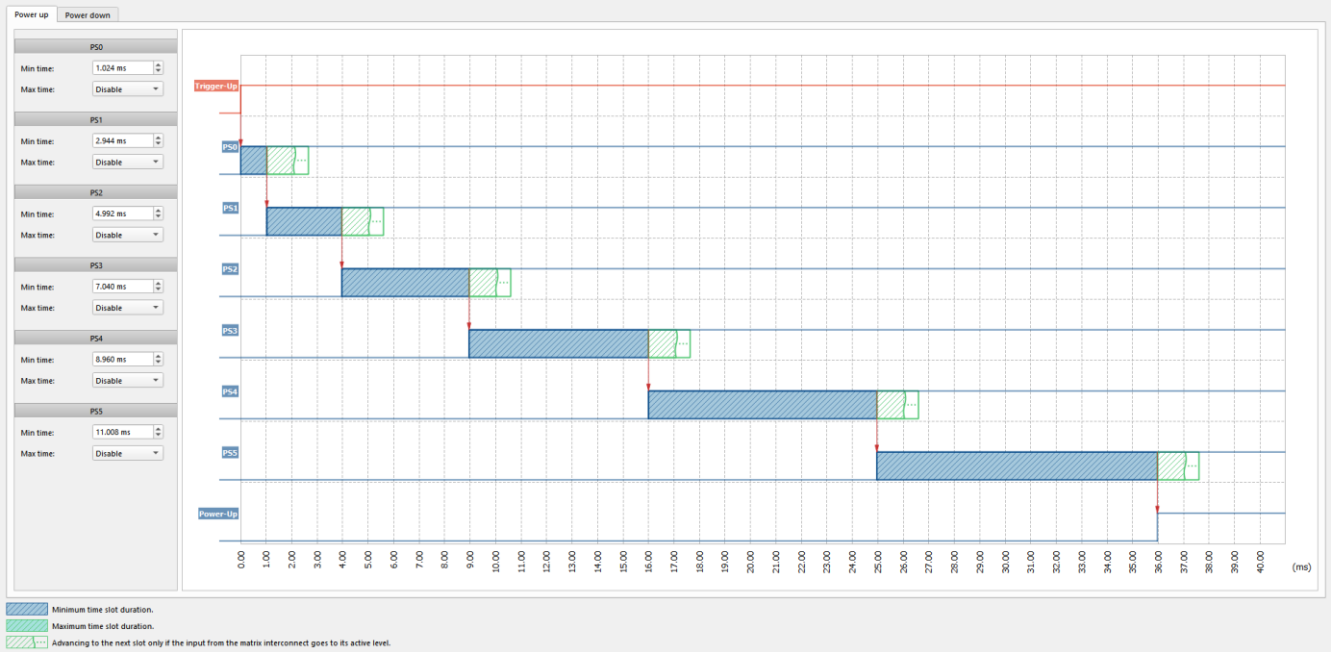


Figure 3a: State control timing diagrams of power sequencer triggered by GPIO - Power up sequence

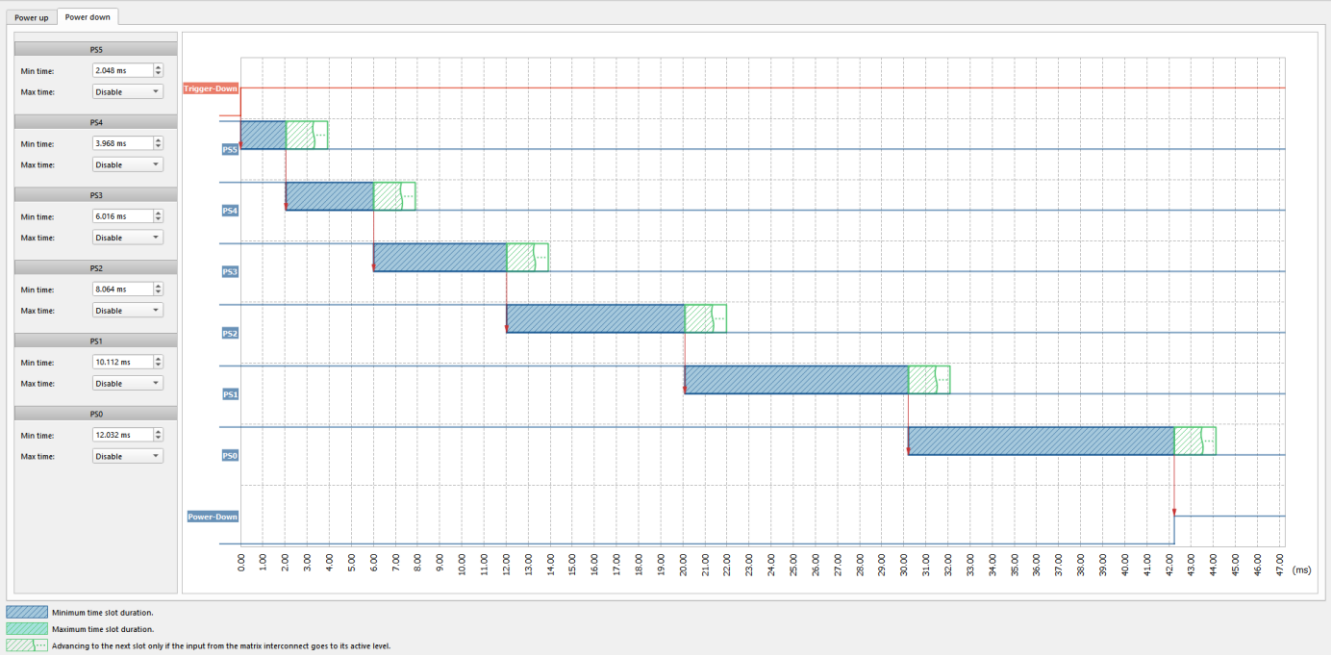


Figure 3b: State control timing diagrams of power sequencer triggered by GPIO - Power down sequence

Note: Min time duration limits support a range of 0 to 32.64ms with a resolution of 128µs.

Max time duration limits support options of 10, 30, 50ms or disable. When Max time is set to Disable, advancing to the next slot happens when the input from the matrix interconnect goes to its active level.

c) **Idle** allows initiation of power-up sequence with the trigger-up control signal from the matrix interconnect.

d) **Seq Up** initiates power-down sequence by applying trigger-down control signal from the matrix interconnect.

e) **Timer Expired** is the power sequencer component that outputs signals/flags if any of six discrete periods of time (slots) between events reaches the minimum or maximum set slot duration limits.

f) **Crash Sequence** is triggered either from the main FSM error conditions or from the power sequencer's trigger-crash input from the matrix interconnect. The crash sequence operates in the same way as a power-down sequence with the exception that only the minimum slot timer is used to control slot advancing. The power-down enable inputs from the matrix interconnect are ignored during crash sequences.

If a crash sequence is triggered in the Seq up state, the power sequencer crashes down to the Idle state through states PS5 to PS0.

If a crash sequence is triggered during a power-up sequence (PS0 to PS5), the power sequencer begins the crash sequence by directly entering the PS5 state before crashing down to the Idle state through states PS4 to PS0. No extra resources are enabled as a result of jumping directly to the PS5 state from a lower power-up sequence state.

If a crash sequence is triggered during a power-down sequence (PS5 to PS0), the power sequencer crashes down to the Idle state from its current state.

6. Typical Scenarios

6.1 Six Rail Power Sequencer Triggered by GPIO

In this scenario, LDO1 to LDO6 need to be powered-up/down one-by-one via GPIO1 in accordance with trigger-up/down and slots sensitivity configurations on Figure 4. On the timing diagrams (Figure 5, Figure 6), PS stands for the Power sequencer slot and represents the expected delay time that is individually configured for each sequence.

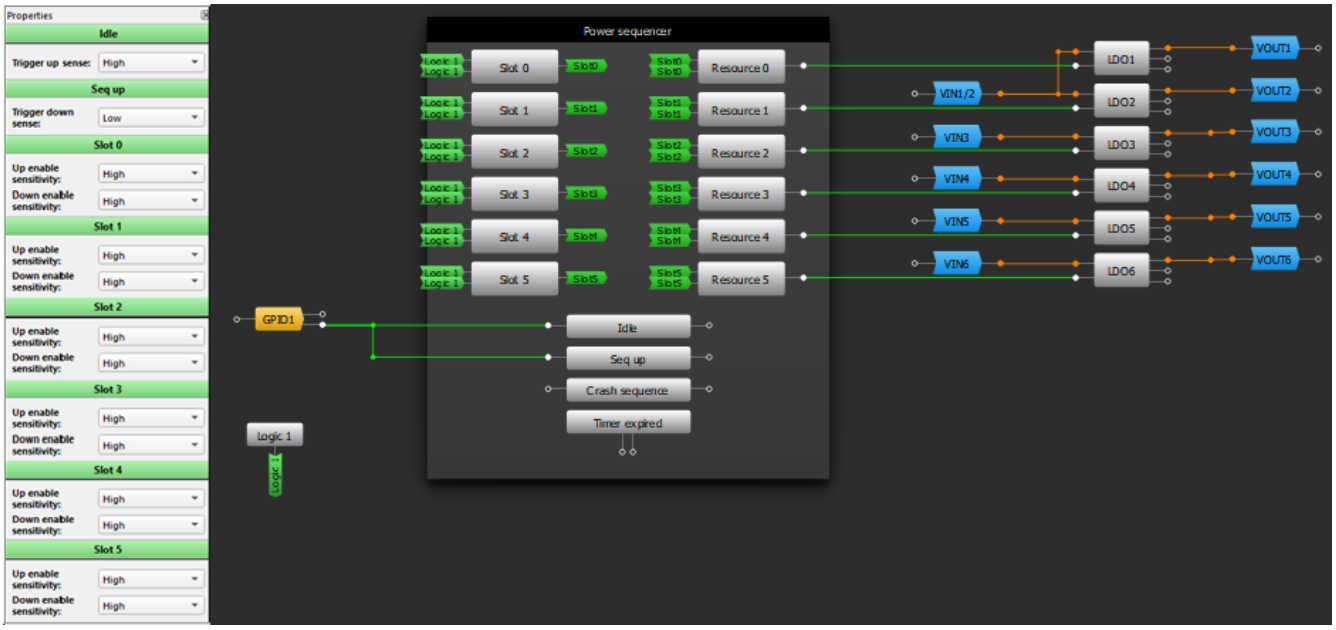


Figure 4: Six rail Power Sequencer triggered by GPIO

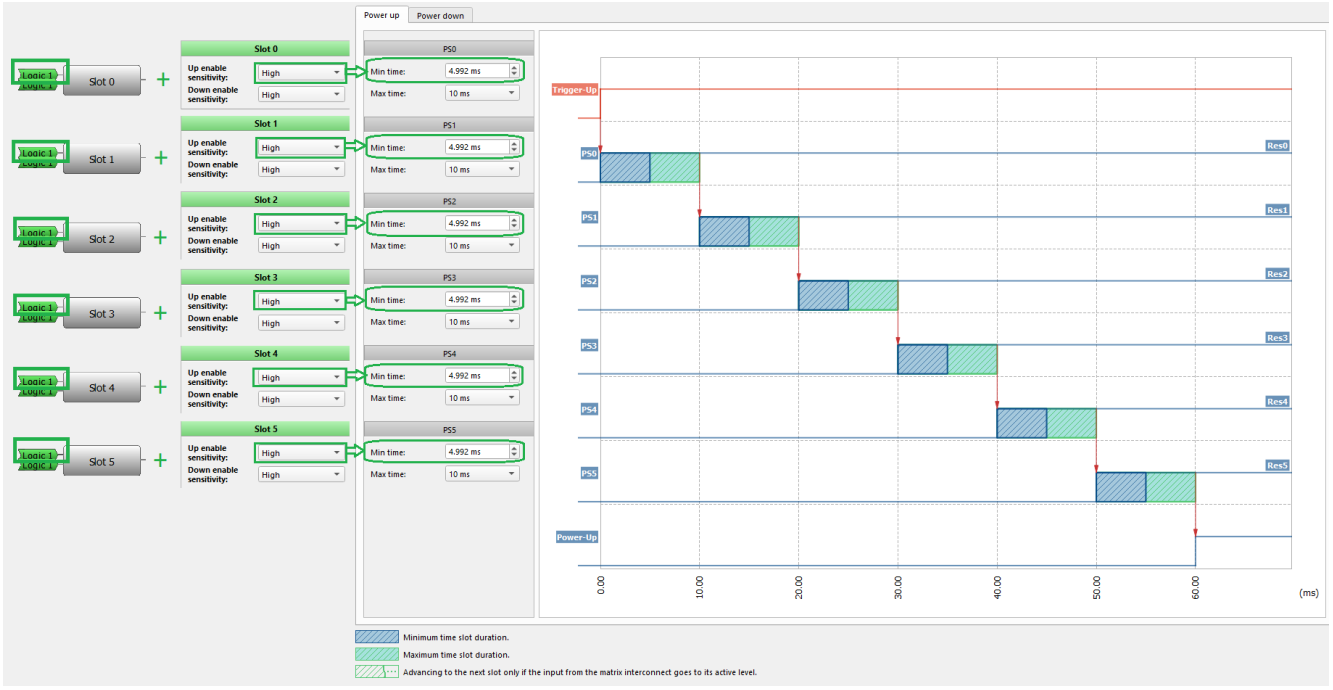


Figure 5: Expected power up timing diagram of power sequencer triggered by GPIO

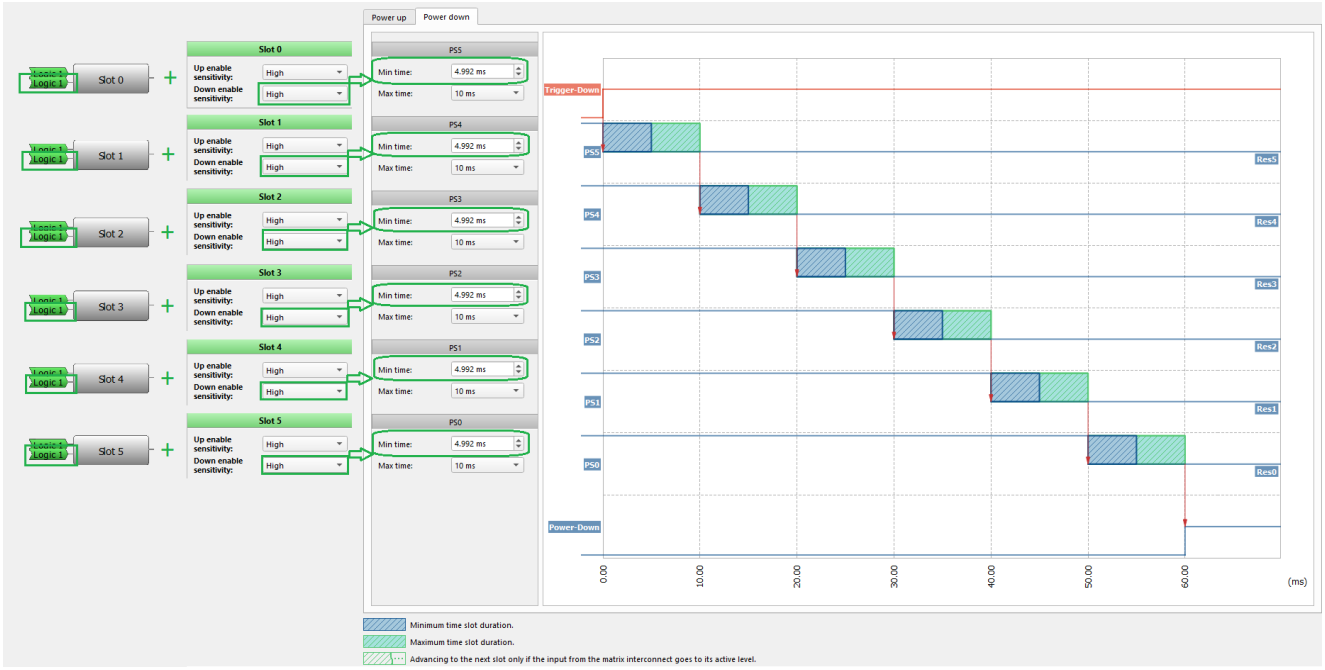


Figure 6: Expected power down timing diagram of power sequencer triggered by GPIO

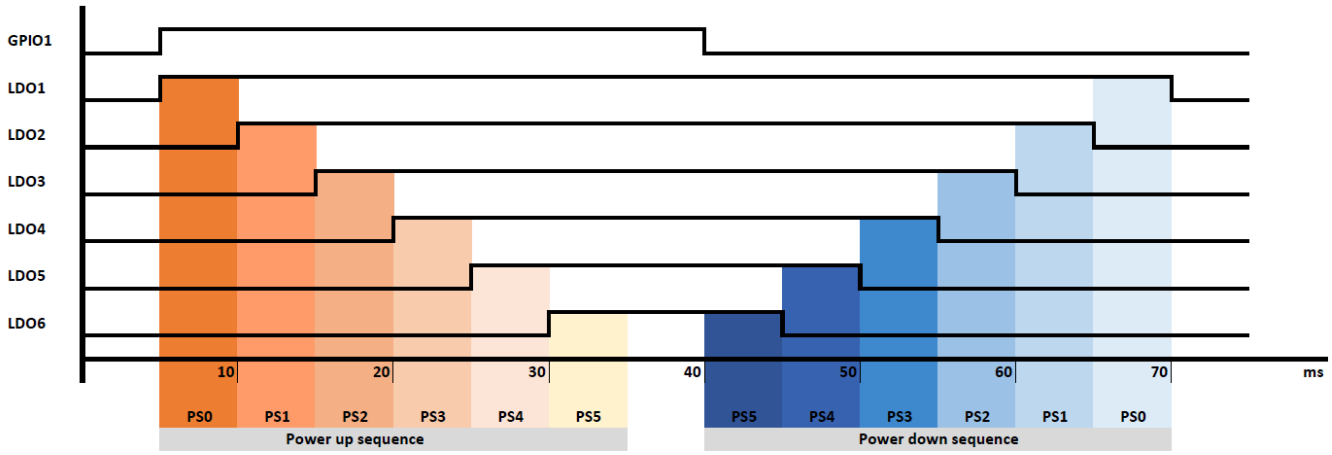


Figure 7: Desired timing diagram of power sequencer triggered by GPIO

6.2 Up/down Slot Sensitivity Setting Example

Power slots have min (range from 0 to 32.64ms with a resolution of 128µs) or max (10, 30, 50ms or Disable) sequencing times. It is possible to configure sensitivity settings and change delay times by matching or mismatching the input trigger event with sensitivity settings on slots. Use static slot configurations with a hard matrix interconnect to “Logic 1” or “Logic 0” for permanent configuration or use the I2C block or GPIO for flexibility in selecting min or max delay times during chip operation.

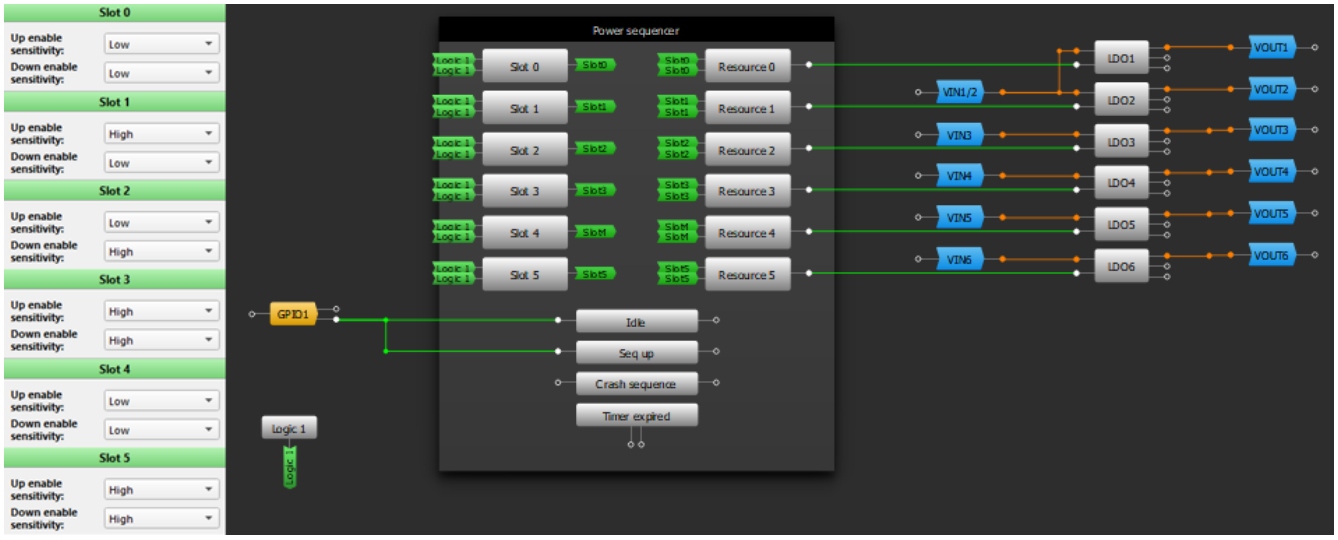


Figure 8: Power Sequencer triggered by GPIO with different up/down sensitivity settings

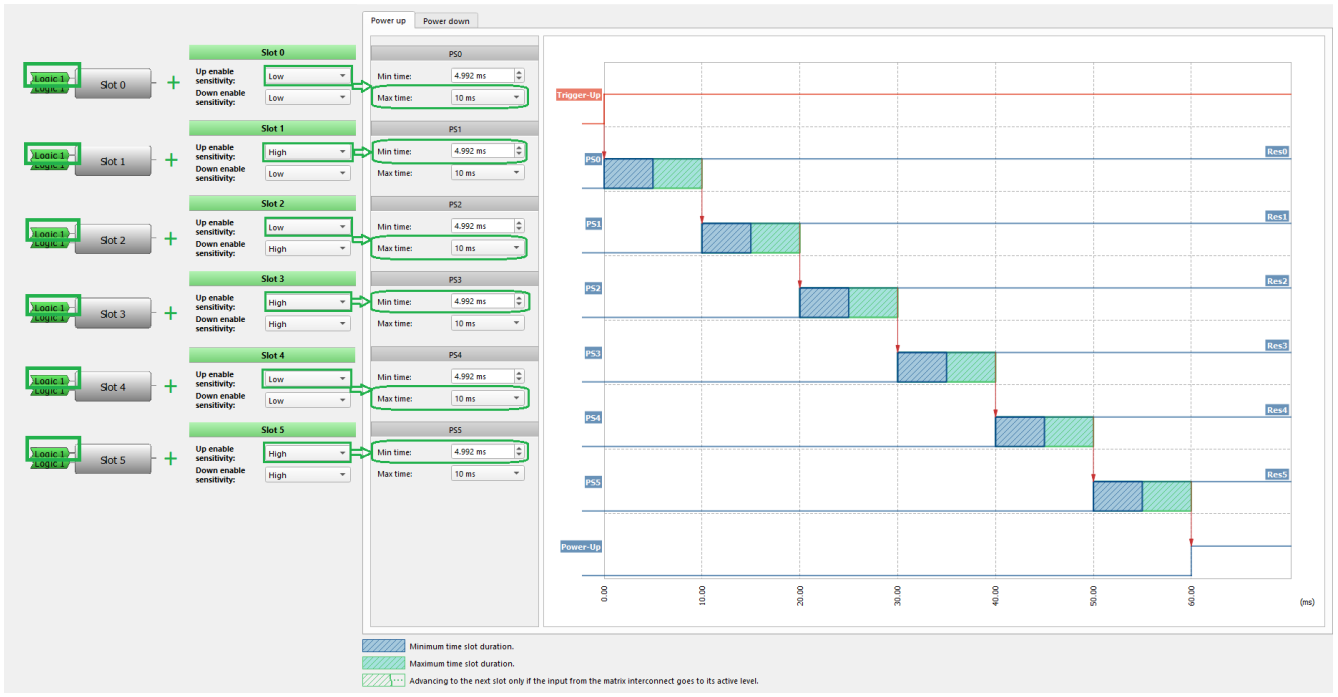


Figure 9: Expected power up timing diagram of power sequencer triggered by GPIO with different up/down sensitivity settings

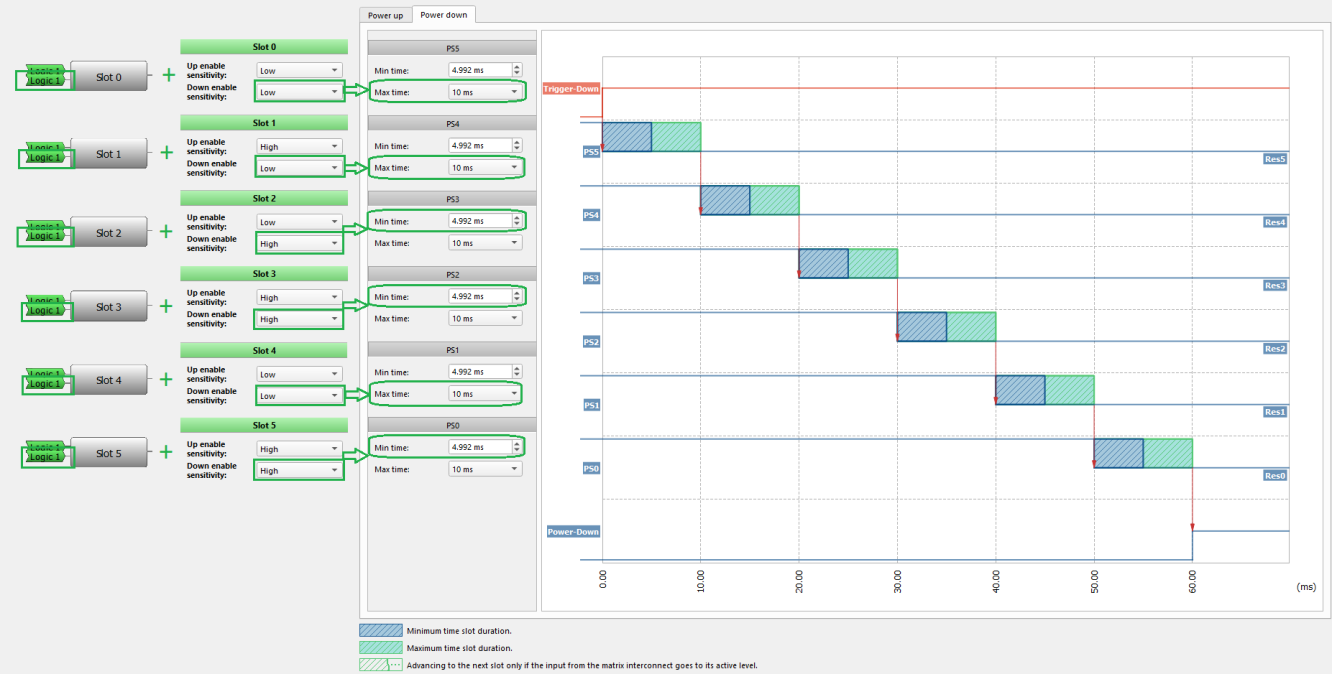


Figure 10: Expected power down timing diagram of power sequencer triggered by GPIO with different up/down sensitivity settings

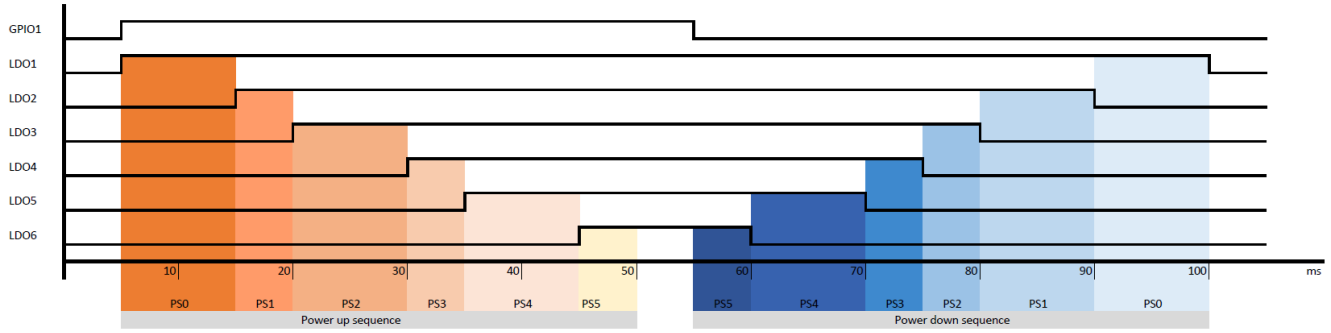


Figure 11 : Desired timing diagram of power sequencer triggered by GPIO with different up/down sensitivity settings

6.3 Multiple Resources Configuration Example

Some special cases require a startup with specific combinations of rail. The Power Sequencer can use flexible programmed sequencing with multiple rail startup configurations, skipped slots for longer delay time and different configured rails on Power up and Power down. Figure 12 shows an example of this.

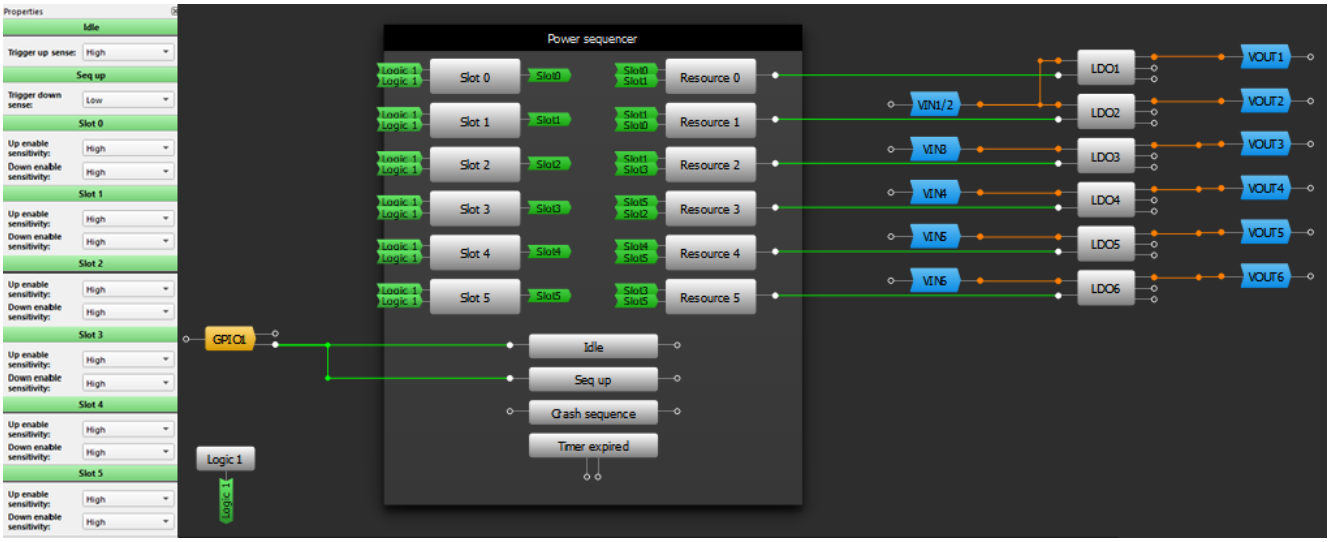


Figure 12: Multiple start up design

Table 3: Expected look-up table with multiple startups according to the example design

Event	In	Out	Selected LDOs
IDLE (Power up)	Slot 0	Resource 0	LDO1
	Slot 1	Resource 1, Resource 2	LDO2, LDO3
	Slot 2	-	-
	Slot 3	Resource 5	LDO6
	Slot 4	Resource 4	LDO5
	Slot 5	Resource 3	LDO4
SEQ UP (Power down)	Slot 5	Resource 4, Resource 5	LDO5, LDO6
	Slot 4	-	-
	Slot 3	Resource 2	LDO3
	Slot 2	Resource 3	LDO4
	Slot 1	Resource 0	LDO1
	Slot 0	Resource 1	LDO2

***Note:** when you are setting up multiple start up, look at the **State control timing diagram** in the Go Configure Software Hub to check output resources enabled in accordance with slots.

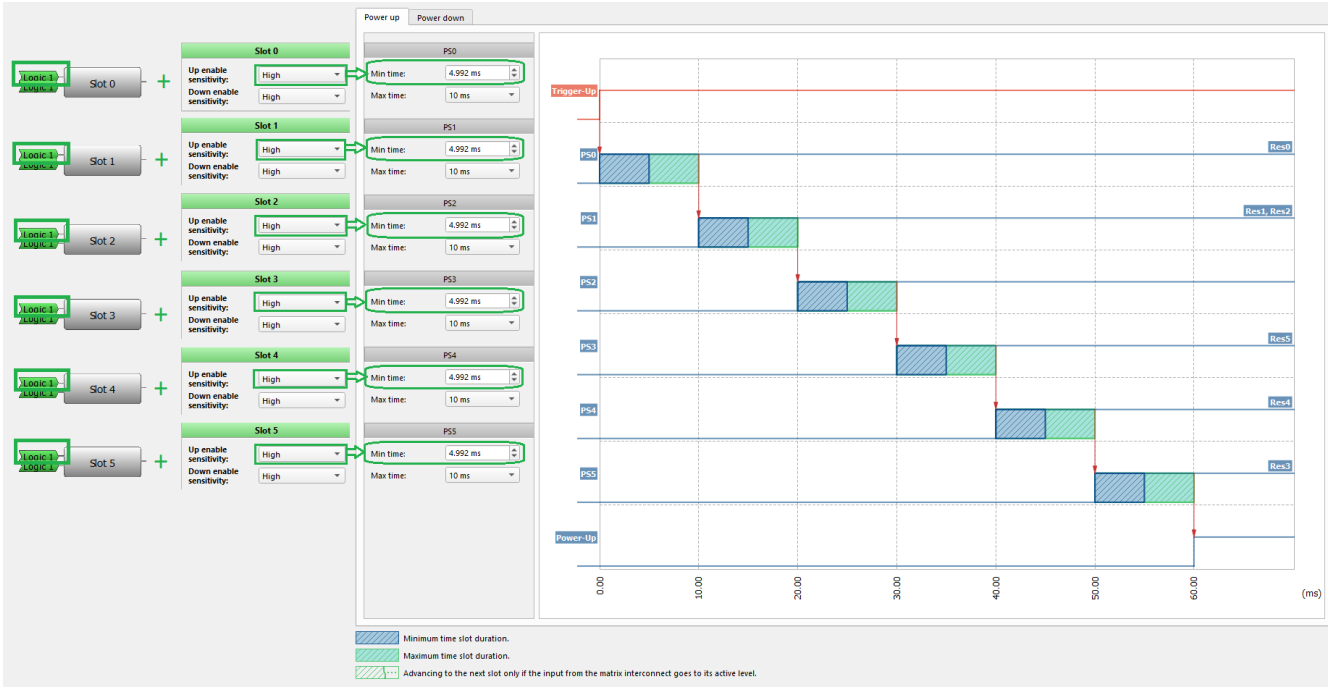


Figure 13: Power up timing diagram triggered by GPIO with multiple up/down start up

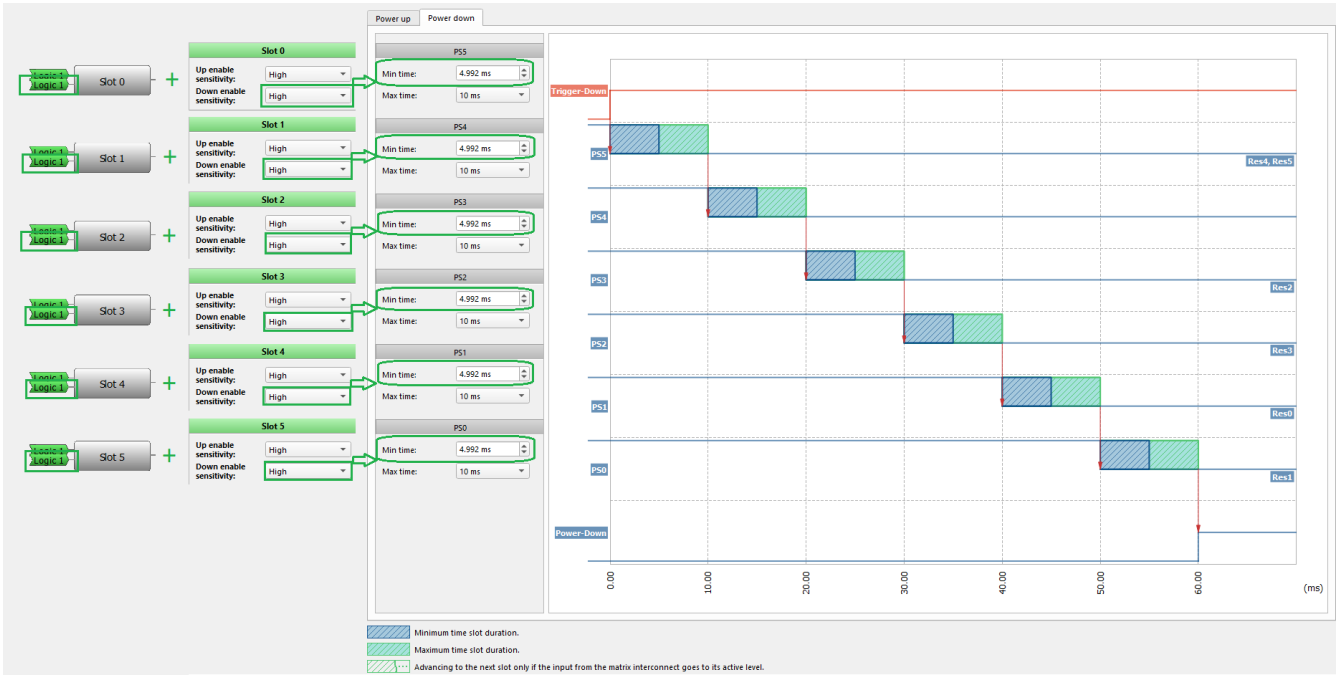


Figure 14: Power down timing diagram triggered by GPIO with multiple up/down start up

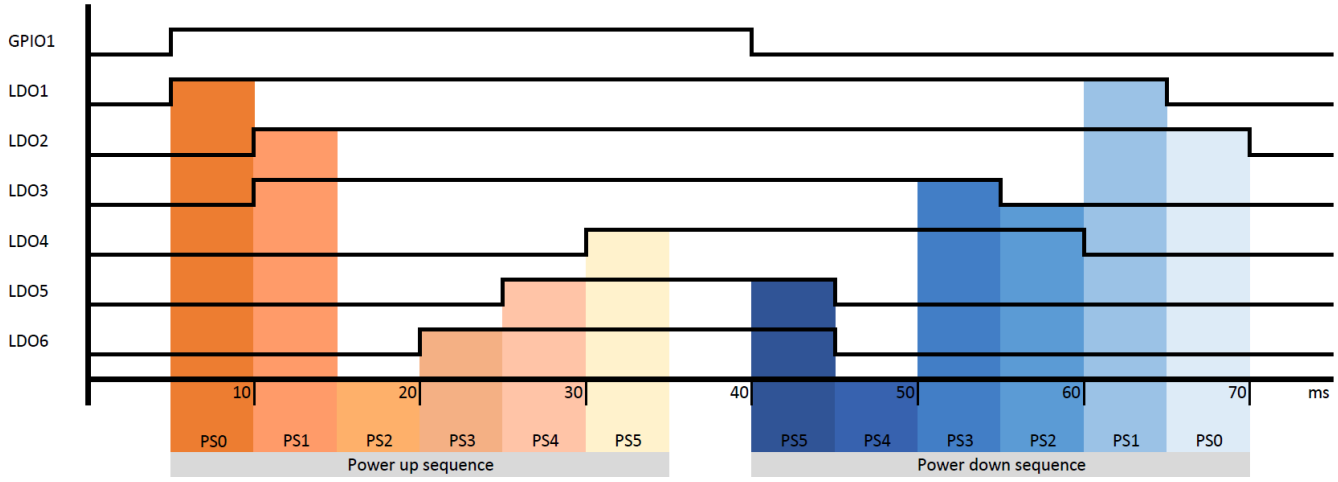


Figure 15: Desired timing diagram of power sequencer triggered by GPIO with multiple up/down settings

6.4 Power Slots Controlled by GPIOs, “Disable” Power Slot

The GPIOs can be used to control duration time. This provides a flexible power sequencer that controls the power-up/down timings. Figure 16 shows the selected sequence time is divided between external events from GPIOs per two slots on each, from GPIO2 to GPIO4.

The “Disable” option provides the possibility to wait or check external signals on a slot`s input and continue the sequence according to the programmed scenario.

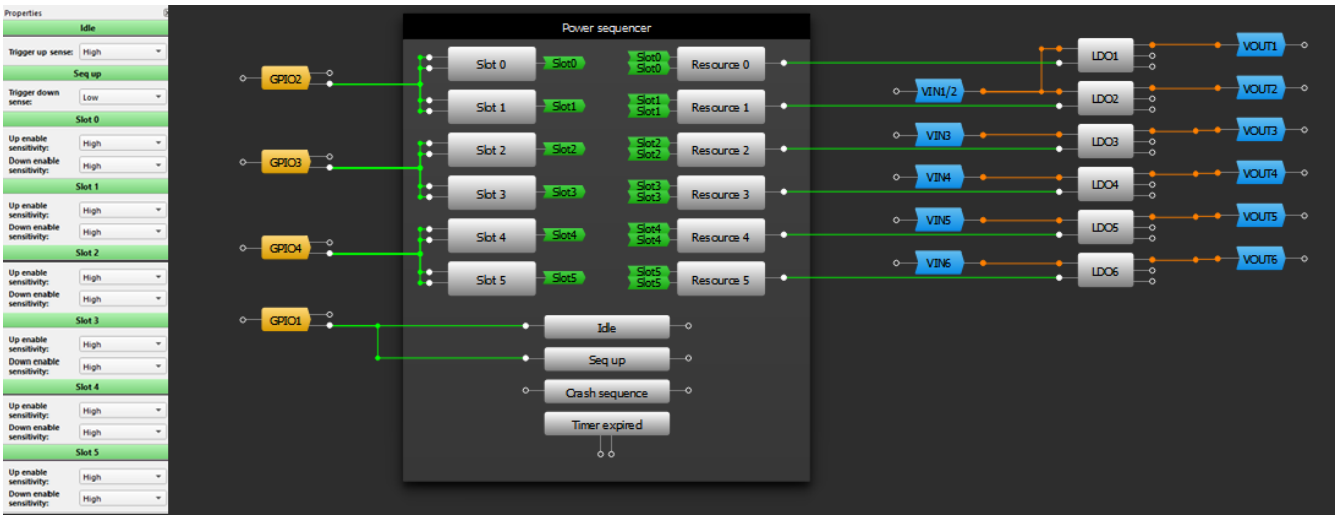


Figure 16: Power slots min/max time controlled by GPIOs

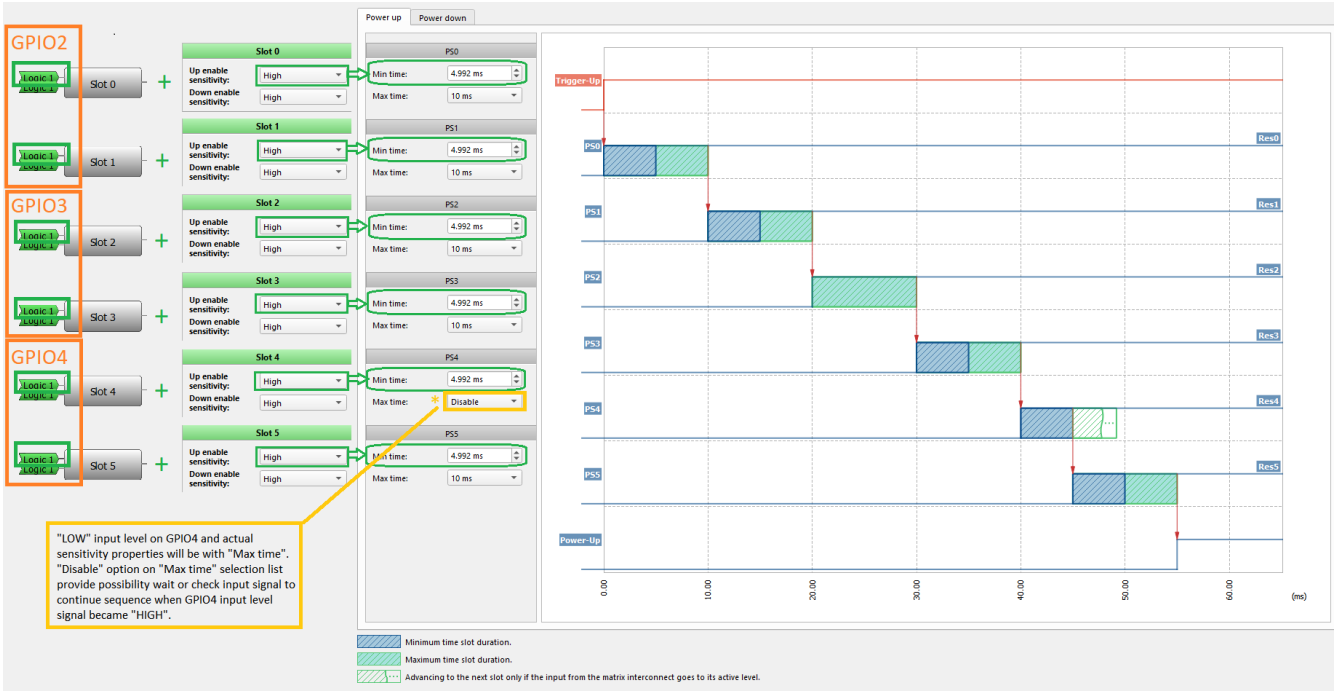


Figure 17: Power up timing diagram with “Disable” on PS4 and min/max time controlled by GPIOs

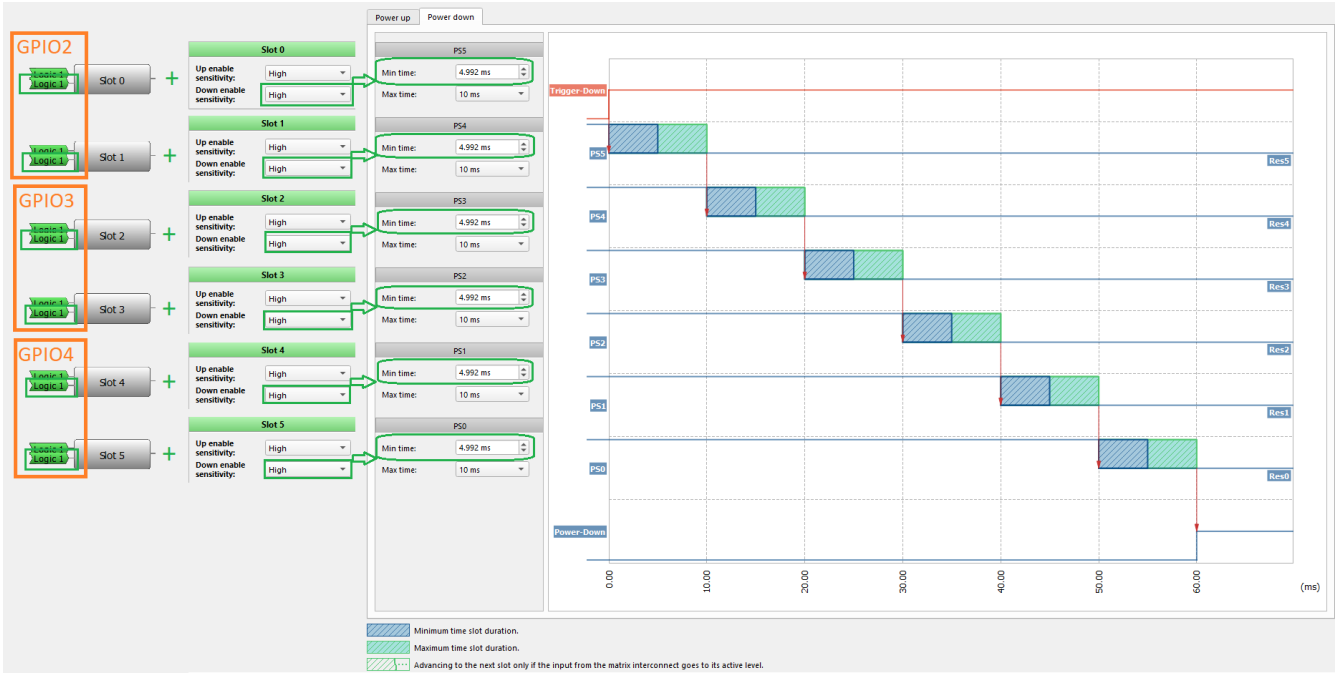


Figure 18: Power down timing diagram with min/max time controlled by GPIOs

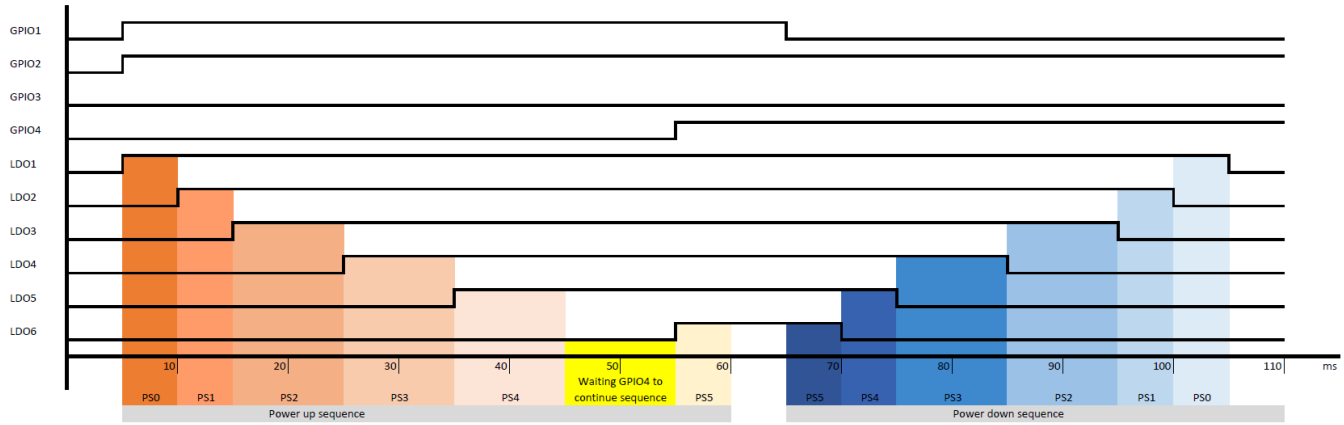


Figure 19: Desired timing diagram of power sequencer with min/max time controlled by GPIOs

6.5 Power Up/Down, Power Slots Controlled by I2C

Another way to use the Power Sequencer is to control it via the I2C block. This allows one to control the PMIC`s sequencing scenarios with an external MCU. Figure 20 shows a simple example with power up, power down and the slot's min or max time duration selected by I2C commands.

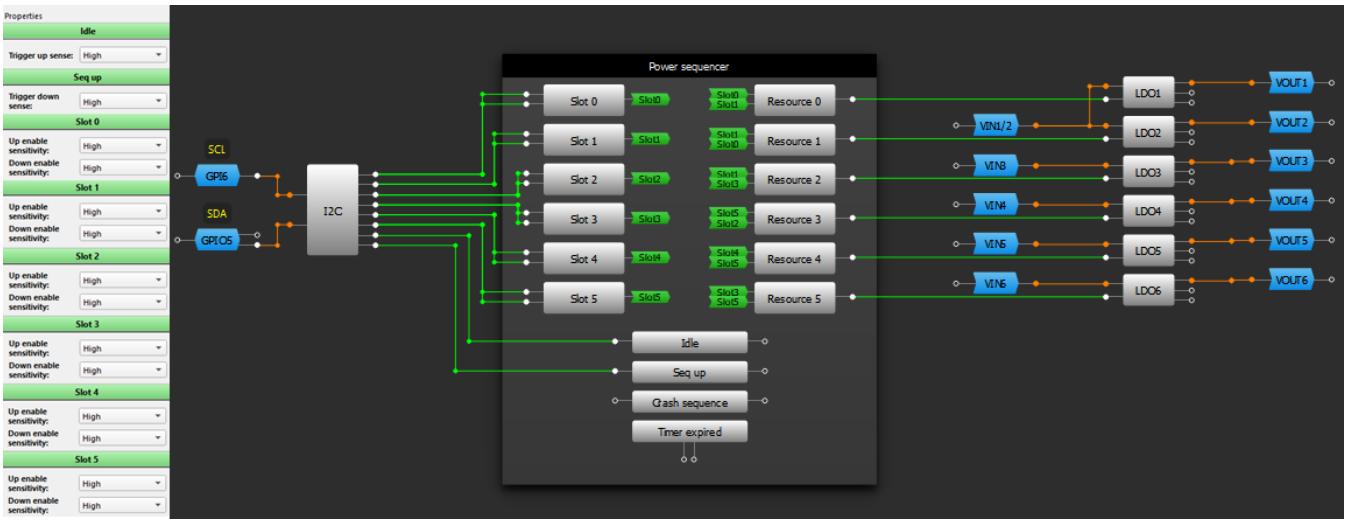


Figure 20: Power slots min/max time, Power up/down controlled by I2C

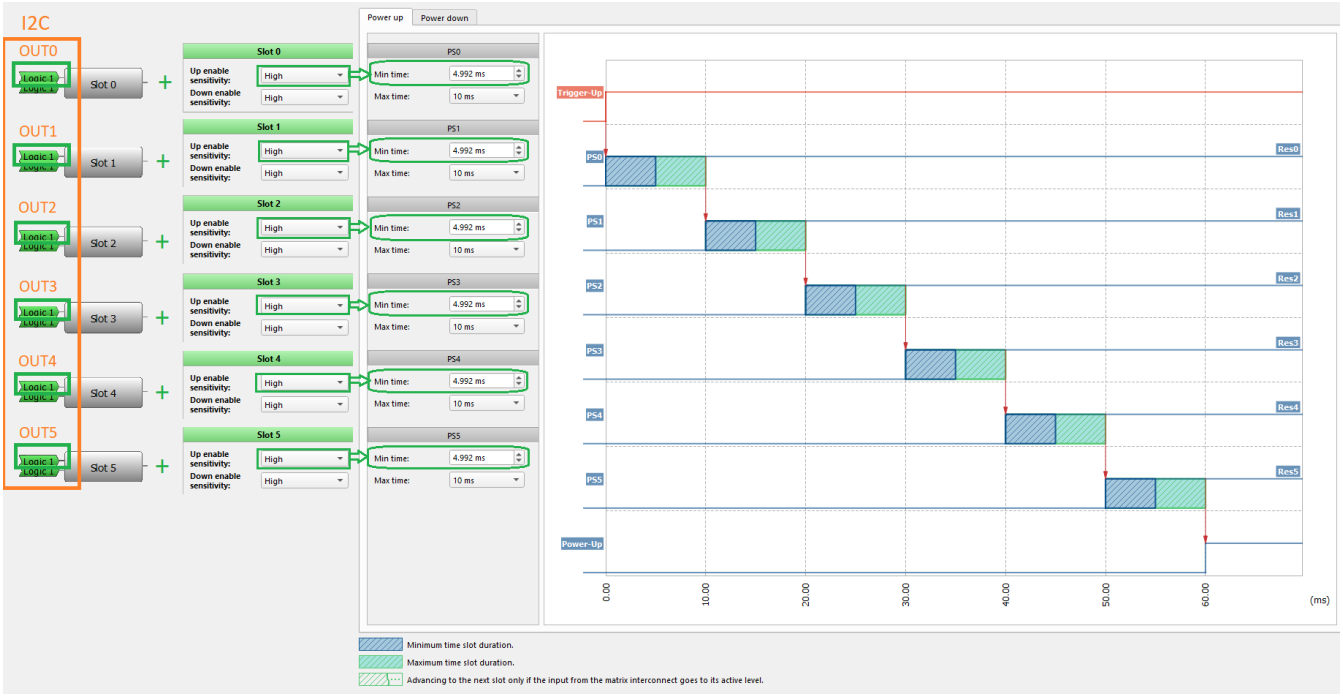


Figure 21: Timing diagram of Power up and min/max slots time controlled by I2C

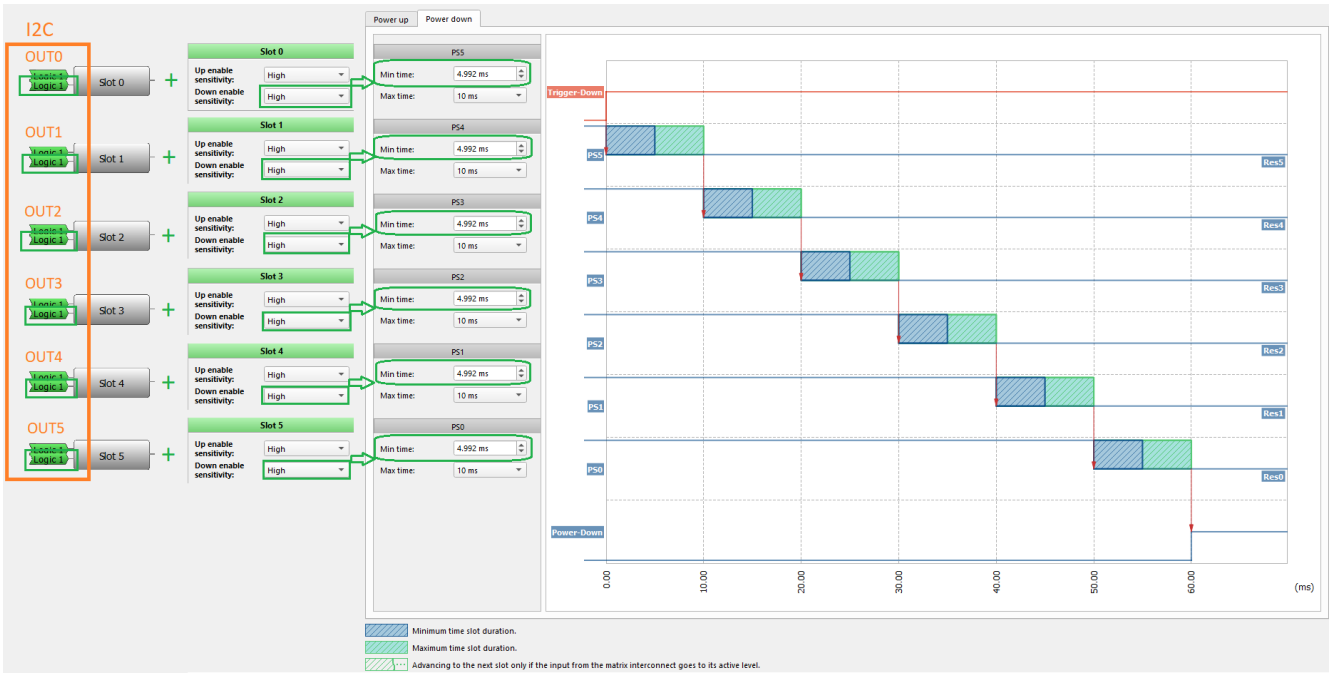


Figure 22: Timing diagram of Power down and min/max slot time controlled by I2C

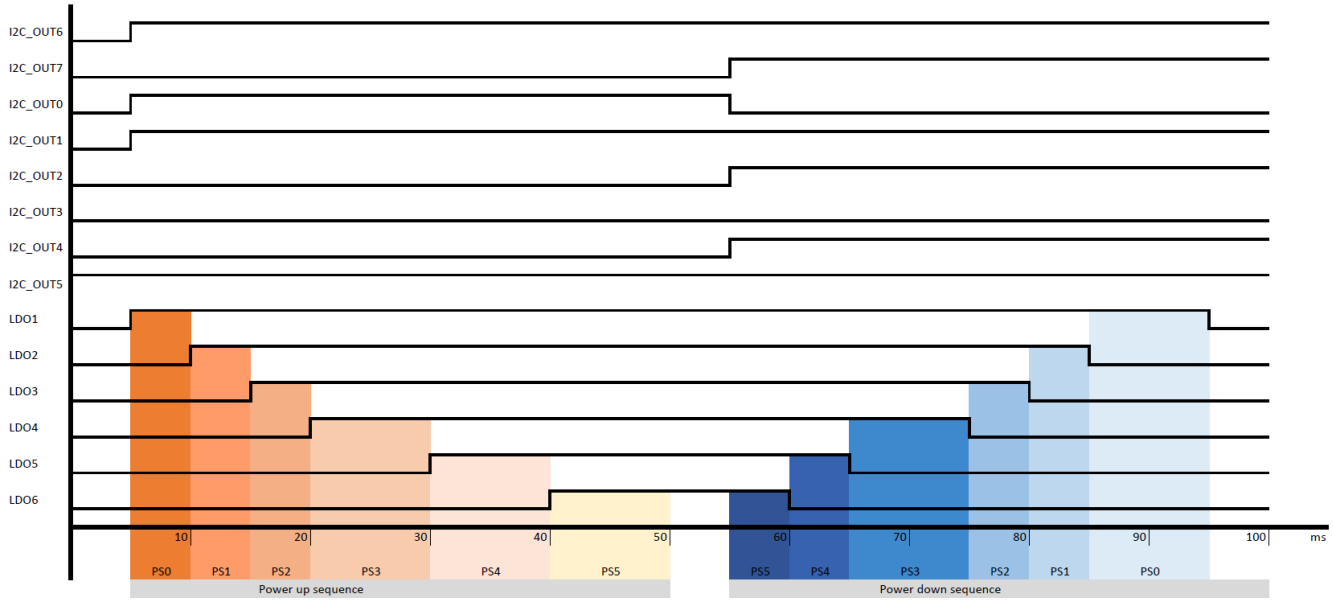


Figure 23: Desired timing diagram of Power down and min/max slot time controlled by I2C

6.6 Crash Sequence Event Example

The block provides an emergency interrupt of sequences with external (GPIO, I2C) or internal (Temp sensor, LDO_VOUT_OK, ILIM, LUT configured settings) signal trigger events, and operates only the minimum slot timer to control slot advancing even if the maximum time is configured. The power-down enable inputs from the matrix interconnect are ignored during crash sequences.

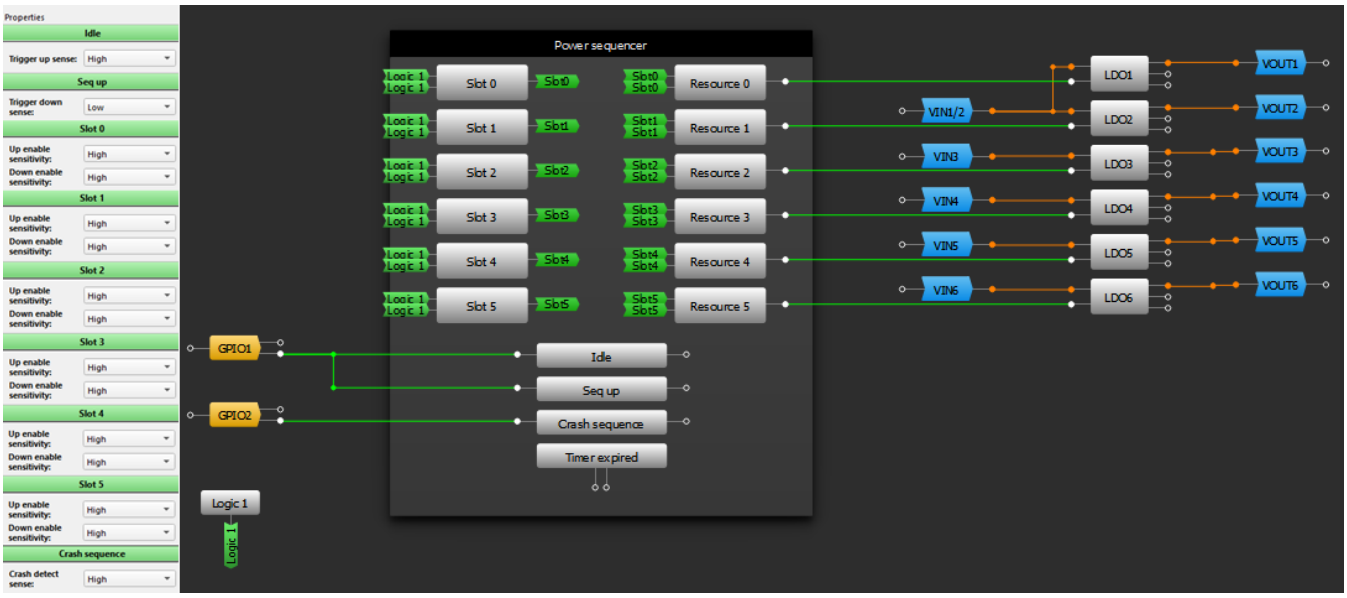


Figure 24: Power up/down and Crash Sequencer controlled by GPIO

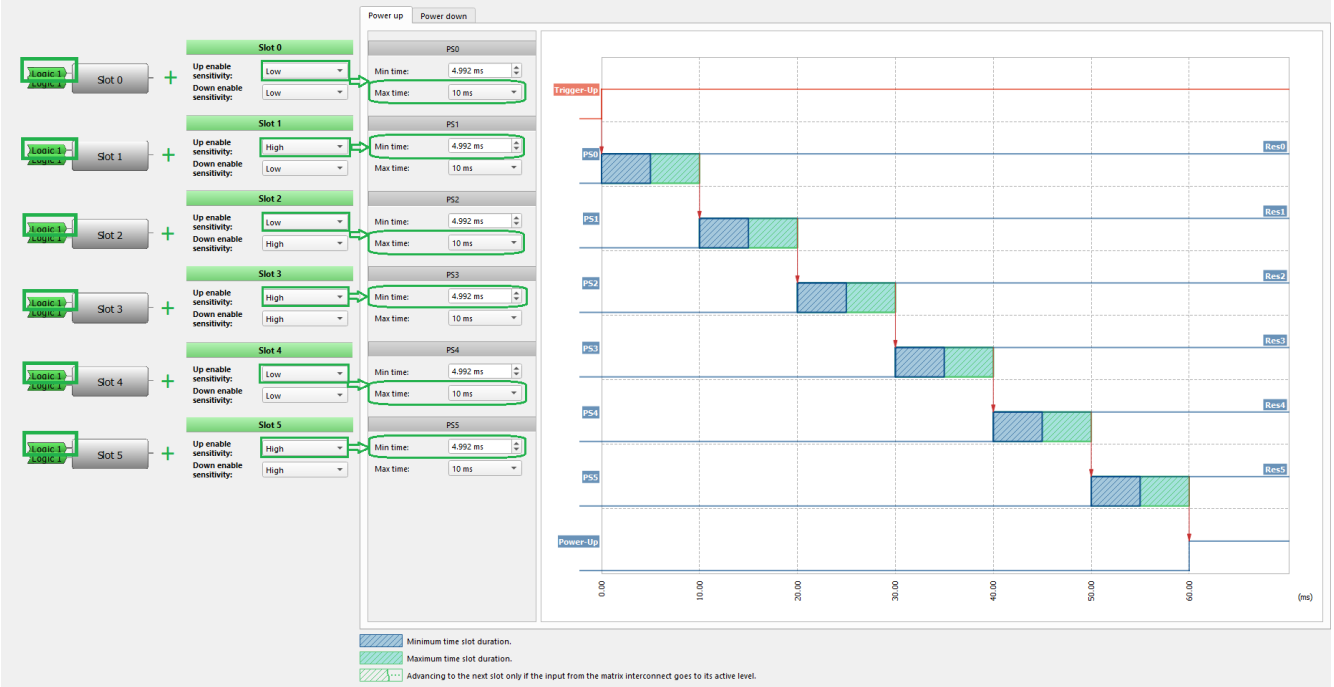


Figure 25: Timing diagram of Power up

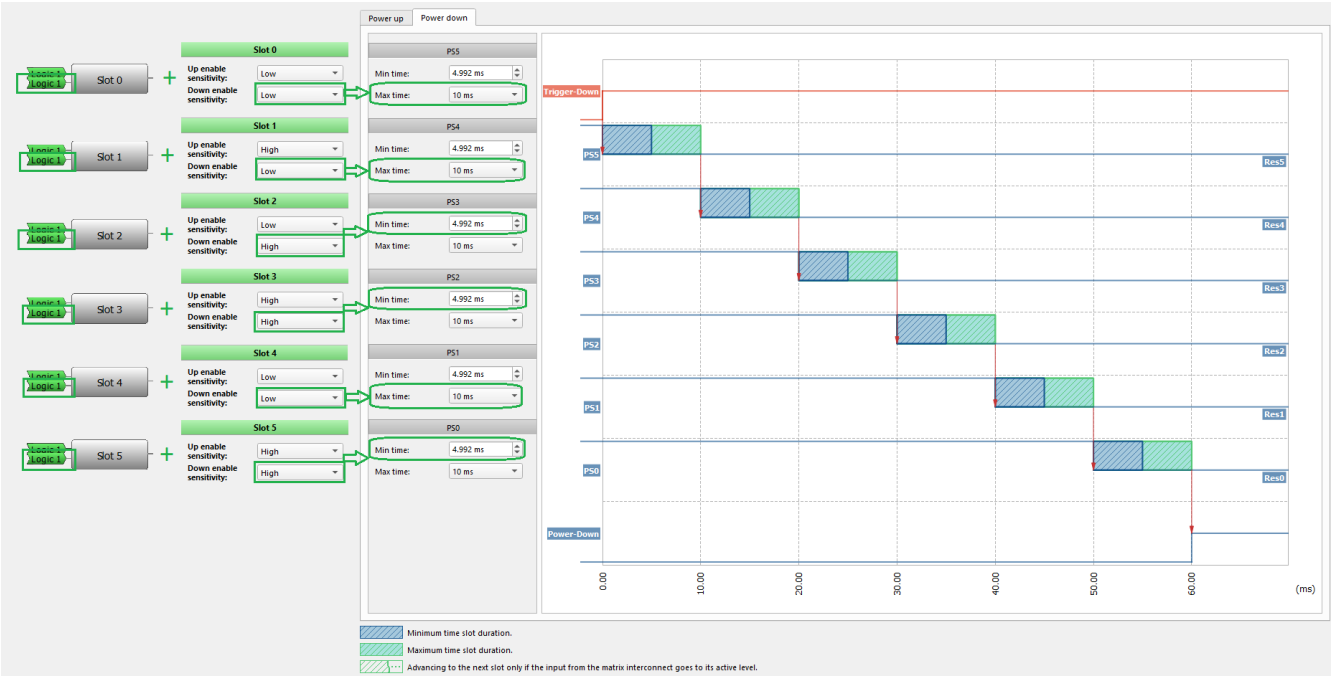


Figure 26: Timing diagram of Power down

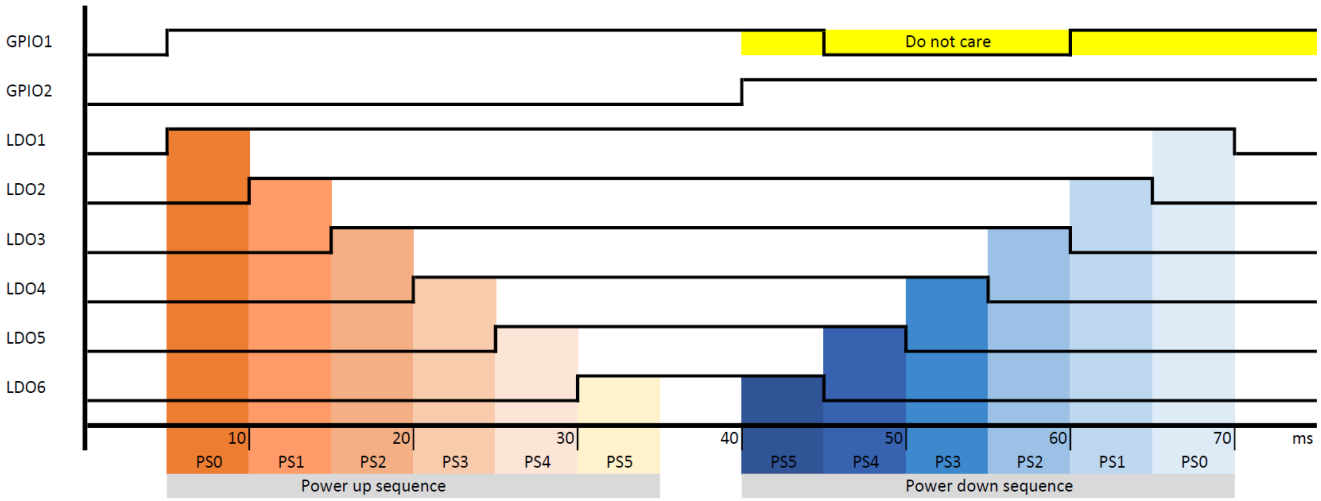


Figure 27: Desired timing diagram of power sequencer with crash sequence triggered by GPIOs

7. Conclusion

The SLG5100X Power Sequencer allows for a variety of configurations. It can provide very flexible usage with customized power up and power down sequences. Sequencing can be controlled by a hardwired connection through GPIOs or using an external MCU with an I2C block by sending control commands.

8. Revision History

Revision	Date	Description
1.00	Nov 7, 2022	Initial release.

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