SLG47105 Buck, Boost, Buck-Boost Converter

This application note describes how to design and build Buck, Boost, and Buck-Boost converters.

The converters are built on the SLG47105. The IC is equipped with two high-current bridge outputs which eliminate the need for external transistors or Schottky diodes leaving only one external power component – the inductance. In addition, the SLG47105 contains numerous different macrocells which allows the user to easily create the circuit up to the task.

The application note comes complete with a design file that can be found in the References section.

Contents

1. Terms and Definitions

ACMP	Analog Comparator
CNT/DLY	Counter-Delay
DC	Direct current
DFF	D Flip-flop
FET	Field Effect Transistor
GPO	General Purpose Output
HV	High Voltage
IC	Integrated Circuit
I/O	Input / Output
I2C	Inter-Integrated Circuit Protocol
LED	Light Emitting Diode
LUT	Look-up Table
MF	Multi-function Macrocell
OSC	Oscillator
OCP	Overcurrent Protection
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
SCL	Signal Clock
SDA	Signal Data

2. References

For related documents and software, please visit:

HVPAK™ | Renesas

Download our free Go Configure software hub and use the HVPAK development tools to freeze the design into your own customized IC in a matter of minutes.

[1] Go Configure Software Hub, Renesas Electronics
[2] AN-CM-358 SLG47105 Buck, Boost, Buck-Boost Converter, design file
[3] GreenPAK Application Notes, Application Notes Library, Renesas Electronics
[4] SLG47105 Datasheet, Renesas Electronics
[5] Buck-Boost Converters
[6] Breakthrough Buck-Boost Controller
[7] https://x-engineer.org/dc-dc-converter/

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3. Introduction

DC-DC converters are widely used to efficiently produce a regulated voltage from a source that may or may not be well controlled to a load that may or may not be constant. This paper briefly introduces DC-DC converters using the SLG47105 IC, simple examples, suggestions on further improvements, and adding extra features.

DC-DC converters are high-frequency power conversion circuits that use high-frequency switching and inductors, transformers, and capacitors to smooth out switching noise into regulated DC voltages. Closed feedback loops maintain constant voltage output even when changing input voltages and output currents. At 90% efficiency, they are generally much more efficient and smaller than linear regulators. Their disadvantages are noise and complexity.DC-DC converters come in non-isolated and isolated varieties. Isolation is determined by whether or

not the input ground is connected to the output ground. This paper describes the non-isolated converters only (buck, boost, and buck-boost), but the IC capabilities allow for designing the isolated ones as well.

A buck converter steps voltage down, producing voltage lower than the input voltage. For example, a buck converter could be used to charge a lithium-ion battery to 4.2 V, from a 5 V USB source.

A boost converter steps voltage up, producing voltage higher than the input voltage. A boost converter could be used to drive a string of LEDs from a lithium cell or provide a 5 V USB output from a lithium cell.

A buck-boost converter steps a voltage up or down, producing a voltage equal to or higher or lower than the input voltage. A buck-boost could be used to provide a 12 V output from a 12 V battery. A 12V battery's voltage can vary between 10 V and 14.7 V. A buck-boost could also power an LED from a single cell. An LED forward drop is about 3.2 V. A lithium battery cell can vary between 2.5 and 4.2 V, see section 6. Buck-Boost Converter for detailed project description.

4. Buck Converter

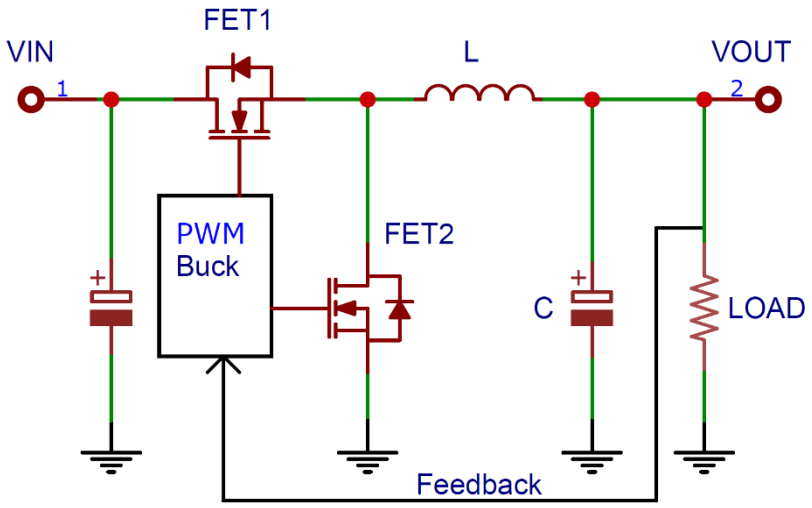

Figure 1: Buck DC-DC Converter Schematic

Buck DC-DC converter, also called a step-down DC-DC converter, is a DC-DC power converter that lowers the output voltage while increasing the output current. It consists of at least four components:

- a power transistor used as a switching element (FET1)
- a synchronous rectifier (FET2)
- an inductor (L) as an energy storage element
- a filter capacitor (C)

The relationships between input and output voltage, current, and power are as follows:

- $V_{out} < V_{in}$
- $I_{out} > I_{in}$
- $P_{out} = P_{in} – P_{loss}$

4.1 Theory of Operation

When each cycle begins, FET 1 turns on first and the inductor current is determined by comparing the feedback loop voltage to an internal reference. When the sense voltage drops below the reference, FET 1 turns off and FET 2 turns on for the remainder of the cycle. FETs 1 and 2 turn on and off alternately, behaving like a typical synchronous buck regulator. The duty cycle of FET 1 increases until the maximum duty cycle of the converter reaches 94%–98%.

As an example, a simple buck converter was designed using the SLG47105 IC and Go Configure software, see Figure 2. It has the following parameters

- Input voltage range (Vin) : 3.6 to 5.5 V
- Output voltage : 3.3 V
- Output current range : 0.5 - 1 A
- PWM frequency : 200 kHz
- Overcurrent/sort circuit protection – internal OCP

Calculated values:

- Rated Peak Withstand Current (Ipk) : 2 A
- Inductance (Lmin) : 2 uH (2.2 uH, 2.5A rated)
- Filter Capacitor (C) : 25 uF (47 uF to 100 uF low ESR capacitor is recommended)

4.2 Go Configure Software Hub Project

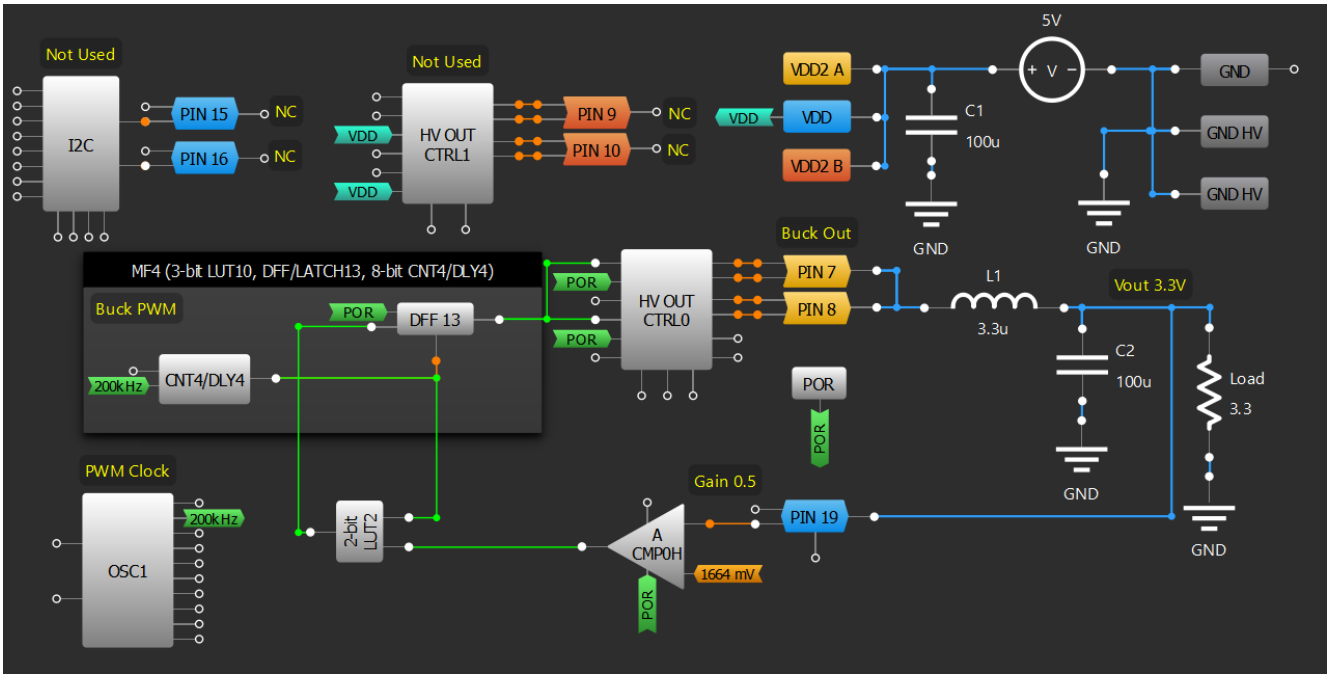

Figure 2: Buck DC-DC Converter Project

The regulator uses a 200 kHz clock which is OSC1 25 MHz divided by 125 using the Flexible divider. This frequency was chosen as a compromise between two requirements:

1. The highest possible frequency so the smallest inductance coil and filter capacitor could be used
2. Low enough frequency to ensure the highest efficiency of the HV outputs

The buck PWM logic is built on MF4 (CNT4/DLY4 and DFF 13) and 2-bit LUT2. The CNT4/DLY4 sets the maximum duty cycle of 96.6 %. It remains at maximum until the feedback signal from the ACMP0H through 2-bit LUT2 cuts it. This is for regulating the output voltage.

It is also possible to use one of two digital PWM microcells within the IC but since they're only 8-bit macrocells, the output voltage stability will be limited to PWM steps plus ACMP input offset voltage:

$$\Delta \boldsymbol{Vout} = \left(\frac{\boldsymbol{Vref}}{\mathbf{256}} \times \frac{\mathbf{1}}{\boldsymbol{G}}\right) + \boldsymbol{Voffset} = \left(\frac{\mathbf{1664}}{\mathbf{256}} \times \frac{\mathbf{1}}{\mathbf{0.5}}\right) + \mathbf{6.5} = 19.5 \text{ (mV)}$$

Where:

Δvout – output voltage drift

Vref – internal voltage reference

G – ACMP IN+ gain

Voffset – ACMP input offset voltage

On the contrary, if using an analog PWM built on MF4 (CNT4/DLY4 and DFF 13) and 2-bit LUT2, the output voltage stability will be limited to ACMP input offset voltage only. It should be mentioned that there are several factors that increase the output voltage instability, such as macrocells propagation delay and other parasitic parameters. The final result will be affect and will be a bit worse .

The HV OUT CTRL0 macrocell is configured as a fast slew rate half-bridge output. It has two half-bridge outputs which are connected in parallel to handle higher output current. Output pins (Pin 7 and Pin 8) are configured to «High and Low side on».

The ACMP0H in this design is used in a voltage feedback loop so the PWM could stabilize the output voltage. The output voltage is determined by the ACMP's Vref and the IN+ internal voltage divider. In this case

$$\boldsymbol{Vout = \frac{Vref}{G} = \frac{1664}{0.5} = 3.328\ (V)}$$

Where:

Vref – internal voltage reference

G – ACMP IN+ gain

The flexibility of the SLG47105 allows building of either two different converters using also the HV OUT CTRL1 and ACMP1H or connecting all HV outputs together for even higher output currents.

5. Boost Converter

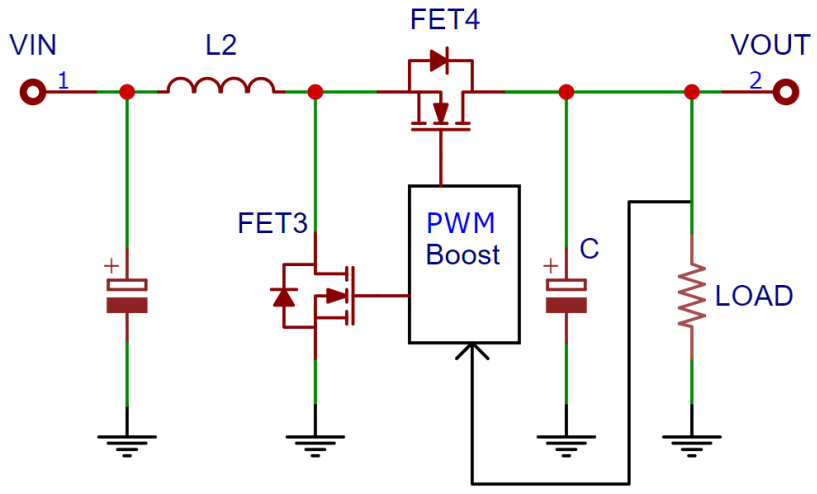

Figure 3: Boost DC-DC Converter Schematic

Boost DC-DC converter also called a step-up DC-DC converter, is a DC-DC power converter that increases the output voltage while decreasing the output current. It contains the same components as a buck DC-DC converter but is arranged in a different topology.
The relationships between input and output voltage, current, and power are as follows:

- $U_{out} > U_{in}$
- $I_{out} < I_{in}$
- $P_{out} = P_{in} – P_{loss}$

5.1 Theory of Operation

When each cycle begins, FET 3 turns on and off for a fixed period, see Figure 3. The coil will generate a voltage spike with a higher amplitude than Vin. If the output voltage rises above the reference voltage, the cycle repeats but the FET 3 turn-on period is short enough to maintain the desired output voltage. FETs 3 and 4 turn on and off alternately, behaving like a typical synchronous boost regulator.

The duty cycle of FET 3 decreases until the minimum duty cycle of the converter in boost mode reaches 4%–6%.As an example, a simple boost converter was designed using the SLG47105 IC and Go Configure software, see Figure 4. It has the following parameters :

- Input voltage range (Vin) : 2.7 to 4.5 V
- Output voltage : 5 V
- Output current range : 0.5 - 1 A
- PWM frequency : 200 kHz
- Overcurrent/sort circuit protection : internal OCP

Calculated values:

- Min. Duty Cycle : 10%
- Max. Duty Cycle : 46%
- Min. Inductor size : 1.7 uH (2.2 uH, 4 A rated)
- Peak Inductor current : 3.7 A
- Filter Capacitor (C) : 100 uF (100 uF low ESR capacitor is recommended)

5.2 Go Configure Project

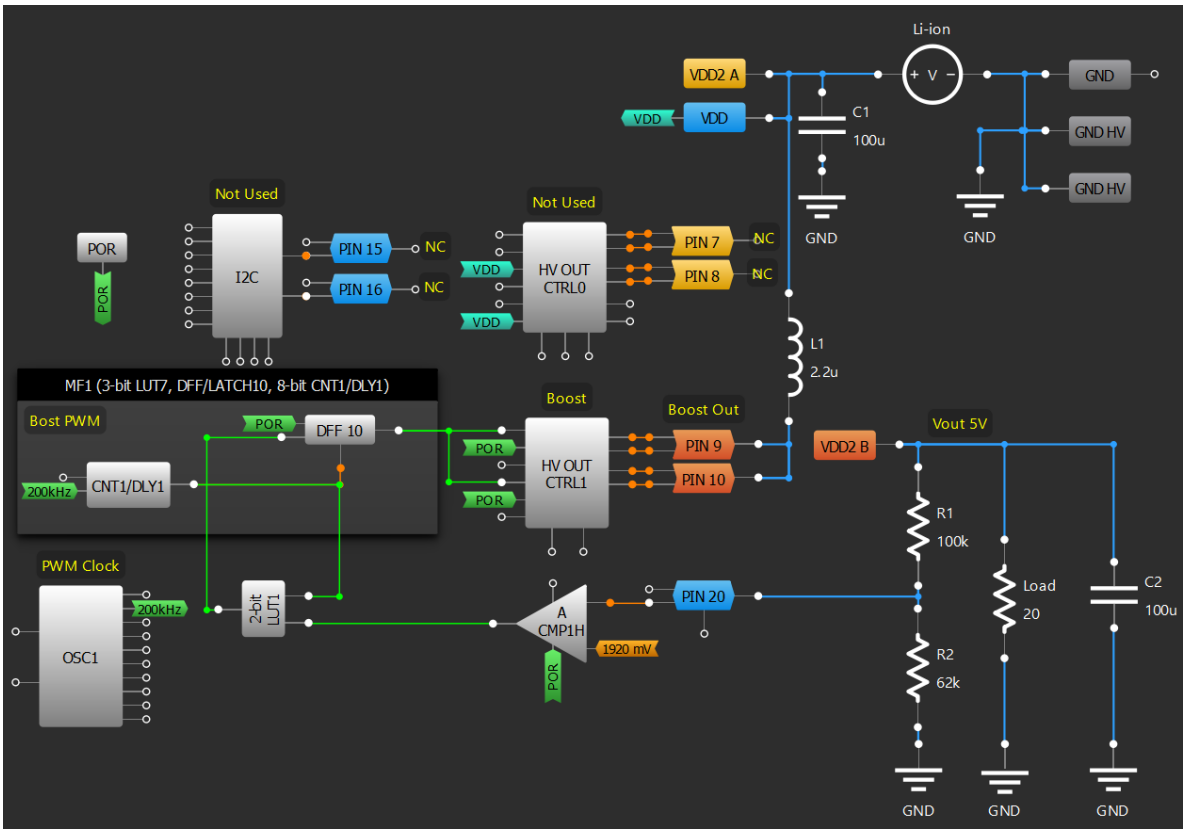

Figure 4: Boost DC-DC Converter Project

The regulator uses a 200 KHz clock like the previous one for the same reasons. The boost PWM logic is built on MF1 (CNT1/DLY1 and DFF 10) and 2-bit LUT1. The CNT1/DLY1 sets the minimum duty cycle of 10 %. It remains at a minimum until the feedback signal from the ACMP1H through 2-bit LUT1 extends it to the width when the voltage on the feedback loop is equal to the Vref maintaining a constant load voltage.

The HV OUT CTRL1 macrocell is configured as a fast slew rate half-bridge output. It has two half-bridge outputs which are connected in parallel to handle higher output current. Output pins (Pin 9 and Pin 10) are configured to «High and Low side on».

The ACMP1H in this design is used in a voltage feedback loop so the PWM could stabilize the output voltage. The output voltage is determined by the ACMP's Vref and the R1R2 voltage divider. In this case

$$Vref = \frac{Vout}{\frac{R1}{R2}+1} = \frac{5}{\frac{100k}{62k}+1} = 1.914\ (V)$$

The closest Vref value available in the SLG47105 is 1920 mV, which is close enough.

Unlike in the buck design, it is impossible using the HV OUT CTRL0 in the boost configuration. This is due to all internal logic circuits of both HV OUTs being powered from VDD 2A and it can be used as voltage input only. On the other hand, VDD 2B powers only two high-side transistors of Pins 9 and 10, thus it can be used as a voltage output.

6. Buck-Boost Converter

A buck-boost converter is a type of switched-mode power supply that combines the principles of the buck converter and the boost converter in a single circuit.

There are many applications, however, such as battery-powered systems, where the input voltage can vary widely, starting at full charge and gradually decreasing as the battery charge is used up. At full charge, where the battery voltage may be higher than needed by the circuit being powered, a buck regulator would be ideal to keep the supply voltage steady. However as the charge diminishes the input voltage falls below the level required by the circuit, and either the battery must be discarded or re-charged. At this point, the ideal alternative would be the boost regulator.

By combining these two regulators designs it is possible to have a regulator circuit that can cope with a wide range of input voltages both higher and lower than that needed by the circuit. Fortunately, both buck and boost converters use very similar components; they just need to be re-arranged, depending on the level of the input voltage.

In Figure 5 the common components of the buck and boost circuits are combined. A control unit is added, which senses the level of input voltage, then selects the appropriate circuit action.

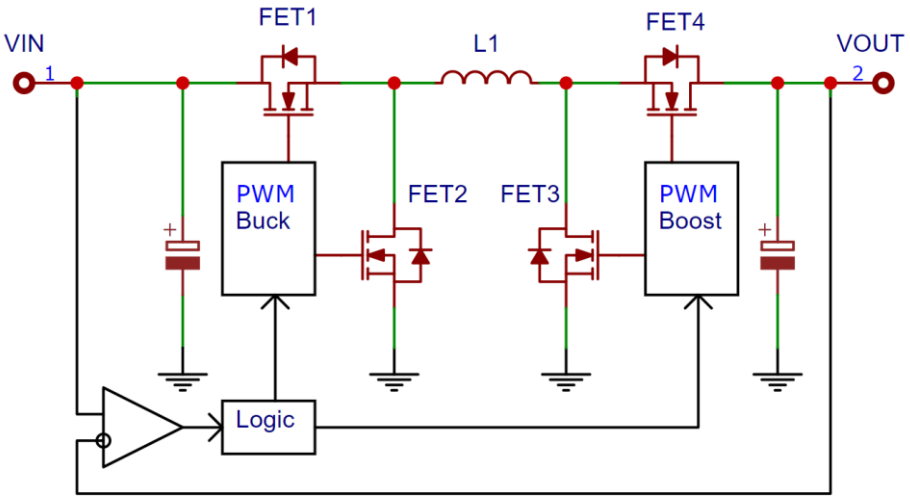

Figure 5: Buck and Boost Converters Combined Circuit

This topology offers a simple solution with an approach that requires neither cumbersome magnetics nor additional control loops. The design takes the form of a synchronous buck or boost, depending on the input voltage. Transitions between modes depend on the duty cycle (Figure 6) and are quick and automatic.

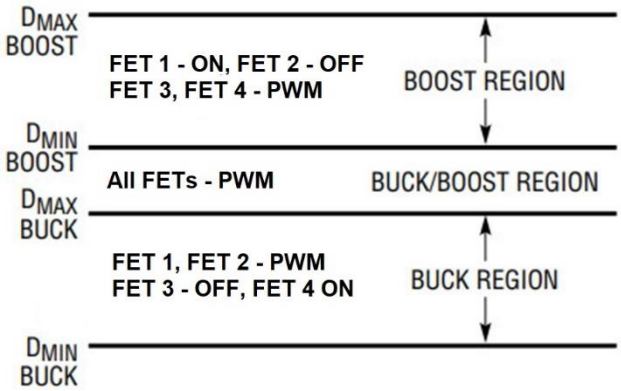

Figure 6: Transitions Between Modes

6.1 Example #1. Powering LED from Single Li-ion Cell

As an example, a simple buck-boost converter was designed using the SLG47105 IC and Go Configure software, see Figure 7 and Figure 9. Its purpose is to drive a 3W LED from a single li-ion cell. It has the following parameters

- Input voltage range (Vin) 2.7 to 4.2 V
- Output voltage 2.9 – 3.6 V (depending on the LED type)
- Output current range 650 mA (regulated)
- PWM frequency 200 kHz
- Overcurrent/sort circuit protection – internal OCP

Calculated values for buck:

- Rated Peak Withstand Current (Ipk) – 1.3 A
- Inductance (Lmin) – 2 uH
- Filter Capacitor (C) – 22 uF

Calculated values for boost:

- Min. Duty Cycle – 10%
- Max. Duty Cycle – 25%
- Min. Inductor size – 1.9 uH
- Peak Inductor current – 1.73 A
- Filter Capacitor (C) – 63 uF

Selected value of the inductance – 3.3 uH and the filter capacitor – 100 uF. For a schematic diagram see Figure 7.

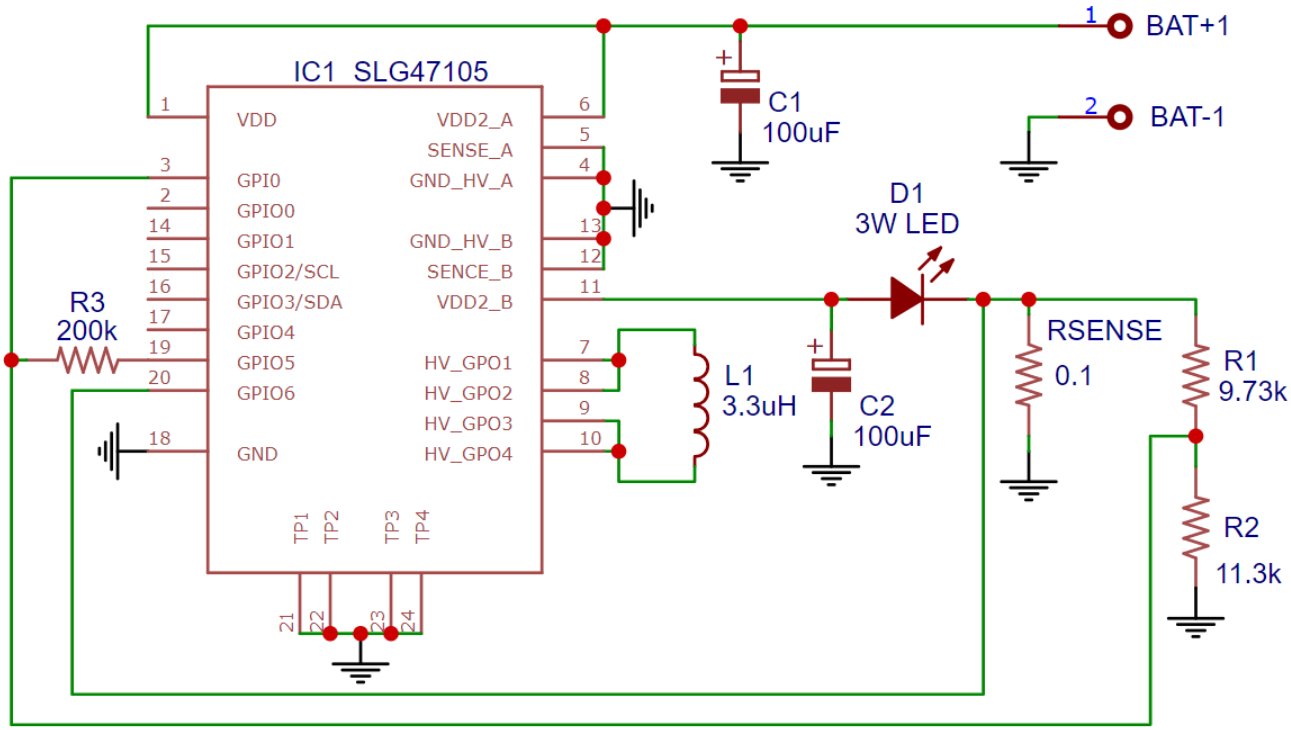

Figure 7: Buck-Boost Schematic Diagram of Example #1

6.1.1. Theory of Operation

Buck Mode

When the input is well above the output (buck mode), the converter behaves as in section 4. Buck Converter.

Boost Mode

When the input is well below the output (boost mode). the converter behaves as in section 5 Boost Converter.

Buck-Boost Mode

Ideally, the buck-boost mode is activated when the boost duty cycle passes its minimum and before buck mode starts. In practice, that causes a slight output voltage instability when transitioning from mode to mode. So, to avoid that, in this design, the buck-boost mode has a bit wider active area at the cost of lower efficiency.

Figure 8 shows all modes for all four switches (FETs).

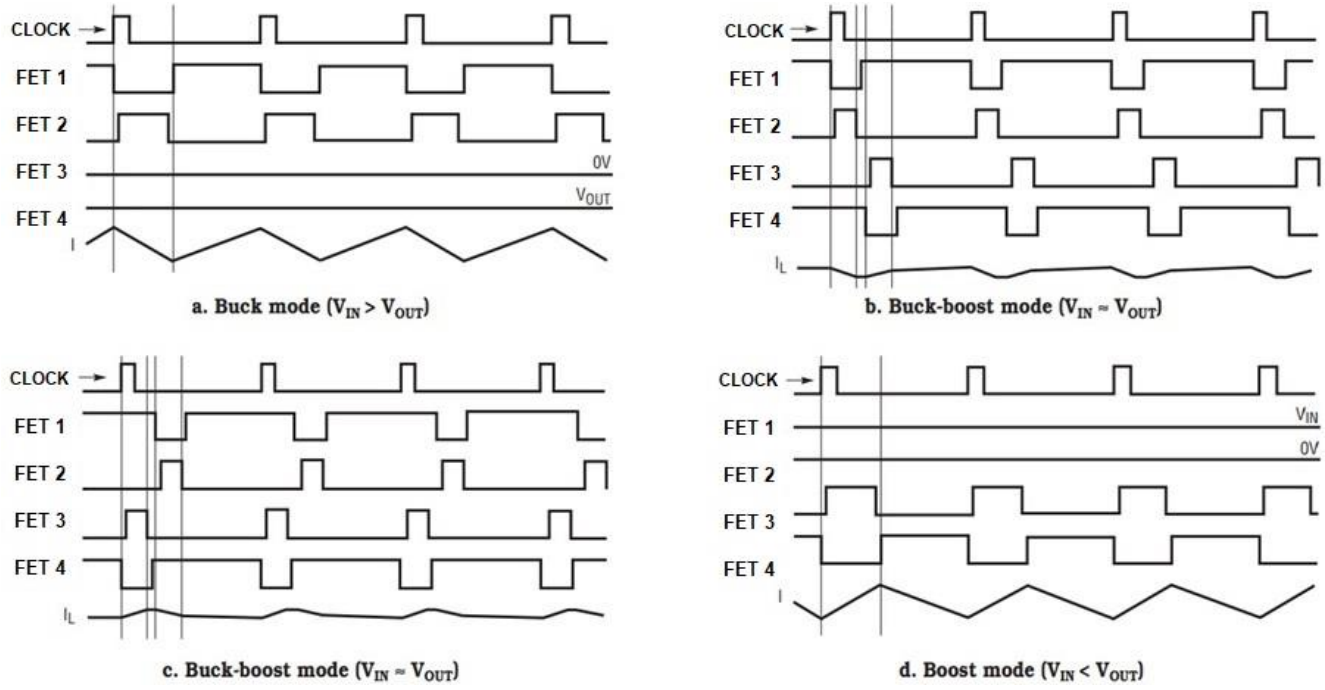

Figure 8: Power Switch Mode in Various Regions of Operation

6.1.2. Go Configure Project

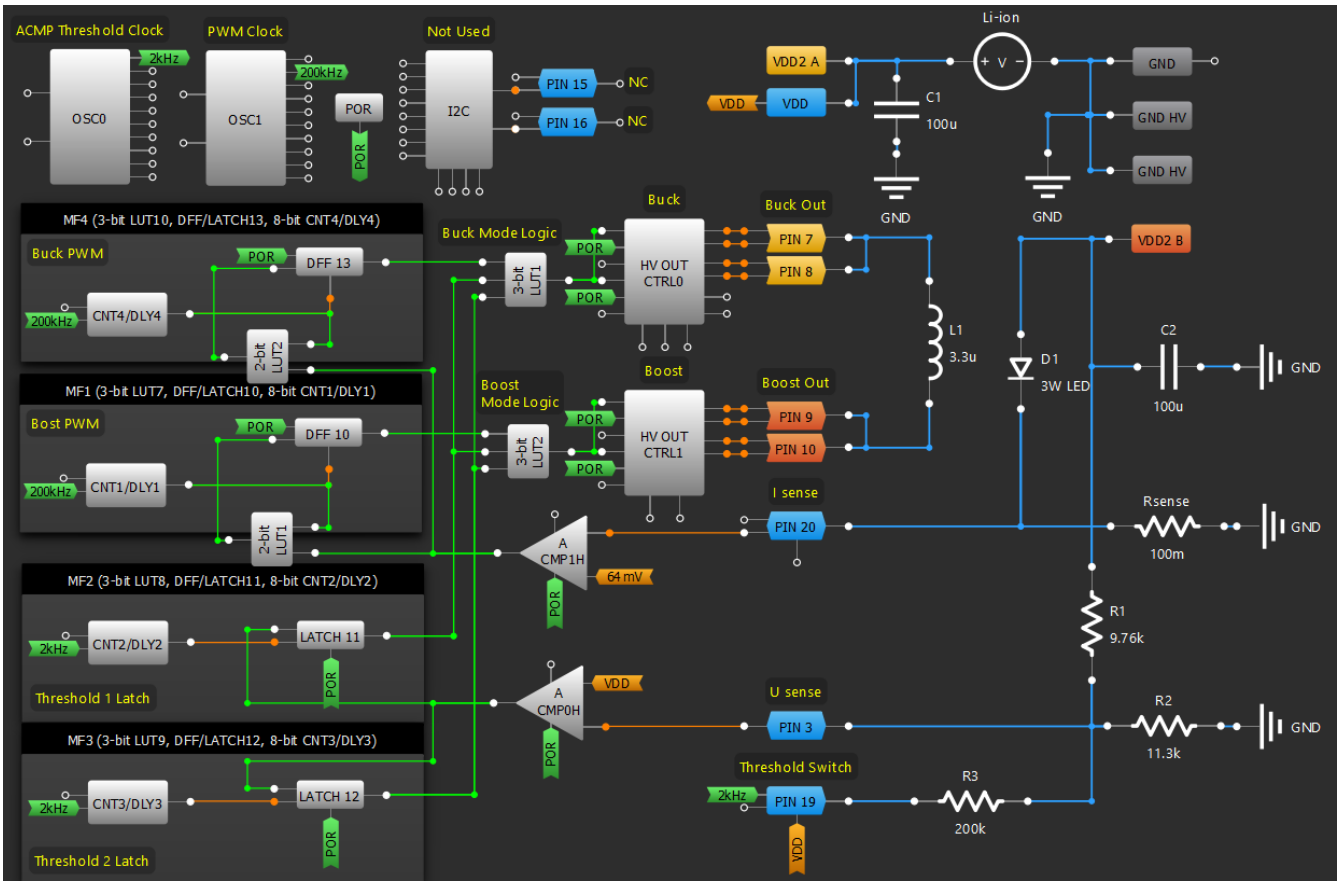

Figure 9: Example #1. Go Configure Project

Both buck and boost regulators within this project are built using the same principals and macrocells as in previous buck and boost converters.

The buck PWM logic is built on MF4 (CNT4/DLY4 and DFF 13) and 2-bit LUT2. The CNT4/DLY4 sets the maximum duty cycle of 96.6 %. It remains at maximum until the feedback signal from the ACMP1H through 2-bit LUT2 cuts it. Thus regulating the output voltage on the current sense resistor, therefore, regulating the load current.

The boost PWM logic is built on MF1 (CNT1/DLY1 and DFF 10) and 2-bit LUT1. The CNT1/DLY1 sets the minimum duty cycle of 10 %. It remains at a minimum until the feedback signal from the ACMP1H through 2-bit LUT1 extends it to the width when the voltage on the current sense resistor is equal to the Vref maintaining a constant load current.

Both HV OUT macrocells are configured as fast slew rate half-bridge output. Each macrocell has two half-bridge outputs which are connected in parallel to handle higher output current. All four HV pins (Pin 7 to Pin 9) are configured to «High and Low side on».

The ACMP1H in this design is used in a voltage feedback loop so both PWMs could stabilize the current sensor voltage, thus maintaining constant current on the load. The output current is determined by the ACMP's Vref and the current sensor resistance. For the particular 3W LED used in this project, the output current should be around 700 mA at a voltage of about 3.6 V. If the current sense resistor value is 0.1 Ω, than

$$\boldsymbol{Vref = 700mA \times 0.1\,\Omega = 700\,mV}$$

The closest Vref value available in the SLG47105 is 64 mV, which is close enough. The output current can be adjusted by changing the current sense resistor value if needed.

The ACMP0H serves as a cross-voltage detector. Its positive input is connected internally to the VDD (VDD and VDDA are connected together) through the ½ internal voltage divider. The negative input is connected to the output also through the voltage divider R1R2 but this one is modified by adding one more resistor R3 which periodically (with 2 kHz frequency) is being connected in parallel to the R2 through open drain PIN 19 making two thresholds for ACMP0H. At the same time, the clock frequency of 2 kHz (from OSC0) goes to two edge detectors within MF2 and MF3 (rising and falling respectively) which together with latches 11 and 12 latch ACMP's output for each threshold. This circuit (ACMP0H, OSC0, PIN 19, MF2, and MF3) allows detecting when the input voltage is close to the output voltage with two thresholds: Vin < Vout and Vin > Vout creating a window for the buck-boost mode.

3-bit LUTs 1 and 2 make a logic that based on the signals from the previously described circuit turns on and off the respective mode: buck, boost, or buck-boost.

6.1.3. Buck-Boost Converter Performance

See the oscilloscope screenshots, where yellow – buck Output (Pins 7 and 8), blue – boost Output (Pins 9 and 10), and purple – output voltage (VDD2 B).

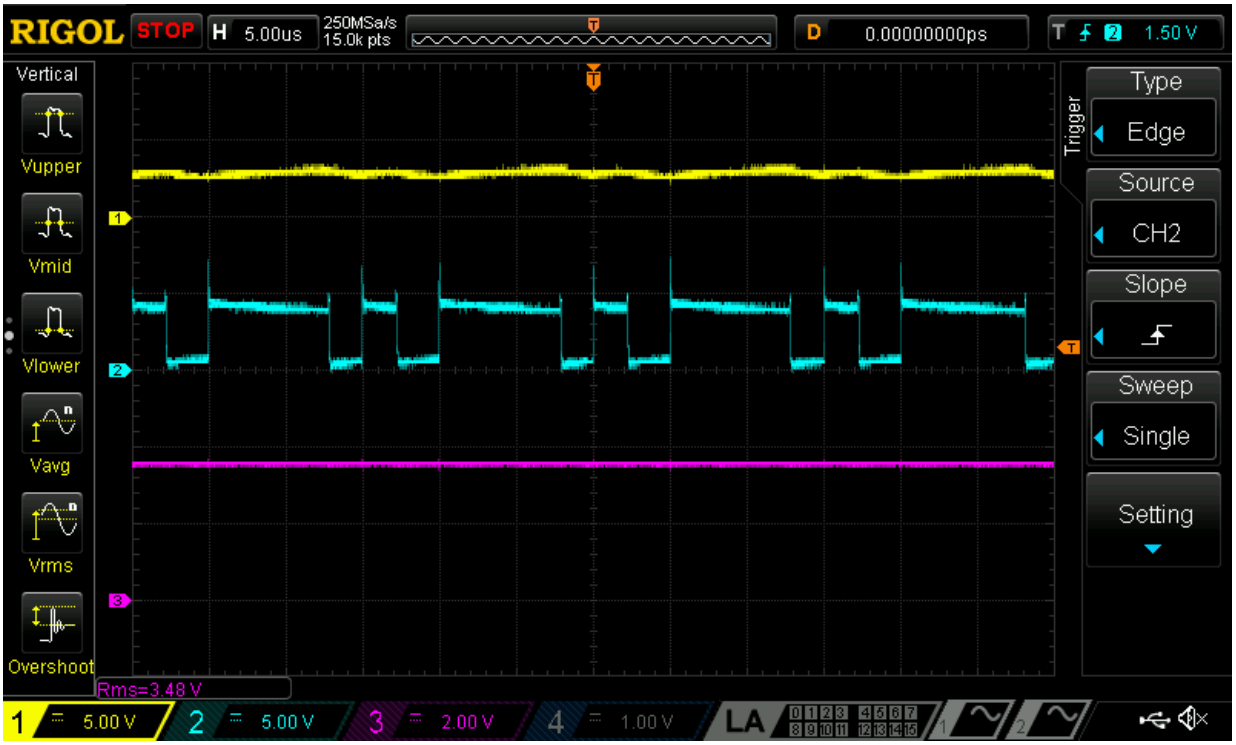

Figure 10: Input Voltage VDD = VDD2 A = 2.7 V

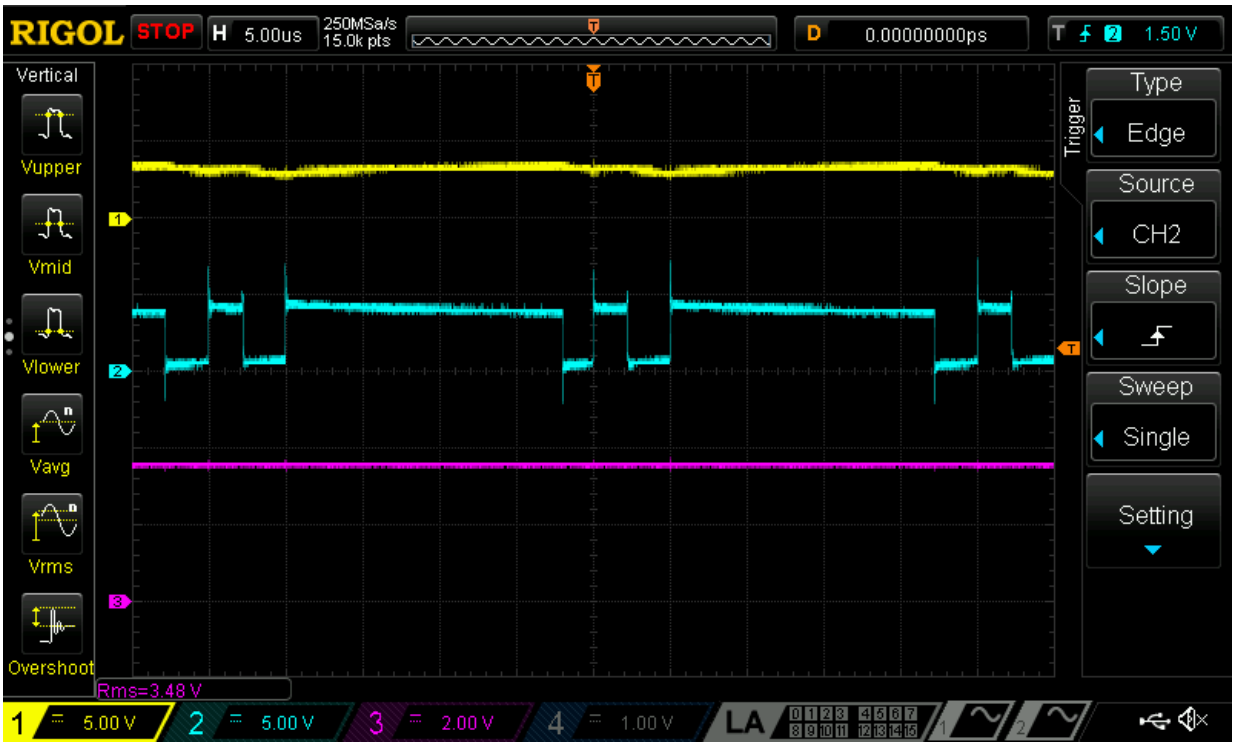

Figure 11: Input Voltage VDD = VDD2 A = 3.0 V

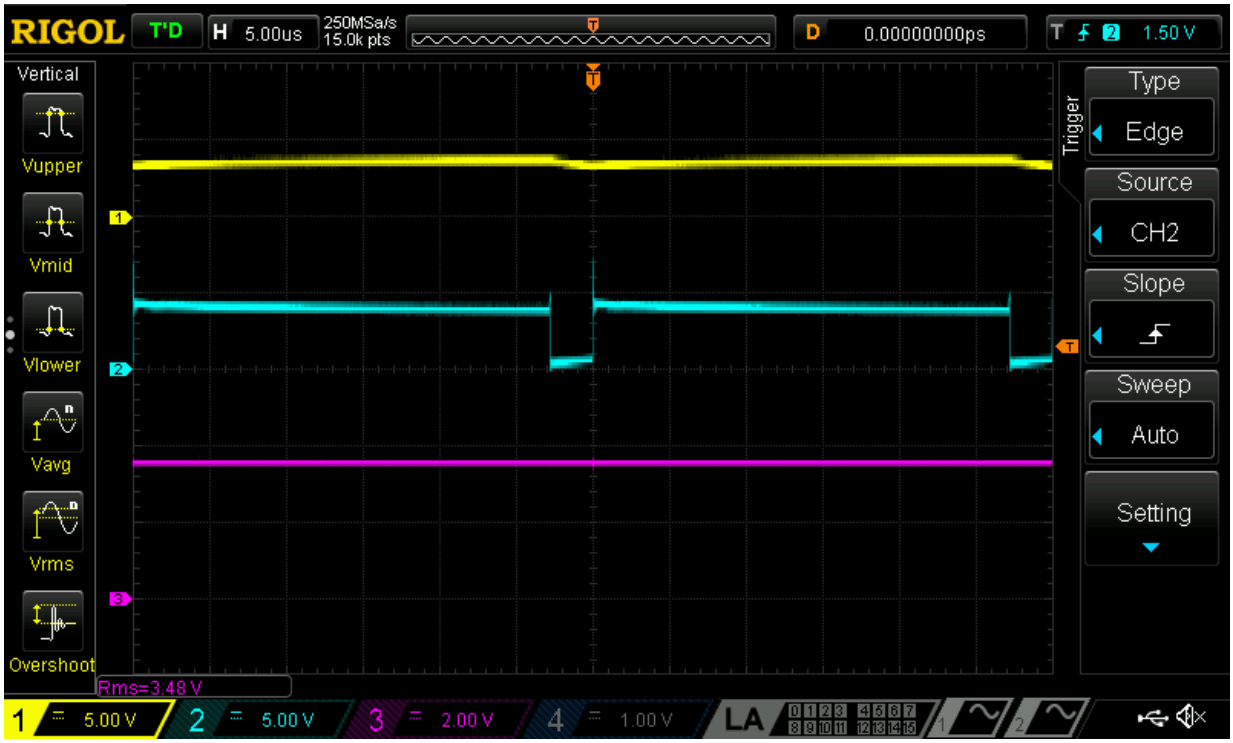

Figure 12: Input Voltage VDD = VDD2 A = 3.3 V

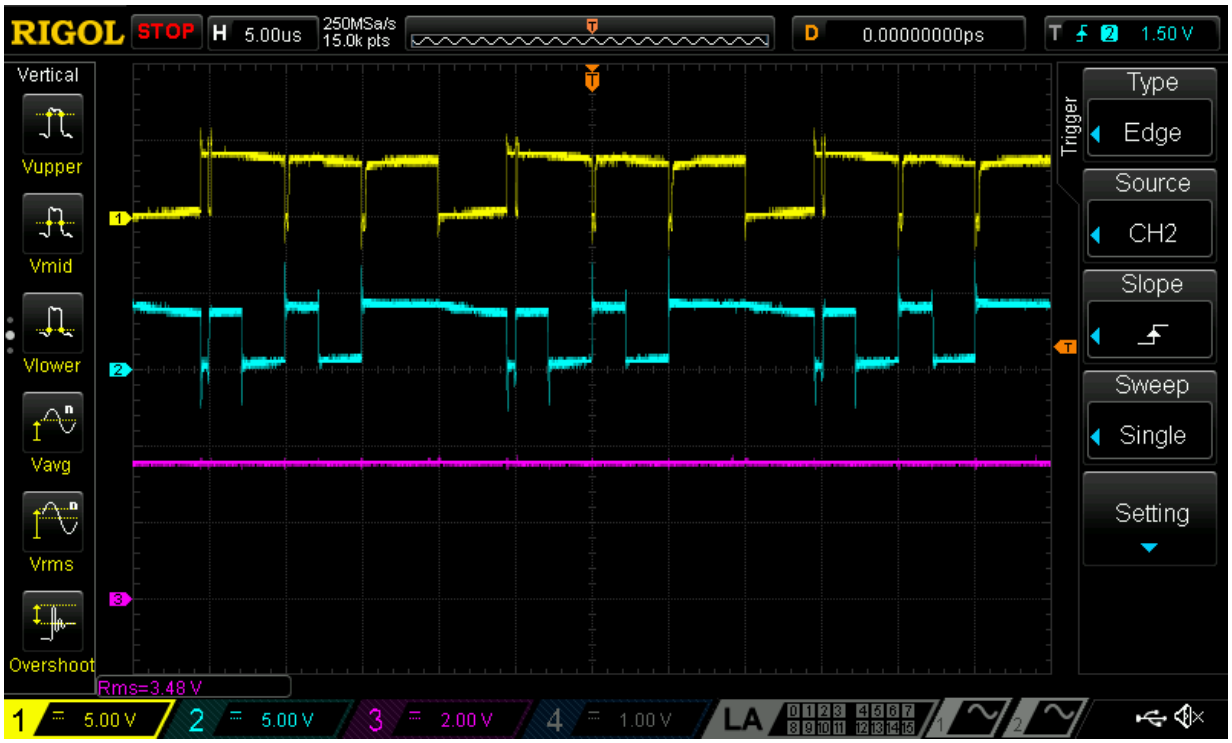

Figure 13: Input Voltage VDD = VDD2 A = 3.6 V

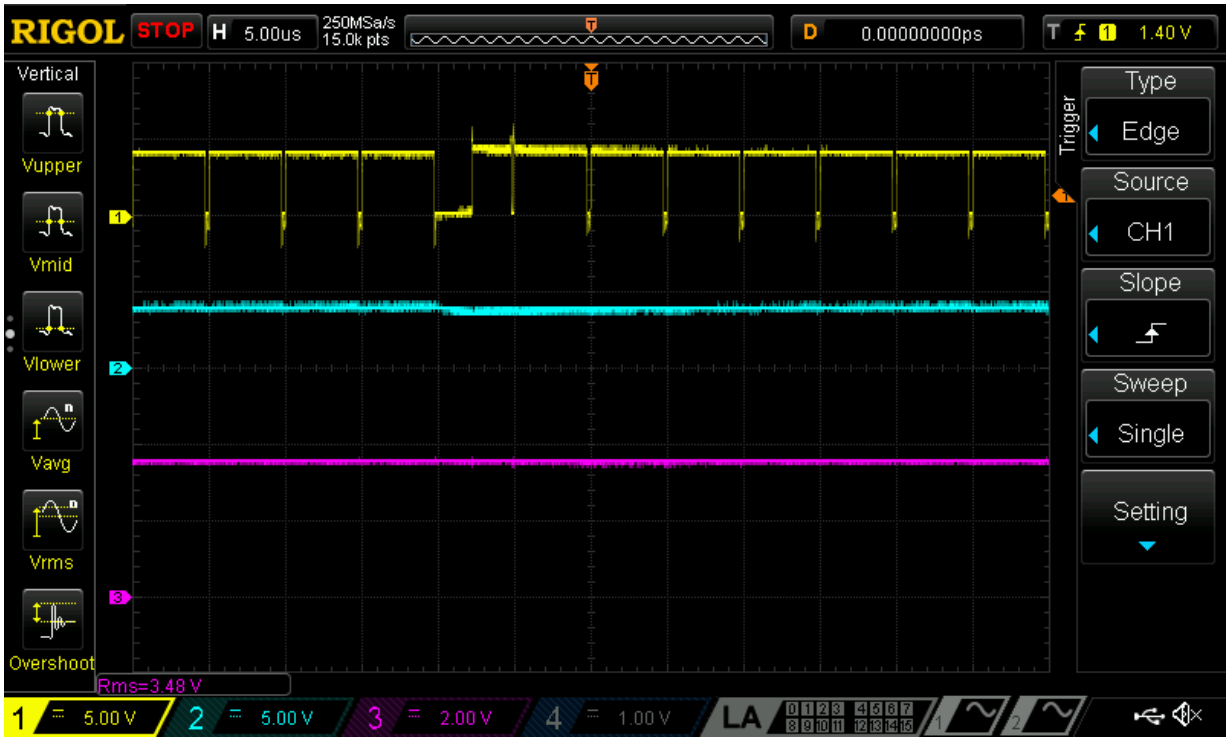

Figure 14: Input Voltage VDD = VDD2 A = 3.9 V

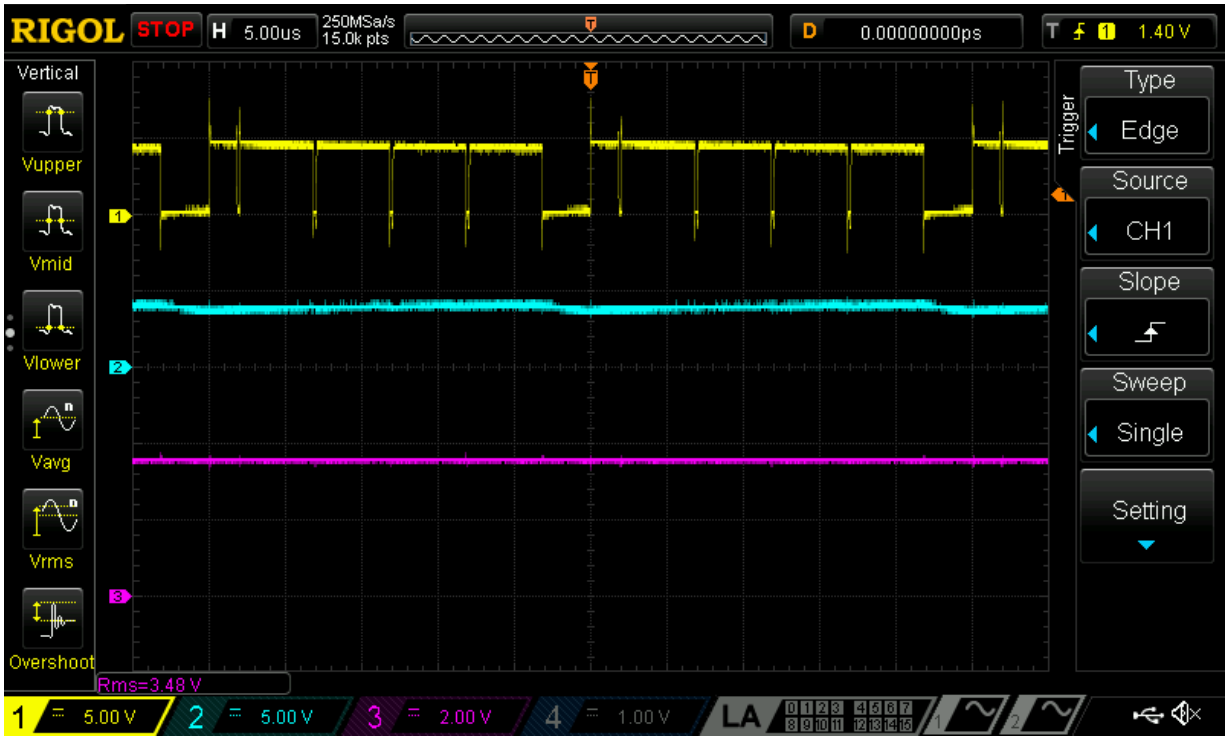

Figure 15: Input Voltage VDD = VDD2 A = 4.2 V

See also the graphs showing the device performance in Figure 16, Figure 17, Figure 18.

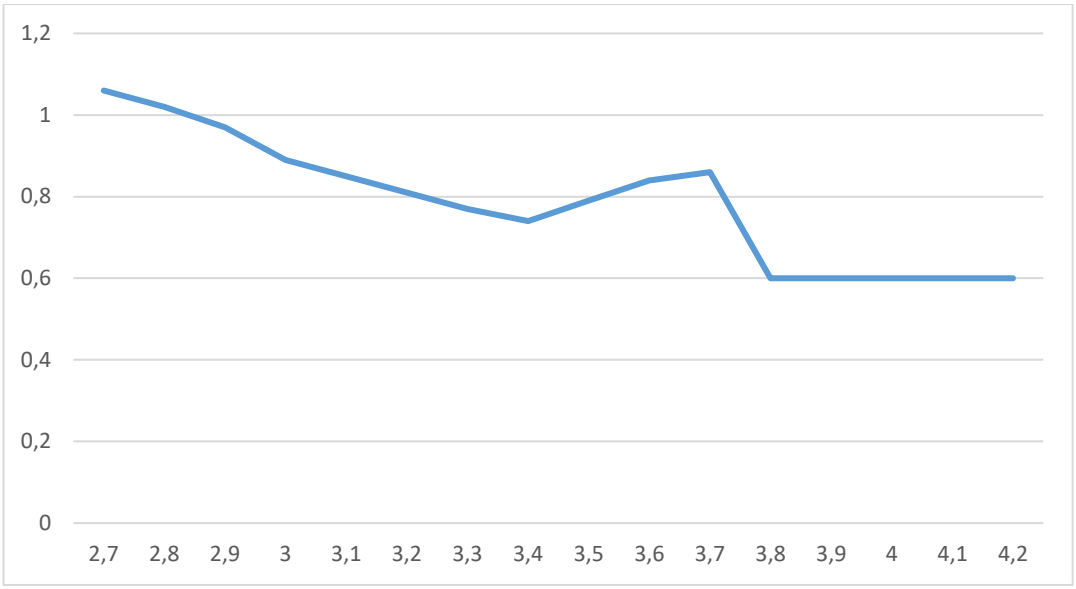

Figure 16: Input Current vs. Input Voltage

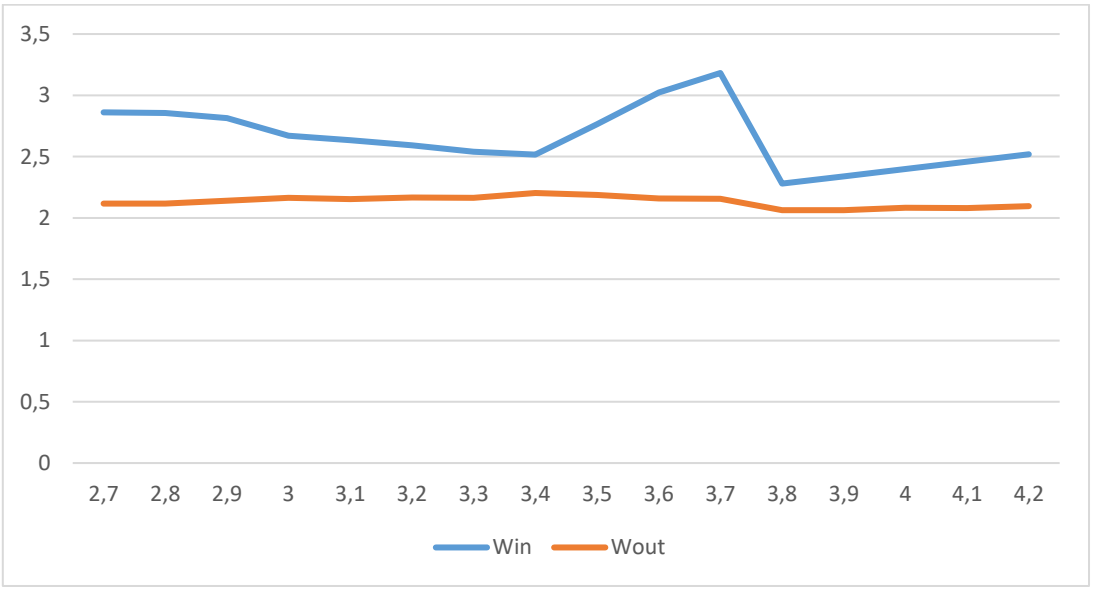

Figure 17: Input and Output Power vs. Input Voltage

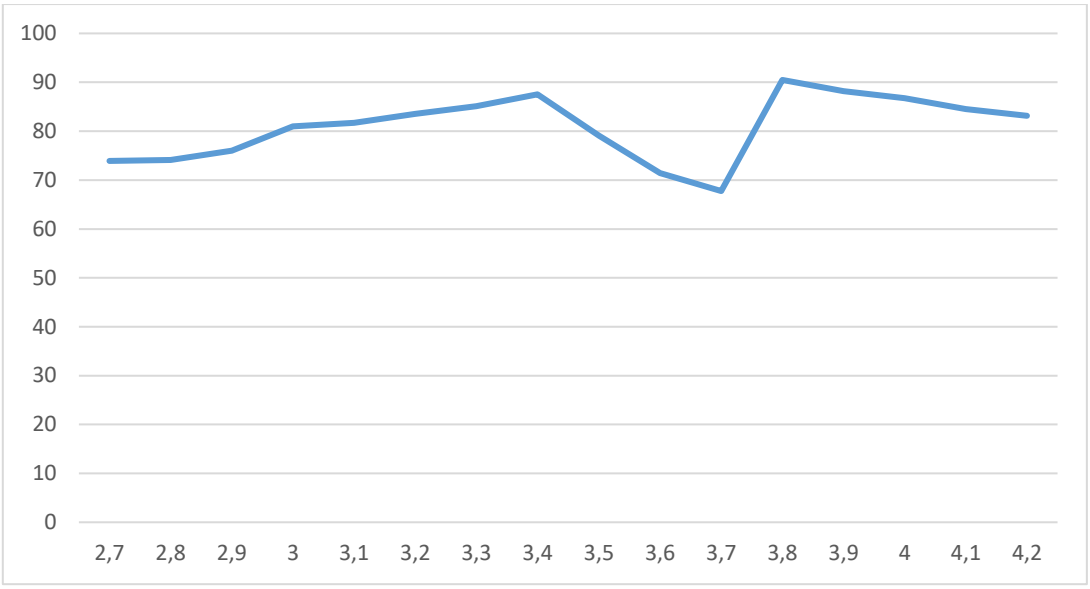

Figure 18: Efficiency vs. Input Voltage

6.2 Example #2. 3.3 V Output from 2.7 V to 5.0 V Input

This buck-boost converter is very similar to the previous one, but uses a non-standard approach to switch between modes. When Vin approaches Vout (taking into account internal switches' voltage drop) instead of engaging both buck and boost modes, this converter does exactly the opposite. Both modes are being disabled allowing Vin to go through the output pins straight to the load uninterrupted by any PWM. This allows for eliminating the efficiency gap at the cost of a slight Vout wobble in the transition moment.

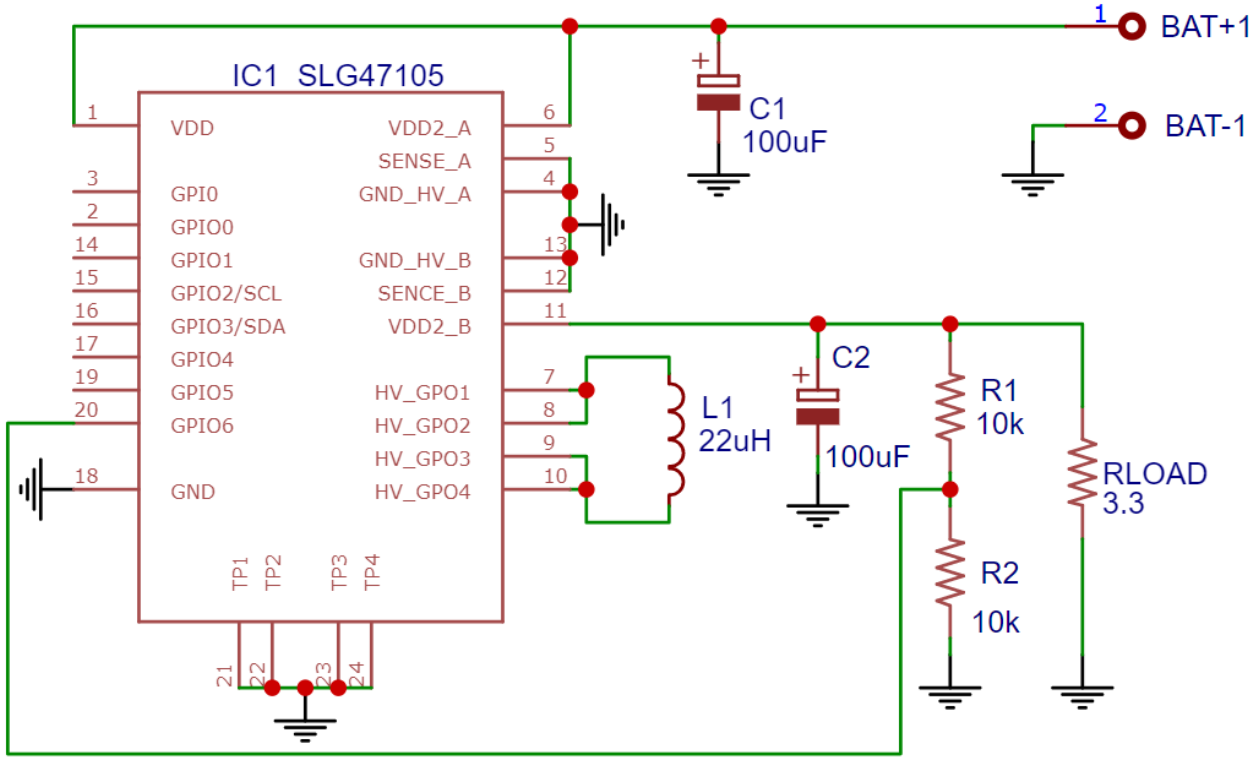

Figure 19: Buck-Boost Schematic Diagram of Example #2

The goal is to get a stable 3.3V 1A supply from the 2.7 V to 5.0 V input voltage range. It has the following parameters

- Input voltage range (Vin) : 2.7 to 5 V
- Output voltage (Vout) : 3.3 V (regulated)
- Output current range : 1 A
- PWM frequency : 200 kHz
- Overcurrent/sort circuit protection – internal OCP

6.2.1. Theory of Operation

The buck and boost modes work the same way as described in the previous example. But there is no buck-boost mode. As mentioned in section 6.2, instead of engaging two modes simultaneously, the input voltage is routed through the internal switches directly to the load, see Figure 20.

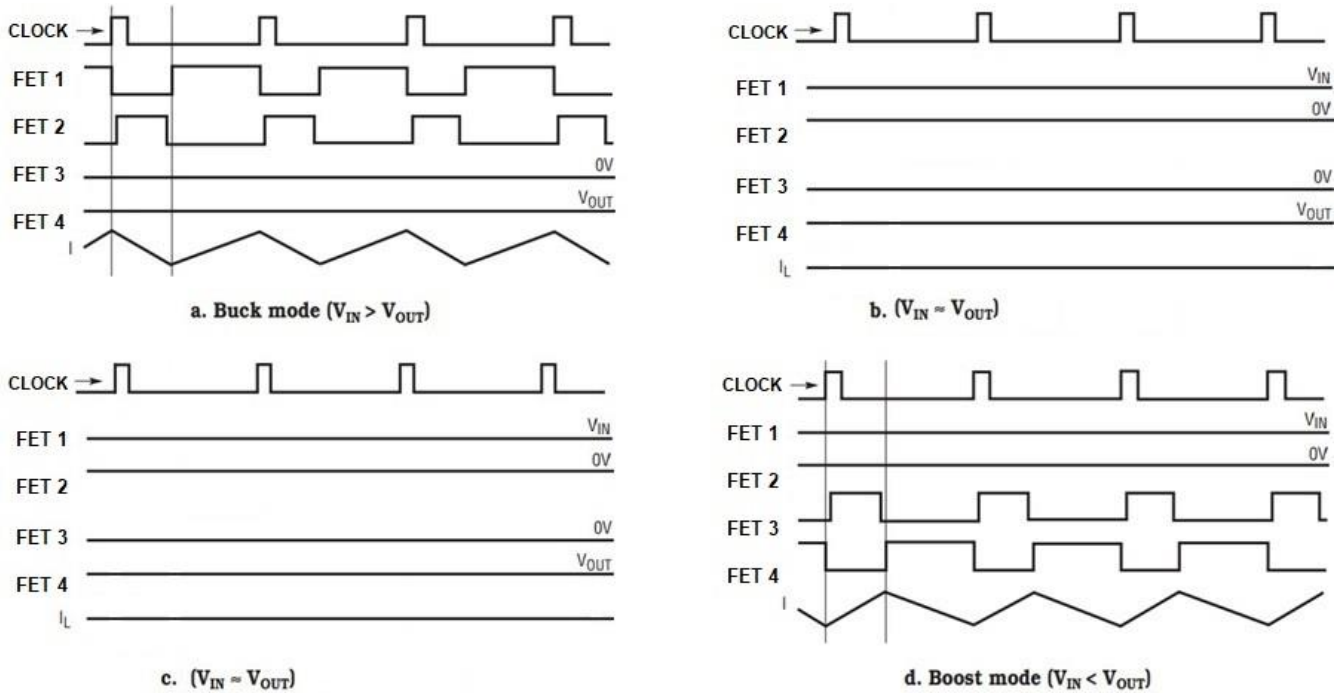

Figure 20: Power Switch Mode in Various Regions of Operation

6.2.2. Go Configure Project

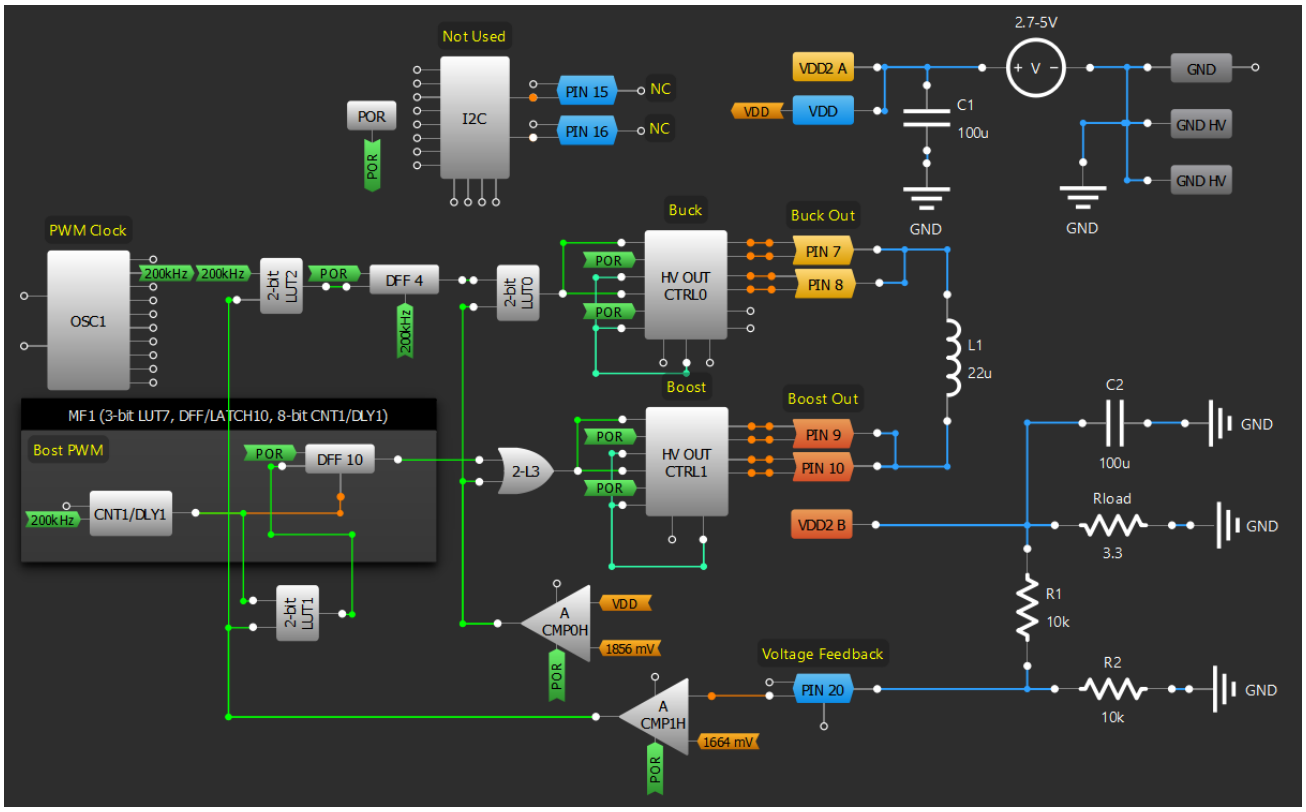

Figure 21: Example #2. Go Configure Project

Both buck and boost regulators within this project are built using the same principles as in the previous buck-boost converter.

The buck PWM logic is built on 2-bit LUT2 and DFF 4. The maximum duty cycle of 99 % is achieved by omitting the delay and using the clock signal directly from the flexible divider. It remains at maximum until the feedback signal from the ACMP1H through 2-bit LUT2 cuts it. Thus regulating the output voltage.

The boost PWM logic is built on MF1 (CNT1/DLY1 and DFF 10) and 2-bit LUT1. The CNT1/DLY1 sets the minimum duty cycle of 25 %. It remains at a minimum until the feedback signal from the ACMP1H through 2-bit LUT1 extends it to the width when the output voltage is twice the Vref maintaining a constant Vout.

Both HV OUT macrocells are configured as fast slew rate half-bridge output. Each macrocell has two half-bridge outputs which are connected in parallel to handle higher output current. All four HV pins (Pin 7 to Pin 9) are configured to «High and Low side on».

The ACMP1H in this design is used in a voltage feedback loop so both PWMs could stabilize the output voltage. The output voltage is determined by the ACMP's Vref and the R1R2 voltage divider. In this case

$$\boldsymbol{Vout = Vref \times \left(\frac{R1}{R2} + 1\right) = 1664\,mV \times \left(\frac{10k}{10k} + 1\right) = 3.328\,V}$$

The ACMP0H serves as a cross-voltage detector. Its positive input is connected internally to the VDD (VDD and VDDA are connected together) through the ½ internal voltage divider which is compared to the internal Vref of 1856 mV with an internal 32 mV hysteresis. This is chosen higher to compensate for the internal transistors' voltage drop under the load. It should be noted that the value of 1856 mV is selected for 1 A load. If the output current is

different, this value should be adjusted. But if the load is planned to be variable, in this case instead of an internal Vref the external voltage divider (with a ½ ratio) should be used. It must be connected between Vout, Pin 3 (ACMP0H IN-), and GND. Also, to avoid ACMP oscillation, external hysteresis must be considered (internal 32 mV hysteresis in this case will be unavailable). To do that, the ACMP0H output must be connected to any available output pin, and from that pin, a 200 kΩ resistor should be connected to Pin 3 (ACMP0H IN-).

6.2.3. Buck-Boost Converter Performance

See the oscilloscope screenshots, where yellow – buck Output (Pins 7 and 8), blue – boost Output (Pins 9 and 10), and purple – output voltage (VDD2 B).

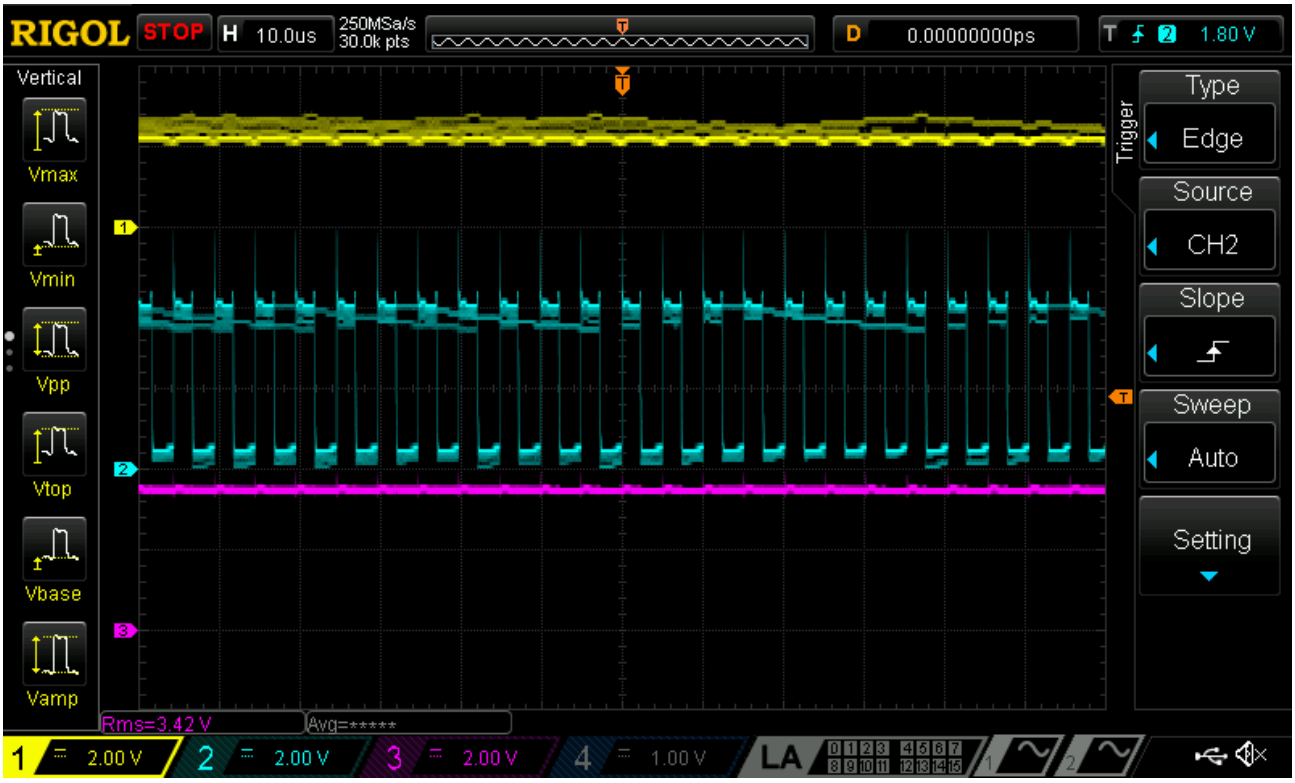

Figure 22: Input Voltage VDD = VDD2 A = 2.7 V

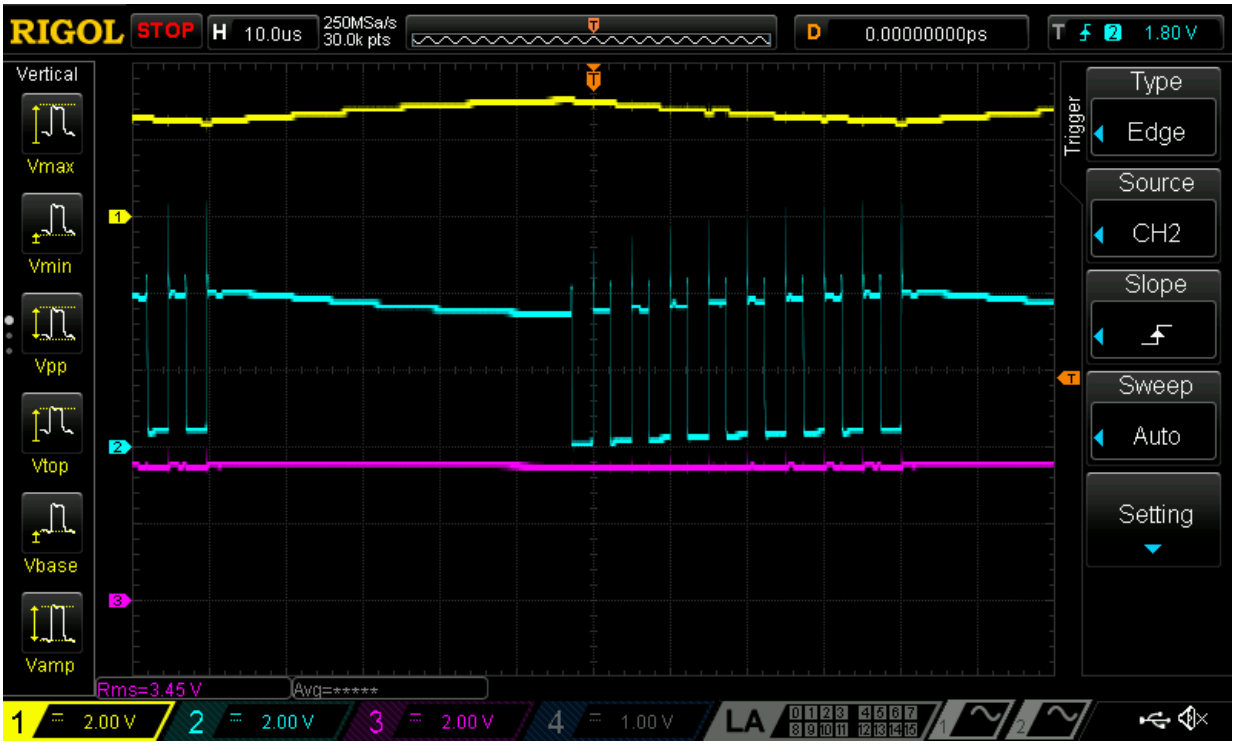

Figure 23: Input Voltage VDD = VDD2 A = 3.0 V

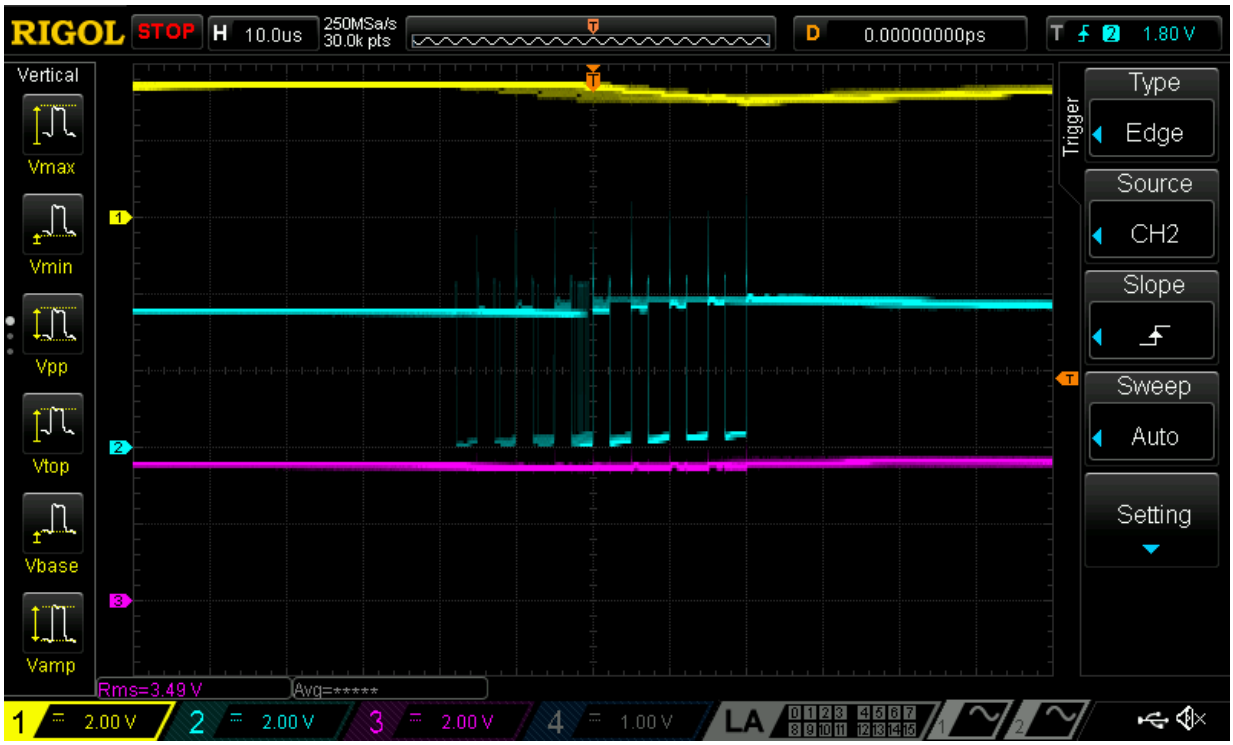

Figure 24: Input Voltage VDD = VDD2 A = 3.5 V

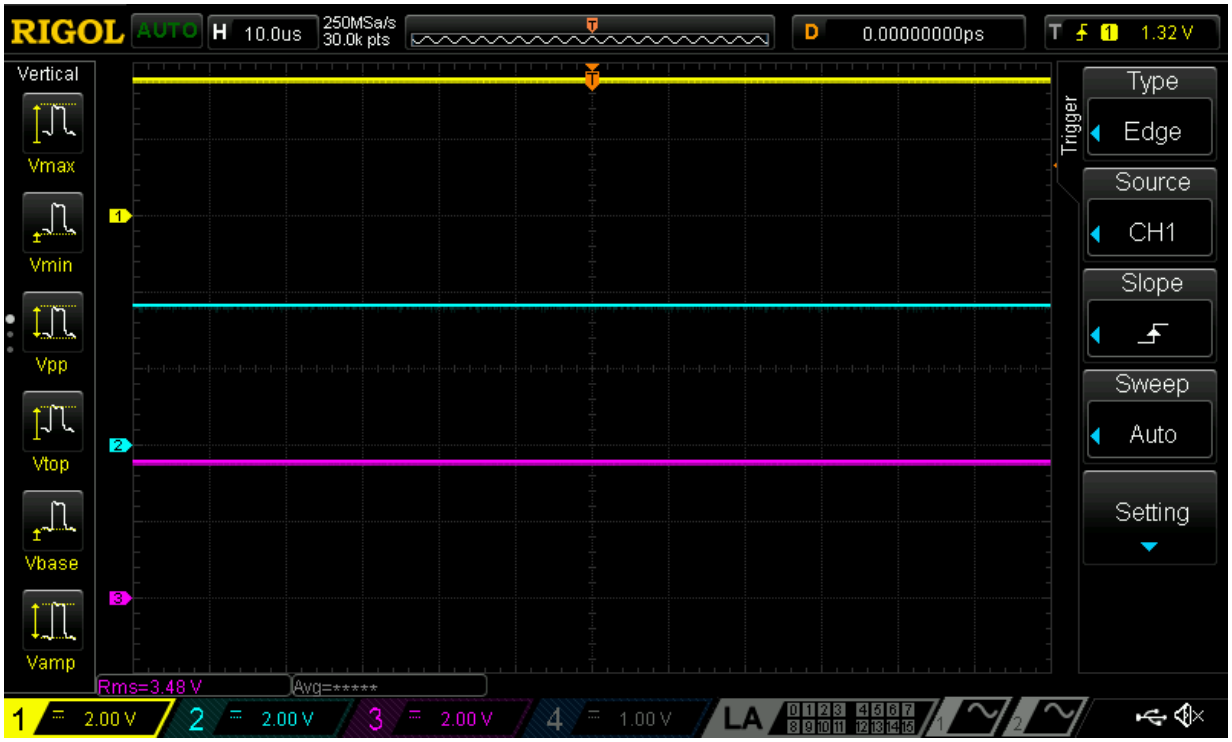

Figure 25: Input Voltage VDD = VDD2 A = 3.7 V

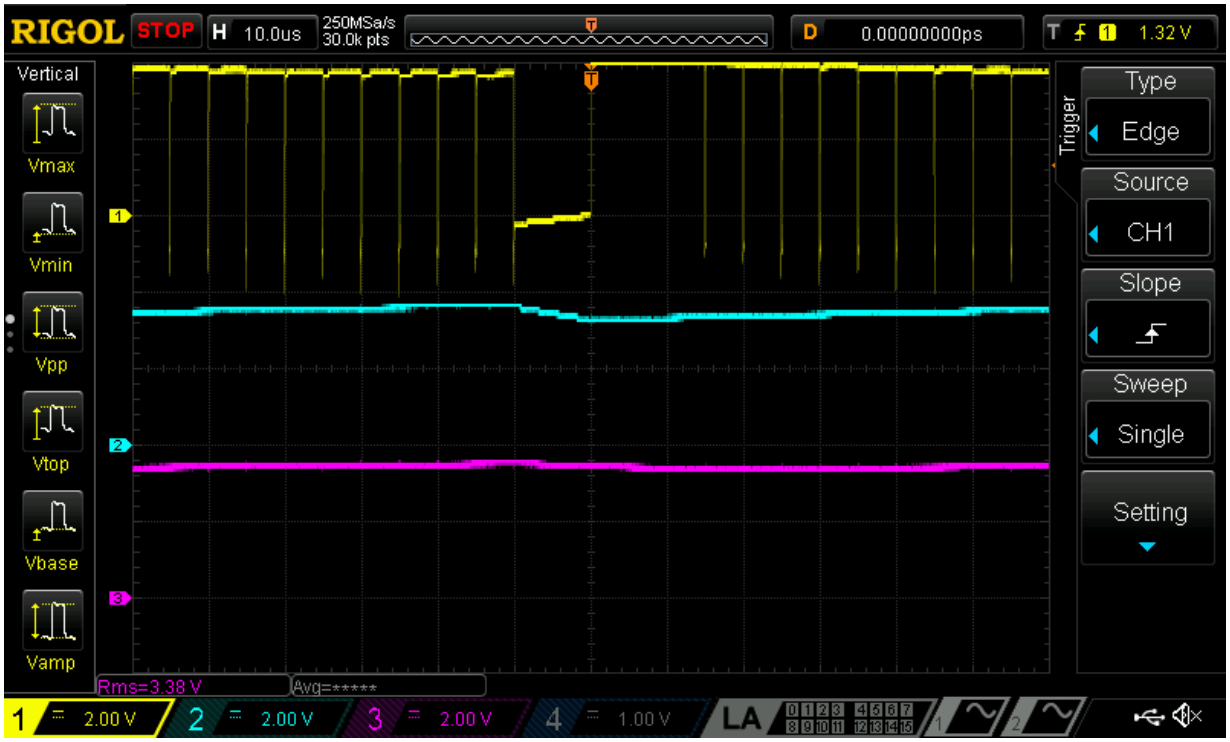

Figure 26: Input Voltage VDD = VDD2 A = 4.0 V

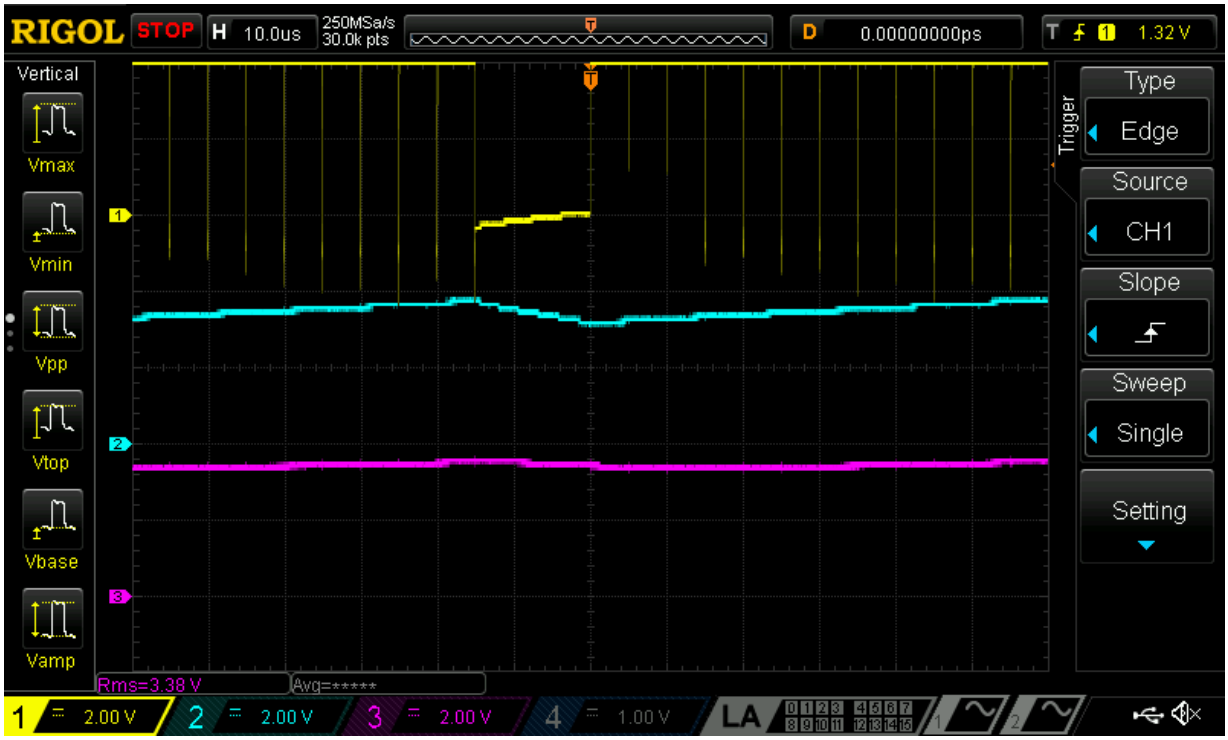

Figure 27: Input Voltage VDD = VDD2 A = 4.5 V

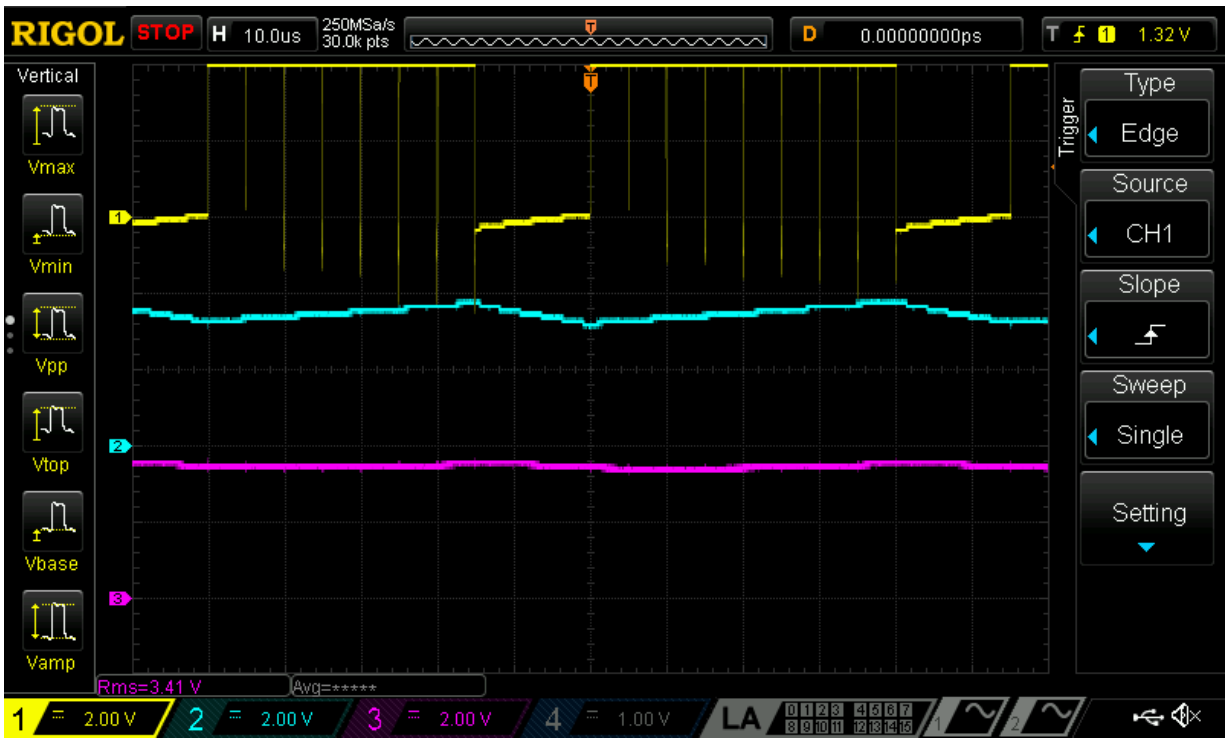

Figure 28: Input Voltage VDD = VDD2 A = 5.0 V

See also the graphs showing the device performance in Figure 29, Figure 30, Figure 31.

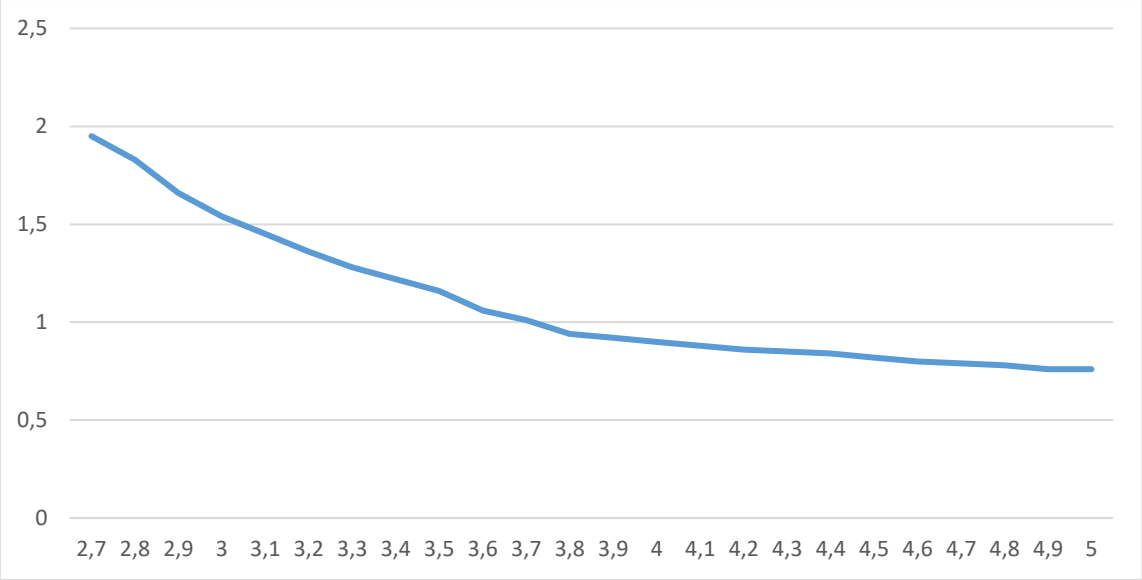

Figure 29: Input Current vs. Input Voltage

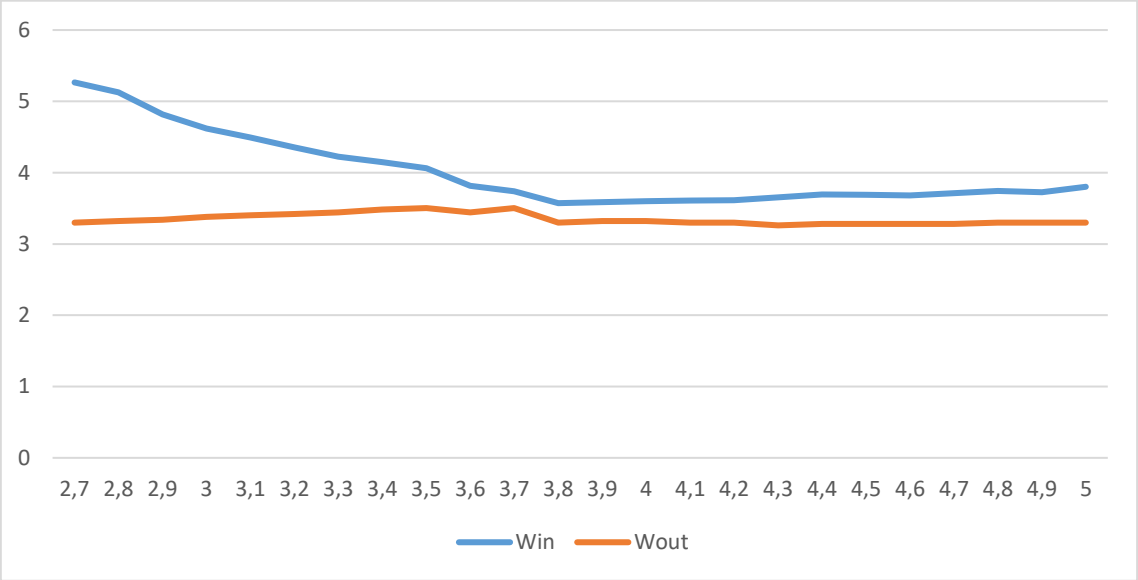

Figure 30: Input and Output Power vs. Input Voltage

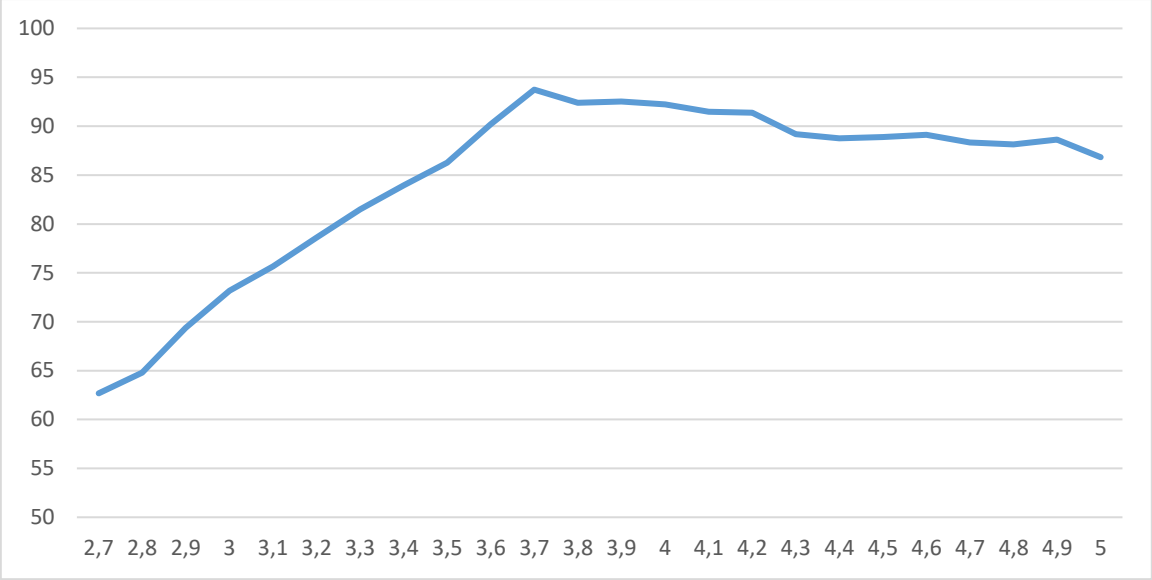

Figure 31: Efficiency vs. Input Voltage

7. Conclusions

As shown in this application note, designing and building buck, boost, and buck-boost converters using the SLG47105 chip with minimum external components is quite easy. The amount of unused macrocells leaves plenty of room for modifications and adding new features for proposed designs. For example, a soft start where a PWM period slowly increases from 0 to the required value reduces a peak start-up current, programmable overcurrent protection, multiple output voltages, etc. Also, the HV OUT pins are suitable for driving external MOSFETs, which allows for building a very high-power DC-DC converter.

8. Revision History

Revision	Date	Description
1.00	Sep14, 2023	Initial release

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