Voltage Regulator with Encoder Control

SLG47003

This application note describes how to use the SLG47003 to implement a voltage regulator.

The SLG47003 is a programmable mixed signal matrix that also includes OPAMPs and an analog switch. In addition, this IC contains a large numberof different macrocells which make it possible to easily design an appropriate circuit for any given task.

The application note comes complete with a design file that can be found in the Reference section.

Contents

1. Terms and Definitions

ACMP	Analog Comparator
CNT/DLY	Counter-Delay
DFF	D Flip-flop
ESR	Equivalent Series Resistance
GPO	General Purpose Output
IC	Integrated Circuit
I/O	Input / Output
LED	Light Emitting Diode
LUT	Look-up Table
MF	Multi-function Macrocell
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
OSC	Oscillator
PCB	Printed Circuit Board

2. References

For related documents and software, please visit:

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Download our free GreenPAK Designer software [1] to open the .aap files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics

[2], AN-CM-383 Voltage regulator with encoder control, Design file, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

3. Introduction

Linear regulators are simple voltage regulator circuits commonly used in many different electronic applications

Figure 1 shows a typical linear regulator based on an Op-Amp and P-FET.

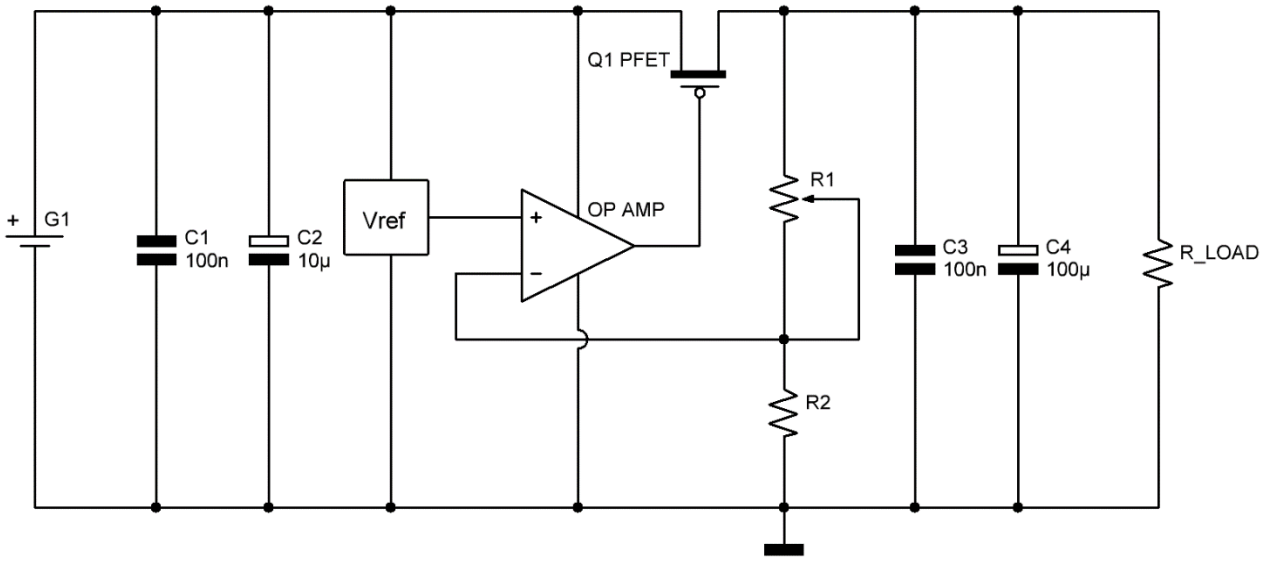


Figure 1. Typical linear regulator based on the OP AMP and P-FET

Linear regulators use a closed feedback loop to bias a pass element to maintain a constant voltage across its output terminals. In Figure 1, the op-amp drives the gate of Q1 to ensure that the voltage at its inverted input will be equal to the voltage reference at its non-inverted input.

The op-amp in this circuit has a small load and minimal capacitive loading. Consequently, it can respond to changes in load very quickly.

Two things can be observed from this schematic:

1. Linear regulators are step-down converters, meaning that the output voltage will always be less than the input voltage. In fact, there is a minimum voltage difference between V_{IN} and V_{OUT} that will allow the linear regulator to work. This value is called the drop-out voltage. If the $V_{OUT} > V_{IN} - V_{DROPOUT}$, then the linear regulator will not be able to regulate the output voltage at the desired voltage.

2. Power is dissipated in the pass transistor. The amount of power is $P = (V_{IN} - V_{OUT}) \times I_{LOAD}$. This dissipated power is wasted heat which causes the temperature of the regulator to increase.

Linear regulators have the following advantages:

1. Simple.
2. Cheap.
3. Power supply rejection ratio. Linear regulators respond quickly to changes in input voltage, producing an output voltage that is mostly free of any ripple on the input.
4. Responds quickly to changes in load voltage.
5. No switching noise. Other voltage conversion circuits, known as DC-DC converters, are susceptible to high-frequency switching noise. Linear regulators don’t have this downside.

The main disadvantage of linear regulators is that they are inefficient. This is due to the voltage drop across the pass element.

The output voltage level can be calculated using the following formula.

$$V_{OUT} = V_{REF} \times (1 + R1\backslash R2)$$

As can be seen, the level of the output voltage depends on the level of V_{REF} as well as on the ratio of resistors R1 and R2. To change the output voltage, it is necessary to change either the level of V_{REF} or the ratio of resistors R1 and R2. Next, we'll look at SLG47003-based designs and the typical SLG47003 circuit diagrams for each of these output voltage control options.

4. The Design

4.1 Circuit Design (Option with Adjustable Feedback Divider)

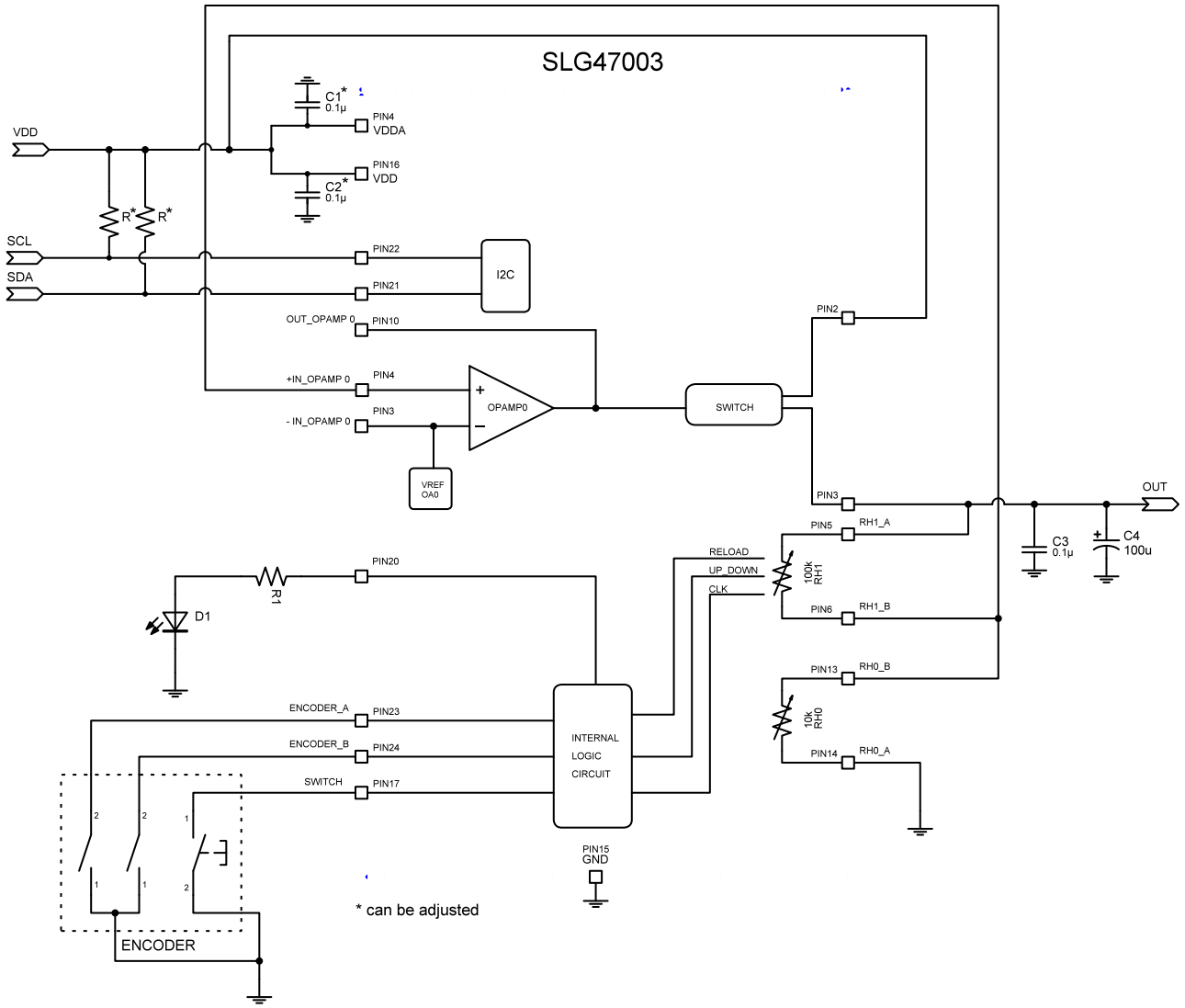


Figure 2: Voltage regulator design with encoder control (option with regulation using adjustable feedback divider)

As an example, a voltage regulator with encoder control (using an adjustable feedback divider) is designed using the SLG47003 IC and Go Configure software, see Figure 2.

It has the following parameters

- Input voltage range (V_{IN})**:** 5.0 V
- Output voltage adjustment range (V_{OUT})**:**
  - 0.5 to 4.5 V (I_{LOAD} = 10 mA),
  - 0.5 to 4.3 V (I_{LOAD} = 100 mA)
- Output current (I_{OUT}): 100 mA max

4.2 Go Configure Project (Option with Regulation Using Adjustable Feedback Divider)

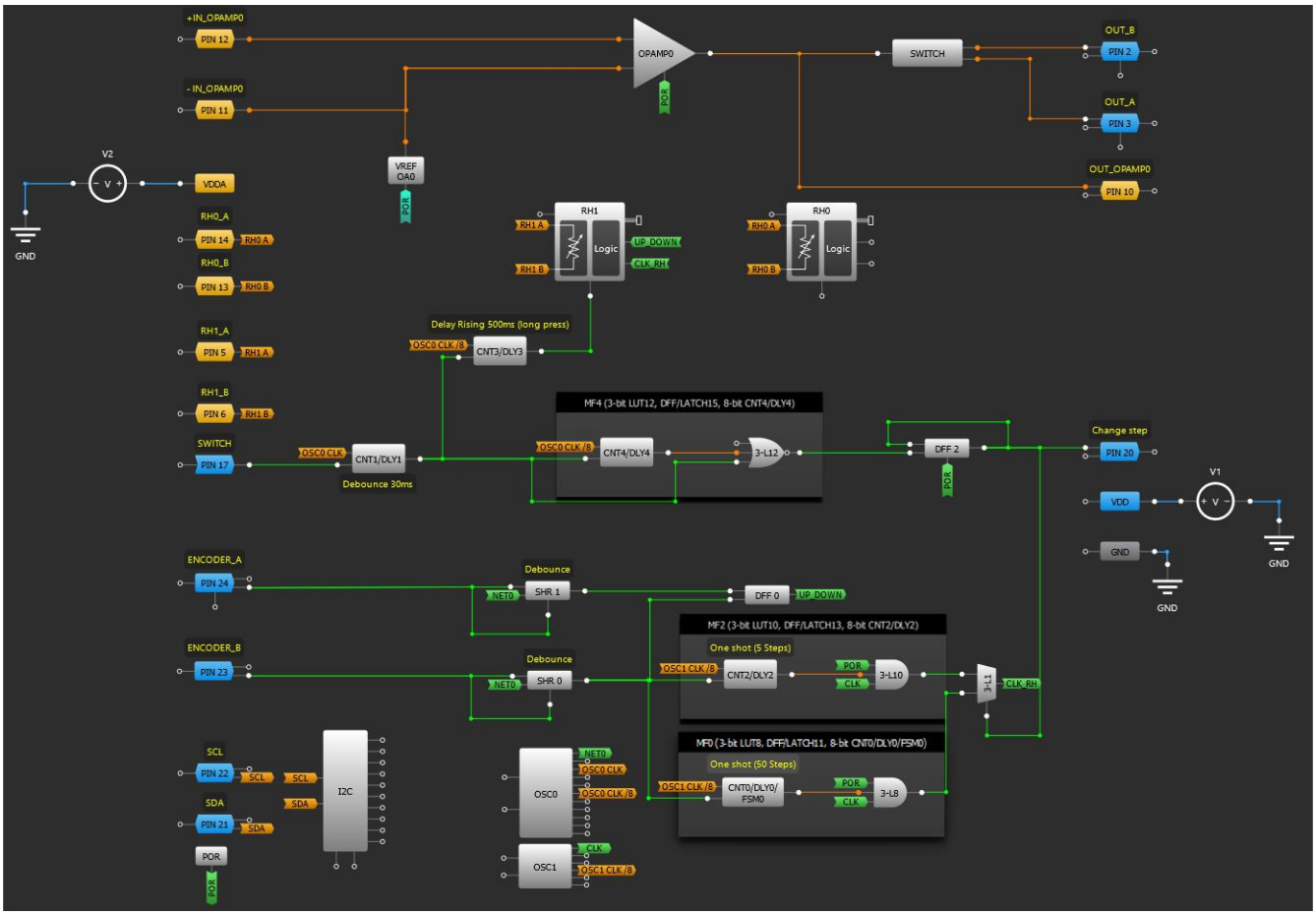


Figure 3: Voltage regulator with encoder control (option with regulation using an adjustable feedback divider)

This voltage regulator design demonstrates the operation of the SLG47003 chip as an adjustable voltage regulator with voltage control using an encoder (option with regulation using an adjustable feedback divider).

The design allows you to change the voltage at the output of the voltage regulator in the range from 0.5 V to 4.5 V, while the current supplied to the load should not exceed 100 mA.

Clockwise rotation of the encoder increases the voltage, while counterclockwise rotation decreases the voltage at the output of the voltage regulator. A short press of the encoder button changes the step of voltage change at the output of the voltage regulator (0.020 V or 0.20 V).

The indicator on the D1 LED (Change step) indicates the step of the voltage change. When the indicator is ON (light), the change step is 0.20 V, when the indicator is OFF (unlit), the change step is 0.020 V.

A long press (of more than 50 0 ms) on the encoder button reduces the voltage at the output of the voltage regulator to the minimum voltage (0.5 V).

The design includes the following basic components:

- OPAMP
- Vref
- Analog switch
- Digital rheostat
- Logical elements (LUTs, delays, DFFs).

The voltage regulator is built according to the standard scheme of the voltage regulator on the Op-Amp. In this scheme, the Op-Amp compares the voltage from the output of the voltage regulator, which is divided by the divider on the digital rheostats (RH1 and RH0), with a stable Vref voltage and controls the switch in analog mode. By opening or closing the analog switch depending on the voltage at the output of the regulator and the current consumed by the load, it maintains a stable voltage at the output of the voltage regulator.

To change the voltage supported by the voltage regulator, it is necessary to change the dividing coefficient of the divider on the digital rheostat RH1 and digital rheostat RH0. That is, change the resistance of the digital rheostat. The output voltage level can be calculated using the following formula.

$$V_{OUT} = V_{REF} \times (1 + RH1\backslash RH0)$$

The design makes it possible to control the digital rheostat in two ways, using I²C or using an encoder. When controlling via I²C, it is necessary to rewrite the values of the digital rheostat registers using I²C commands.

I²C register control data

Address Byte	Register Bit	Block	Function
0x91	reg<1165:1160>	--	Do not used
	reg<1167:1166>	RH0_SET[9:0]	Digital Rheostat0 Value Setting 00 0000 0000b: 0 Ω ~ 11 1111 1111b:100 kΩ
0x92	reg<1175:1168>		
0x93	reg<1181:1176>	--	Do not used
	reg<1183:1182>	RH1_SET[9:0]	Digital Rheostat1 Value Setting 00 0000 0000b: 0 Ω ~ 11 1111 1111b:100 kΩ
0x94	reg<1191:1184>		
0x9A	reg<1237:1232>	--	Do not used
	reg<1239:1238>	RH0_READ[9:0]	Digital Rheostat0 Readback Data (Read-only) 00 0000 0000b: 0 Ω ~ 11 1111 1111b:100 kΩ
0x9B	reg<1247:1240>		
0x9C	reg<1253:1248>	--	Do not used
	reg<1254:1255>	RH1_READ[9:0]	Digital Rheostat1 Readback Data (Read-only) 00 0000 0000b: 0 Ω ~ 11 1111 1111b:100 kΩ
0x9D	reg<1263:1256>		

I²C Commands:

1. [start] [0x00] [w] [0x91] [xxxxxxxx] [xxxxxxxx] [stop] // set Rheostat 0 value
2. [start] [0x00] [w] [0x9A] [start] [0x00] [R] [xxxxxxxx] [xxxxxxxx] [stop] // read Rheostat 0 value
3. [start] [0x00] [w] [0x93] [xxxxxxxx] [xxxxxxxx] [stop] // set Rheostat 1 value
4. [start] [0x00] [w] [0x9C] [start] [0x00] [R] [xxxxxxxx] [xxxxxxxx] [stop] // read Rheostat 1 value

A circuit based on logic elements is used for controlling the use of the digital rheostat.

On CNT1/DLY1 and on Shift Registers 0 and 1, the debounce suppression circuits are implemented in the encoder button contacts and the contacts of the encoder itself, respectively. The CNT1/DLY1 and the Shift Registers 0 and 1 macrocells work like a deglitch filter to eliminate switch bouncing.

Also input pins 17, 23, and 24 are set to operate as a Schmidt trigger digital inputs to reduce the effect of encoder contact bouncing,

The DFF0 element is used to determine the direction of rotation of the encoder. Delayed signal B appears on the CLK input of DFF0. Delayed signal A appears on D input of DFF0. When the encoder disk is rotating in a clockwise direction, signal A leads signal B and the DFF output is High, and likewise, when the disk is rotating in a counterclockwise direction signal B leads signal A and the DFF output is Low. So DFF0 can determine the direction of rotation. A High or Low signal on the Rheostat Up/Down input determines if internal counter's value increases or decreases for each pulse at the CLK input.

A timing diagram for the clockwise encoder rotation is shown in Figure 4 and for the counterclockwise encoder rotation in Figure 5.

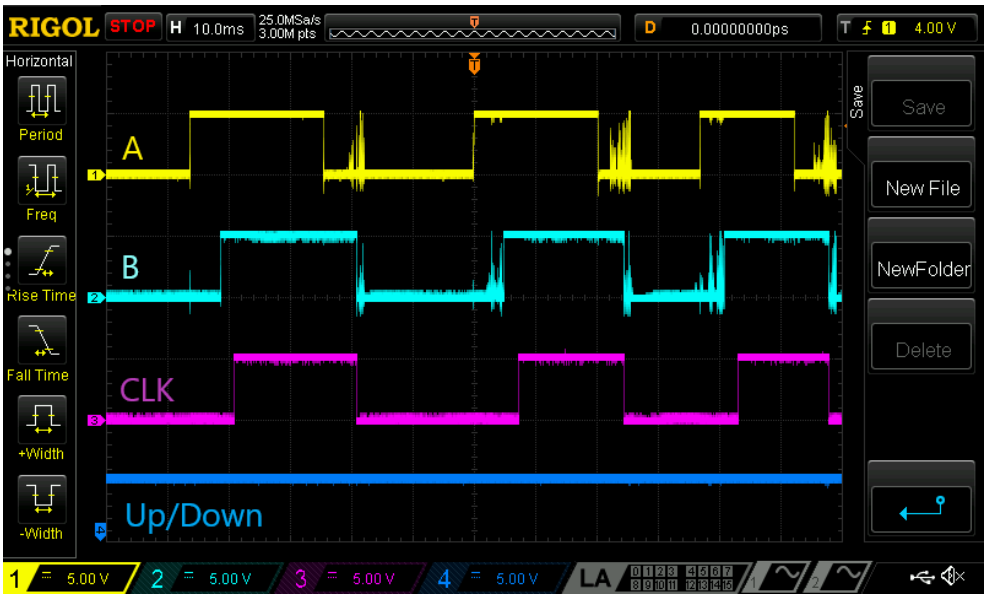


Figure 4: Timing Diagrams for Clockwise Encoder Rotation

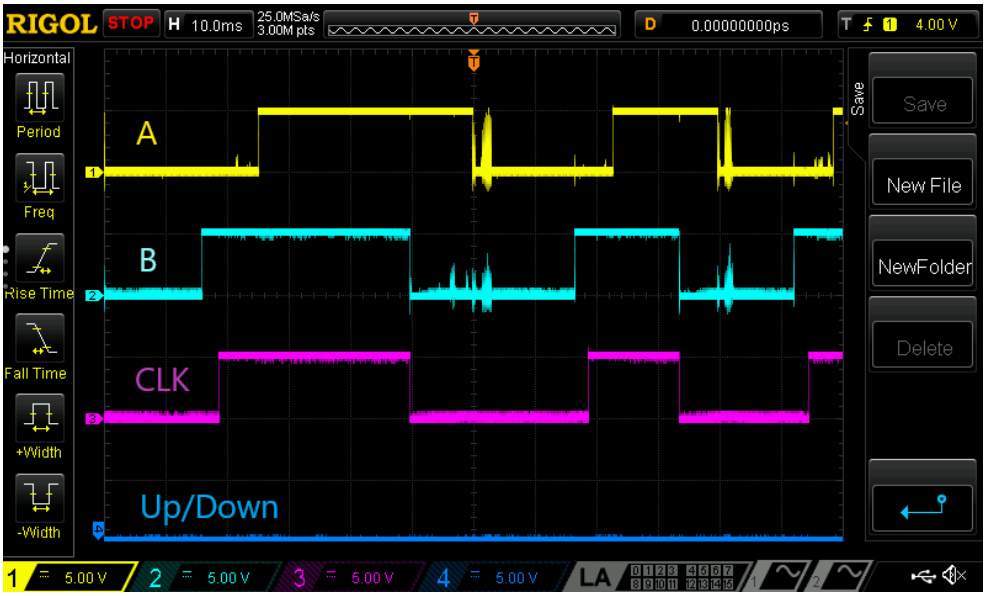


Figure 5: Timing Diagrams for Counterclockwise Encoder Rotation

A long press of the encoder button is detected by the CNT3/DLY3 element. CNT4/DLY4 and 3-bit LUT12 are designed to distinguish between a short and long press of the encoder button.

The elements DFF2, CNT0/DLY0, CNT2/DLY2, 3-bit LUT1, 3-bit LUT8, and 3-bit LUT10, form a circuit for switching the voltage change step at the output of the voltage regulato.

DFF2 changes the state of its output with each short (less than 250 ms) push of the encoder button. A one-shot on CNT2/DLY2 forms a pulse with a width of 31.36 µs, and the 3-bit LUT10 forms a burst of 50 pulses. A one-shot on CNT0/DLY0 forms a pulse with a width of 2.56 µs, and 3-bit LUT8 forms a burst of 5 pulses. The commutator on 3-bit LUT1 switches these two signals and transfers them to the CLK input of the rheostat RH1. The operation of this node is shown in Figure 6 and Figure 7.

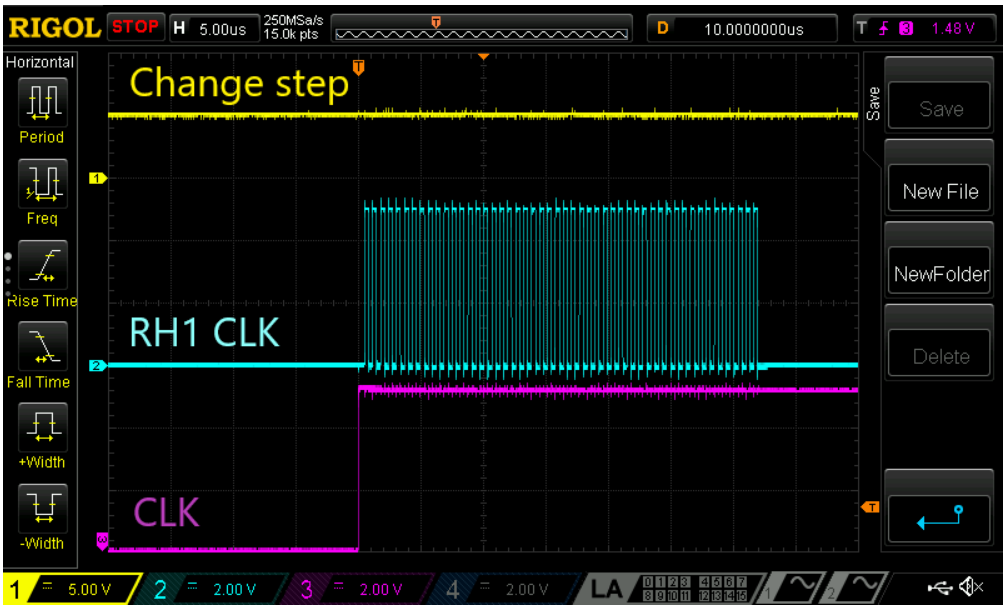


Figure 6: Timing Diagrams for digital rheostat switching in fifty steps

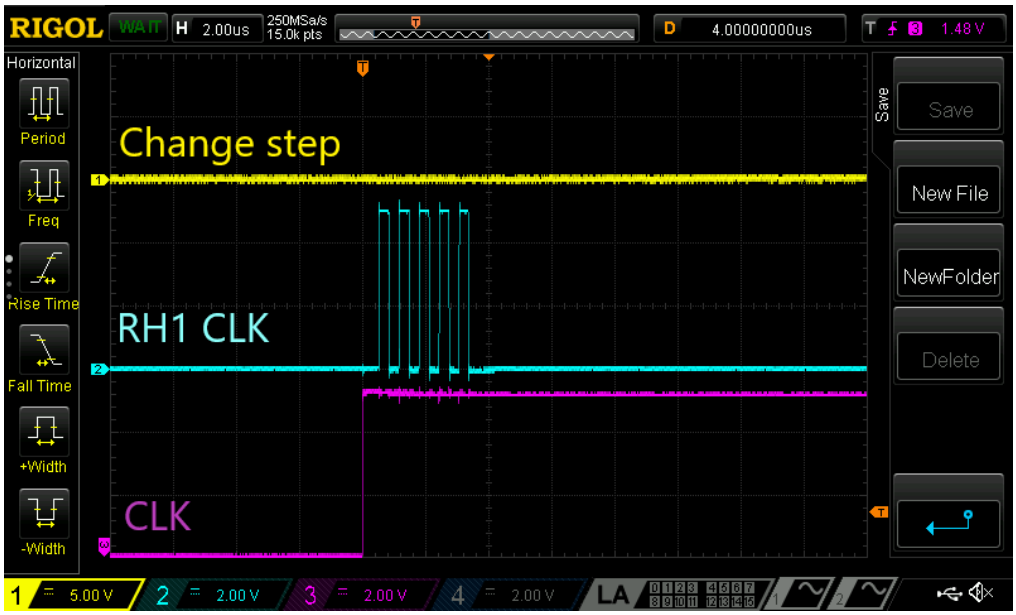


Figure 7: Timing Diagrams for digital rheostat switching in five steps

4.3 Circuit Design (Option with Regulation by Changing the V_{REF} value)

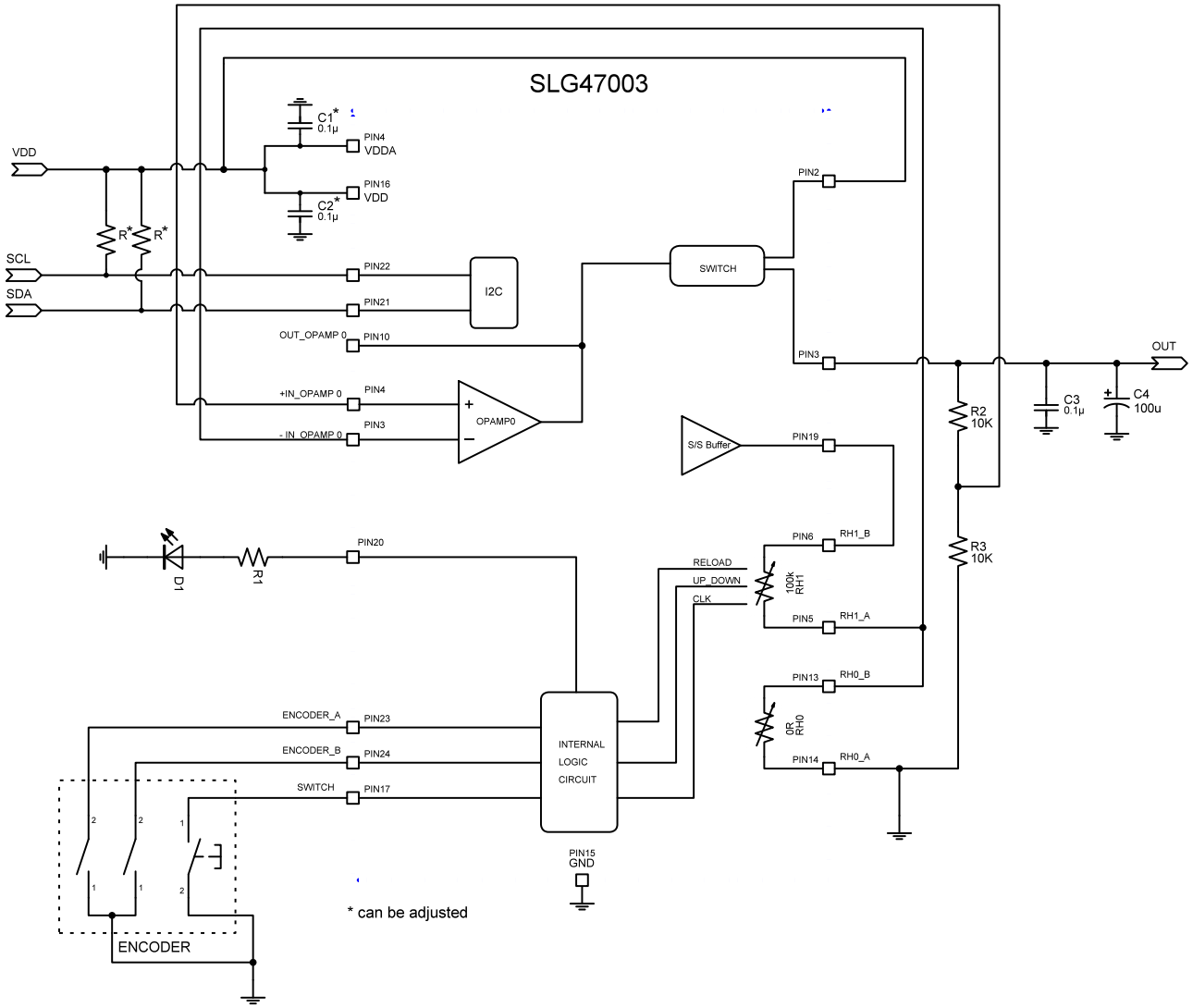


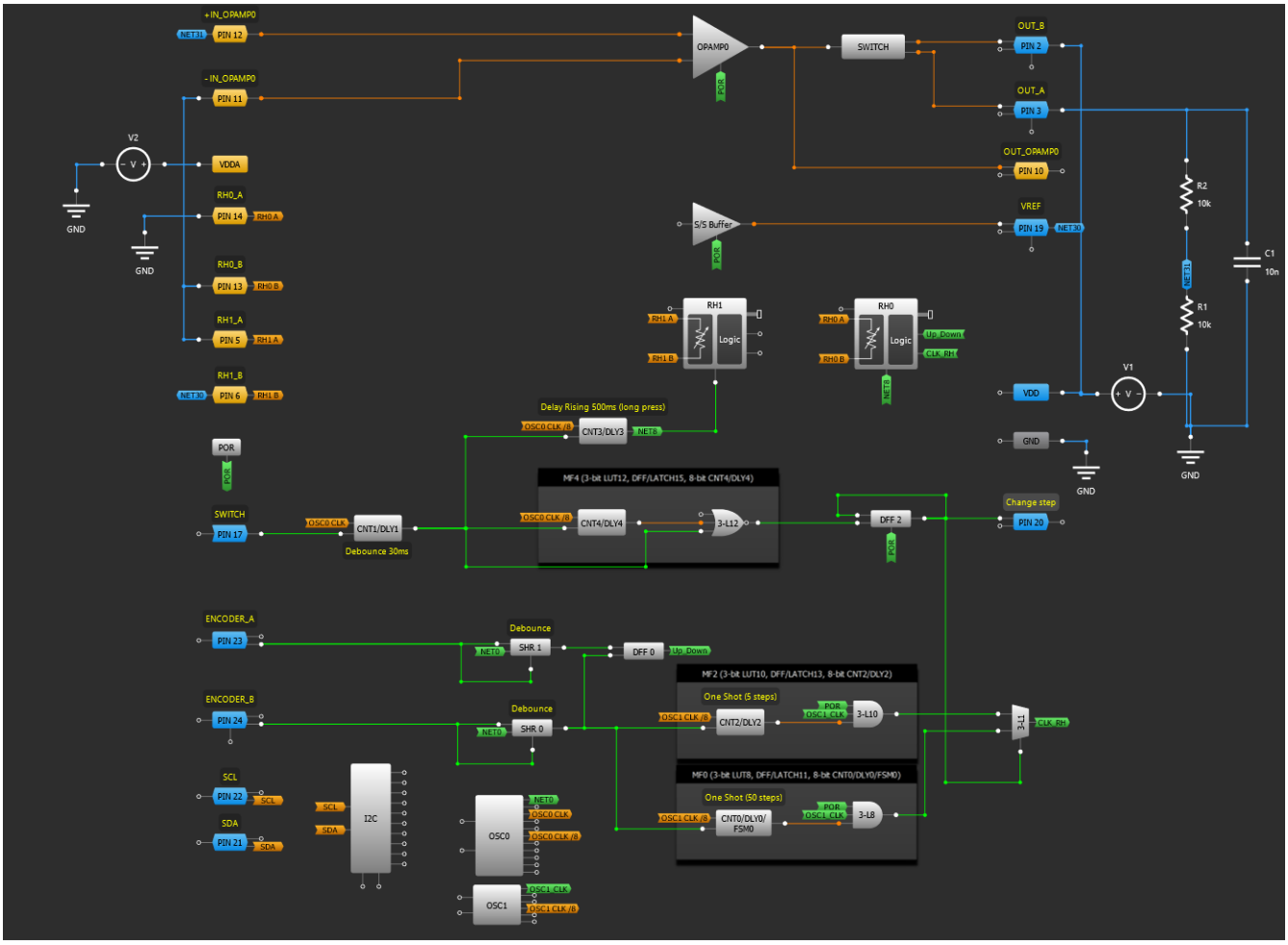
Figure 8: Voltage regulator with encoder control (option with regulation by changing the V_{REF} value)

Figure 2 shows a typical application circuit for the SLG47003 chip as a voltage regulator (option with regulation by changing the V_{REF} value).

It has the following parameters

- Input voltage range (V_{IN}): 5.0 V
- Output voltage adjustment range (V_{OUT}): 0 V to 4.0 V
- Output current (I_{OUT}): 100 mA max

4.4 Go Configure Project (Option with Regulation by Changing the V_{REF} Value)



This design is similar to the previous one. It has the same encoder management logic. The differences in this design are due to the analog parts. The design allows you to adjust the voltage in the range from 0 V to 4.0 V, unlike the previous one, whose adjustment range is from 0.5 V to 4.5 V. Another difference of this design is that when the encoder button is pressed for a long time, the output voltage is reduced to zero.

In this circuit, the operational amplifier compares the voltage from the output of the voltage regulator, which is divided by a divider on resistors R2 and R3, with a stable V_{REF} voltage that can be changed using a divider based on digital rheostats RH0 and RH1 in potentiometer mode, and controls the switch in analog mode. By changing the analog switch's resistance, depending on the voltage at the output of the voltage regulator and the current consumed by the load, the analog switch maintains a stable voltage at the output of the voltage stabilizer.

A sink/source buffer is used to make it possible to use the internal V_{REF} source and connecting the potentiometer to the digital rheostats RH0 and RH1, and the V_{REF} source.

In order to change the voltage maintained by the voltage regulator, it is necessary to change the division coefficient of potentiometer on the digital rheostats RH0 and RH1.

The output voltage level can be calculated using the following formula.

$$V_{OUT} = V_{REF} \times (1 + R2\backslash R3) \times (RH0/(RH0 + RH1))$$

As in the previous design, it is possible to control the voltage at the output of the regulator using I^2C. It is possible to change the resistance of the digital rheostats, as well as the V_{REF} level. The commands to change V_{REF} are given below.

I²C register control data

Address Byte	Register Bit	Block	Function
0x55	reg<682:680>	--	Do not used
	reg<687:683>	BUF_VREF_SEL[5:0]	Sink/Source Buffer V_{REF} Voltage Selection 000000b: 32 mV 000001b: 64 mV 000010b: 96 mV . . . 111110b: 2016 mV 111111b: N/A
0x56	reg<688>		
	reg<694:689>		

I2C Commands:

1. [start] [0x00] [w] [0x55] [xxxxxxxx] [xxxxxxxx] [stop] // set Sink/Source Buffer V_{REF} Voltage value

4.5 Testing Results

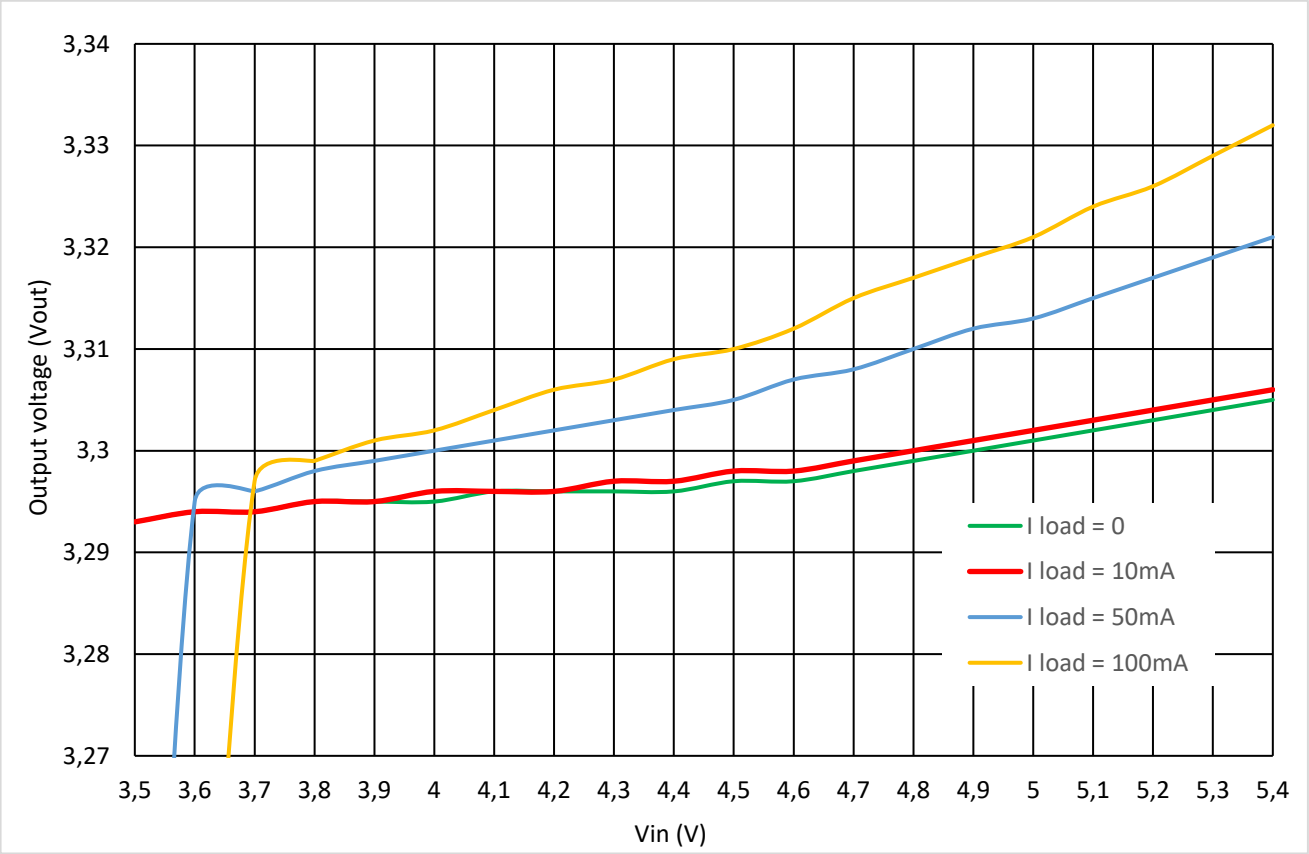


Figure 8: Line regulation $V_{OUT} = f(V_{IN})$ (output voltage = 3.30 V)

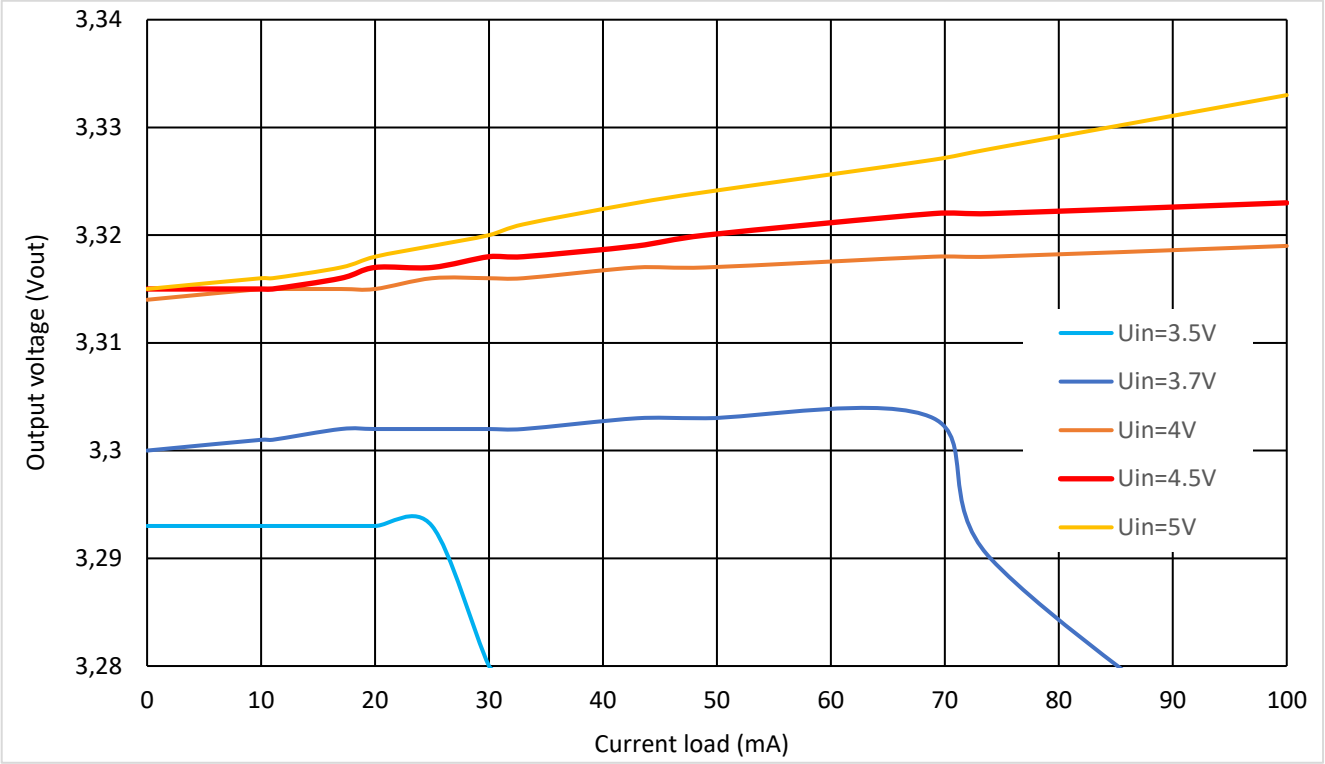


Figure 9: Load regulation V_{OUT} = f(I_{OUT}) (output voltage = 3.30 V)

5. Conclusions

The SLG47003 has everything needed to build an adjustable voltage regulator. This application note illustrates how to use the SLG47003 to implement the adjustable voltage regulator with either encoder control or with I^2C control which is a versatile solution and can be applied to an adjustable power supply among other things.

For the design option with regulation by changing the feedback divider, no external components are required except output capacitors. However this option does not allow for reducing the voltage at the output of the regulator to zero.

For the design option with regulation by changing the V_{REF} value, a few more external components are needed, in addition to the output capacitors, as two additional resistors for the divider are needed. However, this option makes it possible to reduce the voltage at the output of the regulator to zero if required.

6. Revision History

Revision	Date	Description
1.00	September 10, 2024	Initial release

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