

Addressable LEDs Control Using SLG47003  
SLG47003

This application note describes how to control addressable RGB LED WS2812B using the SLG47003 for creating visual decorative effects. The SLG47003 features a 59-byte Extended Pattern Generator with an 8-bit width converter, which in conjunction with the SLG47003’s many configurable logic components make it possible to create a control system for addressable RGB LEDs.

This application note comes complete with design files which can be found in the Reference section.

**Contents**

1. **Terms and Definitions** ..... 2

2. **References**..... 2

3. **Introduction** ..... 2

4. **Operating Principle**..... 2

5. **AnalogPAK Design** ..... 4

6. **Design Testing** ..... 7

    6.1 Waveforms..... 8

7. **Conclusion** ..... 9

8. **Revision History** ..... 10

**Figures**

Figure 1. PWM Control Signal .....3

Figure 2. Timings of the 0 and 1 Coded Signals .....3

Figure 3. Cascade Method .....3

Figure 4. Data Transmission Method (Example for Strip of 3 LED) .....3

Figure 5. LED Color Data .....3

Figure 6. EPG Filled with Color Codes .....4

Figure 7. AnalogPAK Design .....5

Figure 8. Standard Rainbow (20 colors), with HEX Codes of Colors .....6

Figure 9. PWM Converter Operation .....6

Figure 10. Application Schematic .....7

Figure 11. The part of Design with Additional PINs 18 and 19.....8

Figure 12. 8x8 LED Matrix, all LEDs ON After Sending the First Fragment of Data.....9

## 1. Terms and Definitions

CNT/DLY	Counter/Delay
DFF	D Flip-Flop
EPG	Extended Pattern Generator
LED	Light-emitting diode
LUT	Look-up Table
MCU	Micro controller unit
MUX	Multiplexer
NVM	Non-volatile memory
OSC	Oscillator
RGB	Red Green Blue
SHR	Shift register

## 2. References

For related documents and software, please visit:

[AnalogPAK™ | Renesas](#)

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

- [1] [GreenPAK Go Configure Software Hub](#), Software Download and User Guide, Renesas Electronics
- [2] [AN-CM-384 Addressable LEDs Control Using SLG47003](#), Design File, Renesas Electronics
- [3] [GreenPAK Development Tools](#), GreenPAK Development Tools Webpage, Renesas Electronics
- [4] [GreenPAK Application Notes](#), GreenPAK Application Notes Webpage, Renesas Electronics
- [5] [Video](#), Renesas Electronics

## 3. Introduction

The WS2812B is an intelligently controlled RGB LED light source. It is widely used in LED strips for visual decorative effects. The control circuit and RGB chip are integrated into a single package of components, to form a complete addressable LED pixel. The WS2812B is controlled using a digital serial protocol and a single data line.

In this design, we will use the SLG47003 to implement a visual effect of a running display of 20 rainbow colors in a 64 LED matrix.

## 4. Operating Principle

The internals of the WS2812B includes an intelligent digital port data latch and signal reshaping amplification drive circuit. It also includes a precision internal oscillator and a voltage-programmable constant current control block, effectively ensuring high color consistency.

After the LED power-on reset occurs, the DIN port receives data from the AnalogPAK SLG47003. The first LED collects the initial 24-bit data which is sent to the internal data latch. The internal signal sends the data to the reshaping amplification circuit which then sends the data to the next cascaded LED through the DO port. After transmission for each LED, the signal is reduced by 24 bits (see [Figure 3](#) and [Figure 4](#)). When the low-level signal is held for a period  $> 50 \mu\text{s}$ , all the received data is latched and displayed by the LEDs.

For programming the LEDs, a serial bitstream of logical 0s and 1s should be transformed into pulse width modulated voltage levels (see [Figure 1](#)). The timings are described in [Figure 2](#). So, the transfer time of 1 bit of data is:

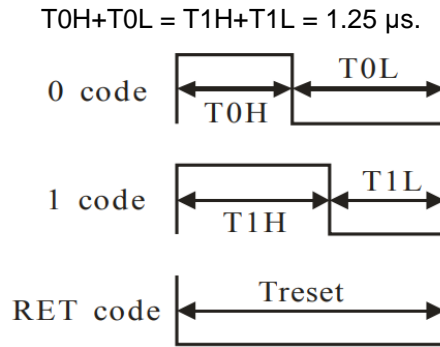


Figure 1. PWM Control Signal

T0H	0 code, high voltage time	0.4 $\mu s$	$\pm 150 ns$
T1H	1 code, high voltage time	0.85 $\mu s$	$\pm 150 ns$
T0L	0 code, low voltage time	0.85 $\mu s$	$\pm 150 ns$
T1L	1 code, low voltage time	0.4 $\mu s$	$\pm 150 ns$
Reset	Low voltage time	Above 50 $\mu s$	

Figure 2. Timings of the 0 and 1 Coded Signals

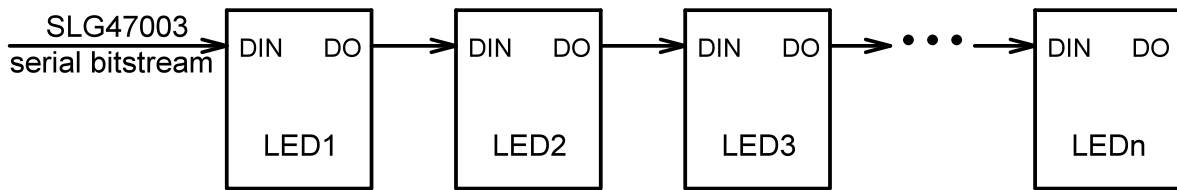


Figure 3. Cascade Method

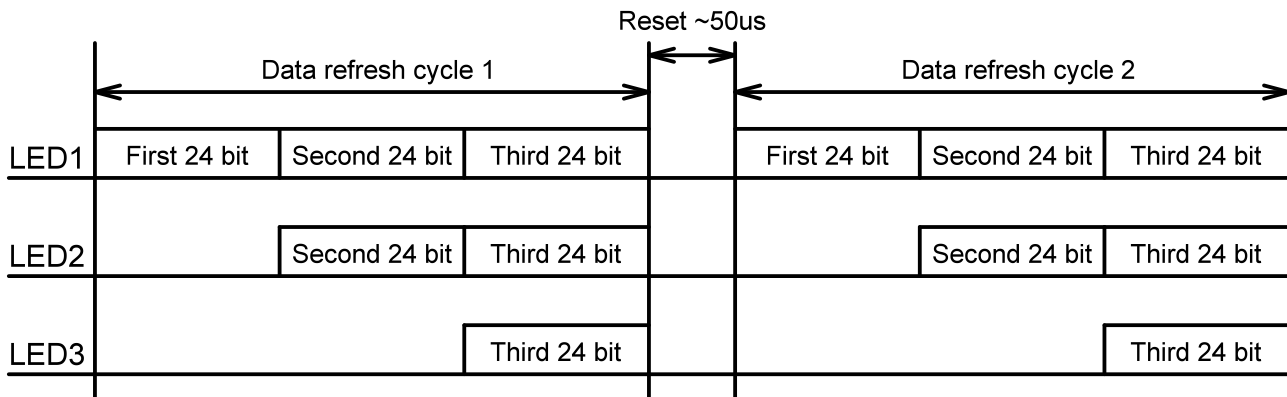


Figure 4. Data Transmission Method (Example for Strip of 3 LED)

Please note the data received by LED1 is sent by the AnalogPAK device (SLG47003 in this application), while data sent to LED2 and LED3 is transmitted through the LED internal reshaping amplification circuit.

The 24-bit data segment contains information about the brightness of each of the three primary colors (Red, Green, and Blue). Each primary color has 256 brightness steps (8 bits). We can see the composition of the 24-bit data below.

G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0	B7	B6	B5	B4	B3	B2	B1	B0
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Figure 5. LED Color Data

**Note:** Follow the order of GRB to send data with the most significant bit sent first.

The Extended Pattern Generator (EPG) is used to store the color codes in the SLG47003 (see [Figure 6](#)). The logic components of the SLG47003 are used to convert the EPG data into a serial bit stream (in 24-bit segments). Also, using the AnalogPAK allows us to create a state machine for controlling the LEDs – turning on, turning off, changing modes, etc.

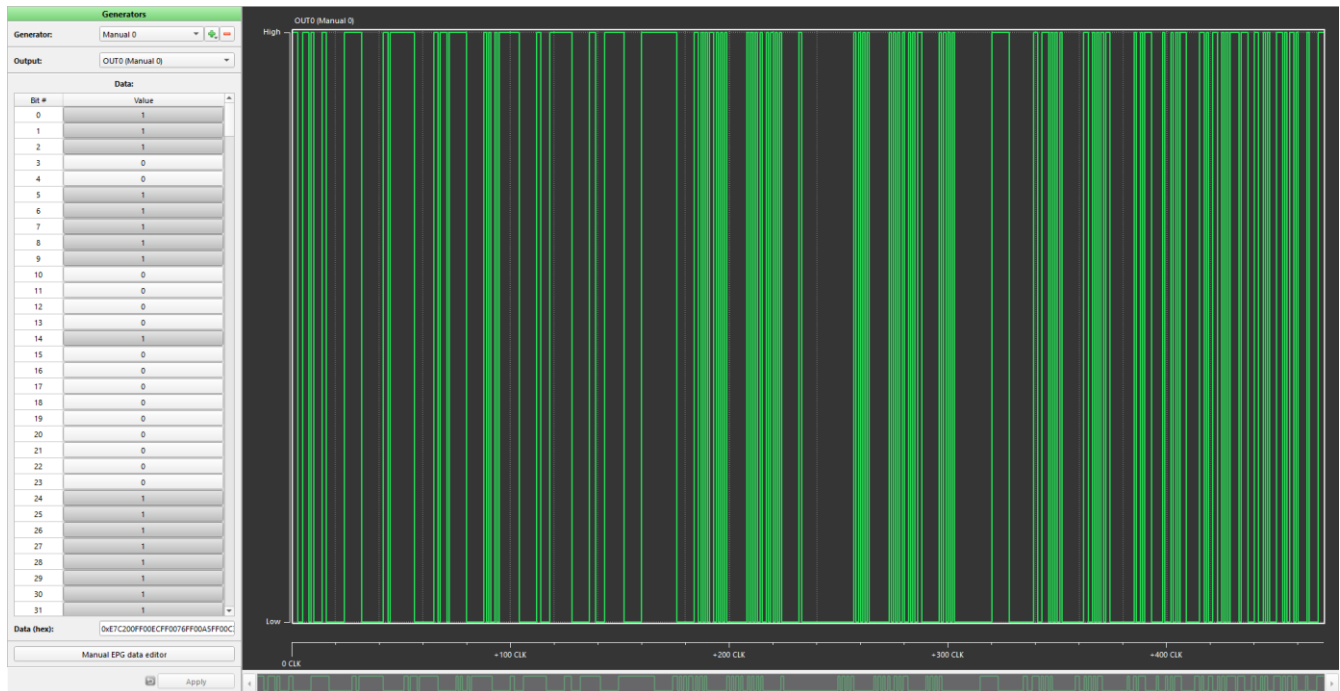


Figure 6. EPG Filled with Color Codes

## 5. AnalogPAK Design

The Extended Pattern Generator (EPG) is a key part of the design. The EPG range is 59 bytes, and is stored in the NVM. The EPG also has a width converter and supports four conversion modes:

- 8-to-8 Mode (8-bit parallel output);
- 8-to-4 Mode (8-bit word to two 4-bit words);
- 8-to-2 Mode (8-bit word to four 2-bit words);
- 8-to-1 Mode (8-bit word to serial bit stream).

The EPG is used in 8-to-1 mode in this design. This EPG mode and the flexible AnalogPAK logic components allow us to easily create a serial bit stream of data to control the WS2812B LED matrix.

To control the addressable LEDs, we need to generate 24-bit fragments of data for each LED in the matrix. Considering that the EPG has 59 bytes of dedicated NVM memory and one more byte for the Initial state, we have  $60 \times 8 = 480$  available bits in total. So  $480/24 = 20$  different colors can be stored at a time in the SLG47003. In this design, the EPG is programmed with 20 standard rainbow colors for demonstration (see [Figure 8](#)).

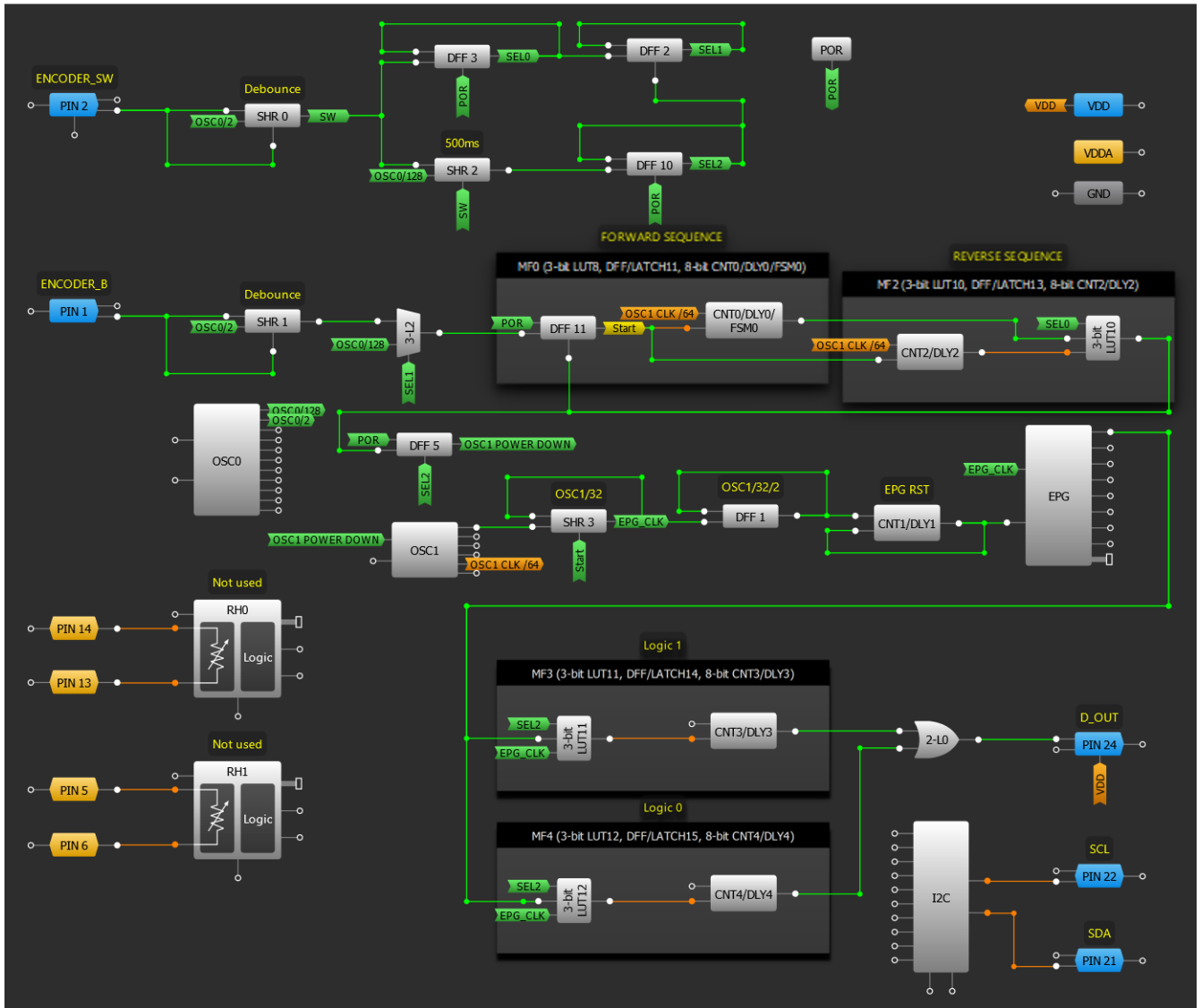


Figure 7. AnalogPAK Design



Figure 8. Standard Rainbow (20 colors), with HEX Codes of Colors

To program the WS2812B LEDs, the data from the EPG must be converted into a PWM signal with a fixed high-level time. For Logic 1: 0.85 μs, for Logic 0: 0.4 μs, and the PWM period is 1.25 μs. These timings are not so strict and allow for some deviation.

The PWM converter consists of 3-bit LUT11 and DLY3 for encoding logical 1s, and 3-bit LUT12 and DLY4 for encoding logical 0s (see Figure 7). Using the internal dividers of OSC1 and shift register SHR3 to divide by 4, we get an EPG\_CLK signal with a frequency of about 780 kHz (1.28 μs period). The design uses the EPG\_CLK signal as the CLK source for the EPG and for converting the EPG data into the PWM signal. Each rising edge of the EPG\_CLK signal outputs a new bit from the EPG to the input of the PWM converter (see Figure 9). The following falling edge of the EPG\_CLK signal triggers the corresponding One-shot (DLY3 or DLY4) to generate a PWM signal with a particular high-level time (logical 1 or 0).

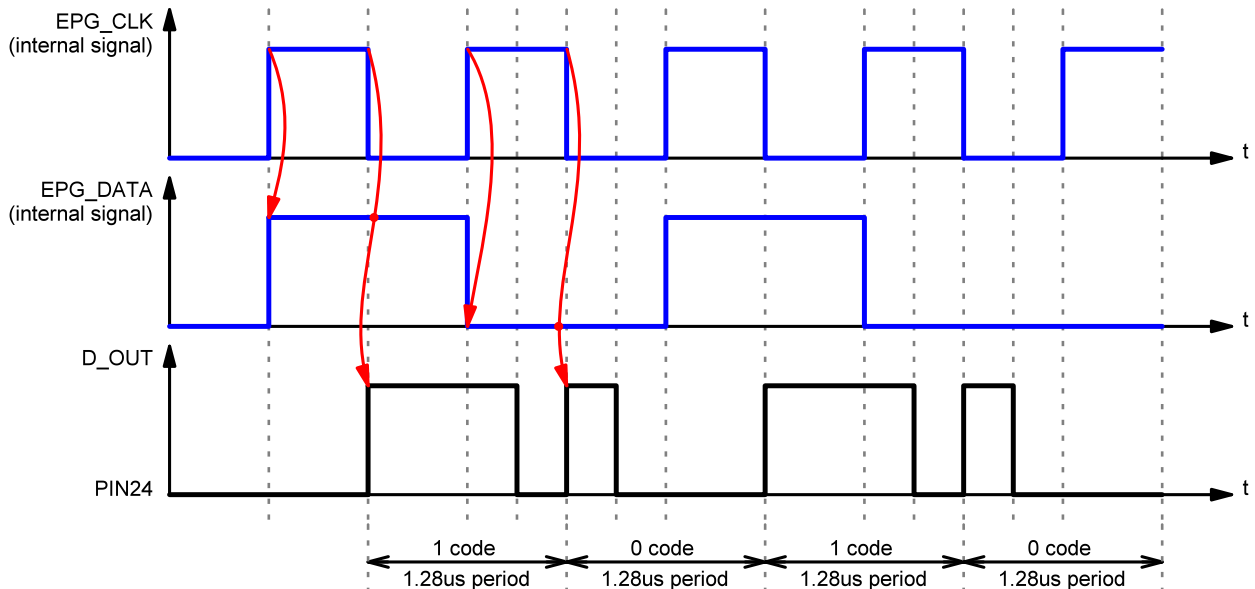


Figure 9. PWM Converter Operation

As mentioned above, we have 480 bits for implementing 20 rainbow colors. Therefore, to write all 20 colors to the LED matrix, we need 480 pulses on the CLK input of the EPG. If we send 480 pulses every recording cycle, it is clear that each LED of the matrix will always glow in some specific color (one of 20). Therefore, we will send 24 more or 24 fewer pulses for each cycle to display a running colors effect. The EPG CLK generator, composed of DFF11, 3-bit LUT10, DLY0, and DLY2 are used to send the appropriate number of pulses to the EPG CLK input. Each rising edge from MUX 3-L2 triggers the EPG CLK generator, sends this group of pulses, which then rewrites the LEDs of the matrix. Since the LED matrix has 64 LEDs and the EPG contains only 20 colors, the design will send 20 color codes four times to light up all LEDs in the matrix.

DLY1 resets the EPG after every 480 bits. This is necessary because we need to use the Initial byte of the EPG for every rewrite cycle. This Initial byte is available only after the EPG is reset.

The design is controlled by an encoder. Shift registers SHR0 and SHR1 are used for the debounce function. The encoder switches the state machine, which is composed of DFF2, DFF3, and DFF10. The state machine controls 3-bit LUT10, 3-bit LUT11, 3-bit LUT12, and MUX 3-L2.

A long press of more than 500 ms on the encoder button turns the LED matrix ON and OFF. The 500 ms delay is provided by shift register SHR2. A short press on the encoder button selects the operating mode:

- Forward – continuously running
- Reverse – continuously running
- Forward – running by turning the encoder clockwise (ENCODER\_B input)
- Reverse – running by turning the encoder counter-clockwise (ENCODER\_B input).

When continuously running mode is chosen (either Forward or Reverse) the EPG CLK generator is triggered by each period of OSC0/128 (62.5 ms), and we observe the running colors. When ENCODER\_B is chosen, we can start the rewriting cycle of the LED matrix manually. In this case, when we turn the encoder knob, each pulse from the encoder will shift the LEDs matrix by one color. To turn OFF the LED matrix, a zero code will be written to all LEDs.

## 6. Design Testing

The application schematic is shown in Figure 10. The quiescent current of the design is about 1  $\mu$ A at  $V_{DD} = 5$  V. In the continuously running mode, the design current consumption is about 20  $\mu$ A (average value) at  $V_{DD} = 5$  V. The main current consumer is the 25 MHz oscillator, so the current consumption of this design depends on the  $V_{DD}$  voltage level and the frequency of the LEDs refresh rate.

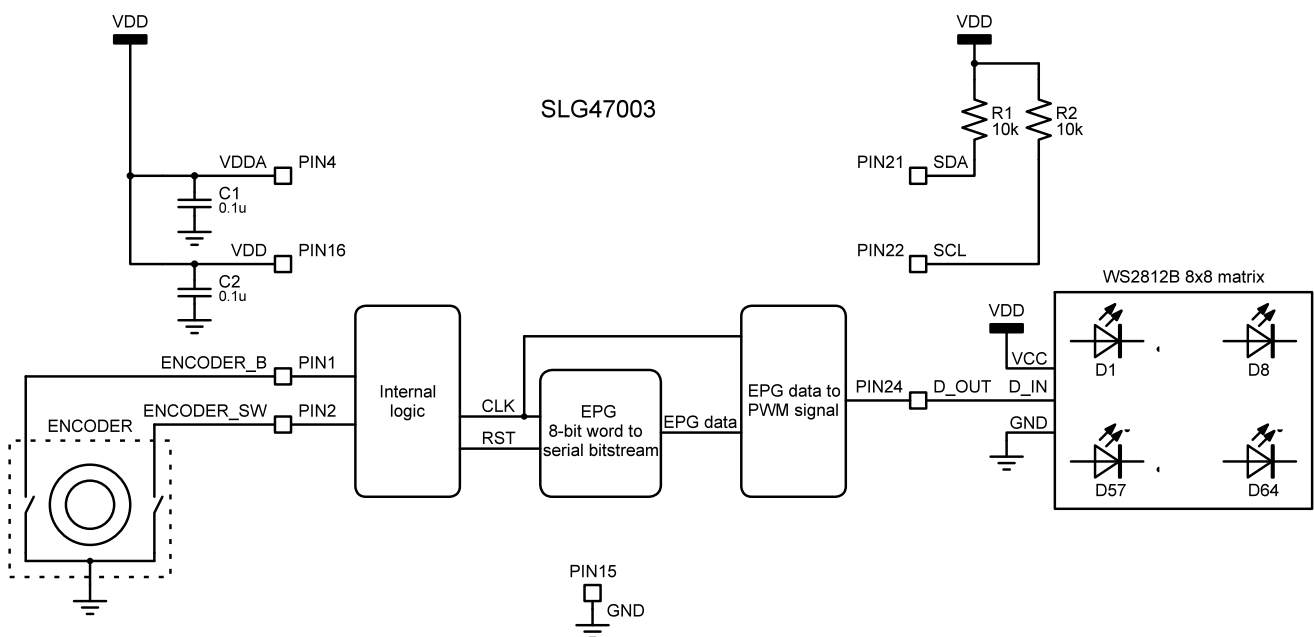


Figure 10. Application Schematic

To demonstrate how the design works (sending the bitstream), two additional PINs are used for EPG\_CLK and EPG\_DATA signals so that we can see the waveforms (see Figure 11).

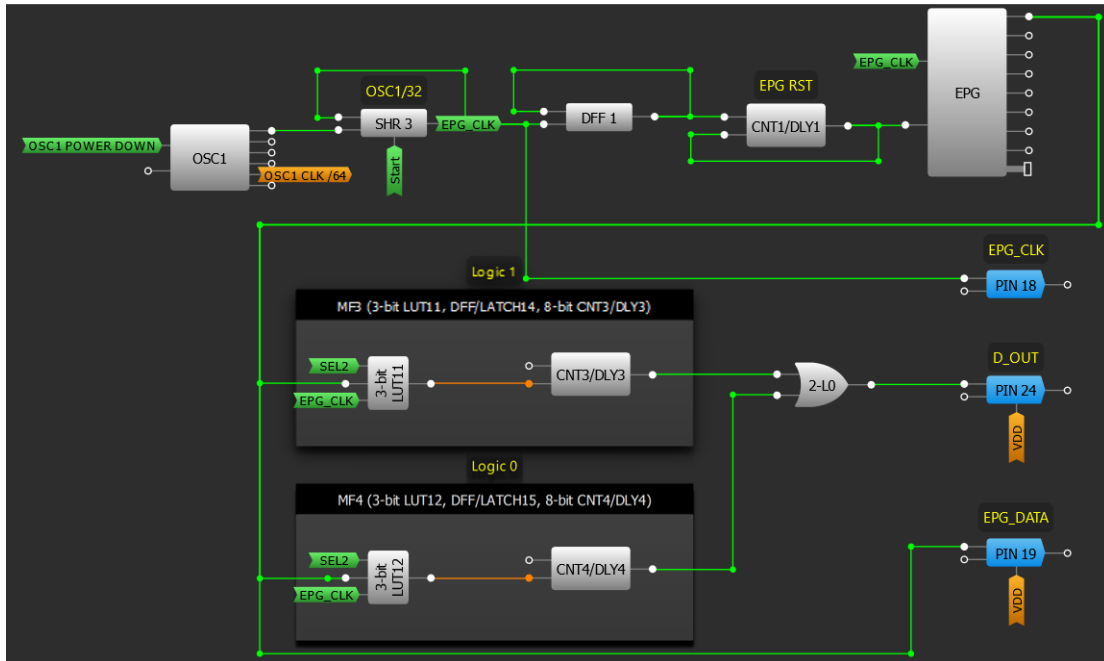
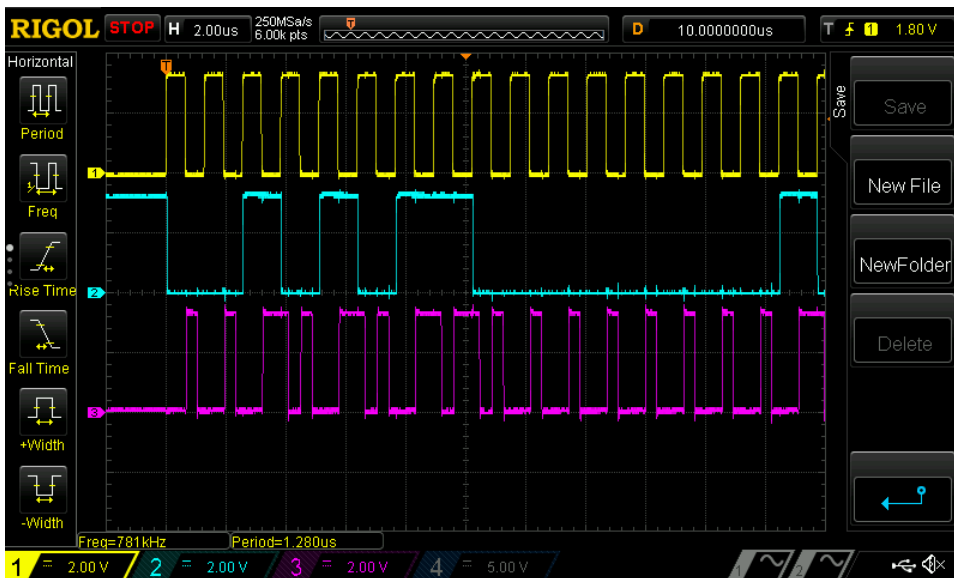


Figure 11. The part of Design with Additional PINs 18 and 19

### 6.1 Waveforms

- Channel 1 (yellow/top line) – PIN# 18 (EPG\_CLK)
- Channel 2 (light blue/2nd line) – PIN# 19 (EPG\_DATA)
- Channel 3 (magenta/3rd line) – PIN# 24 (D\_OUT)

1. Design functionality. Sending the bitstream

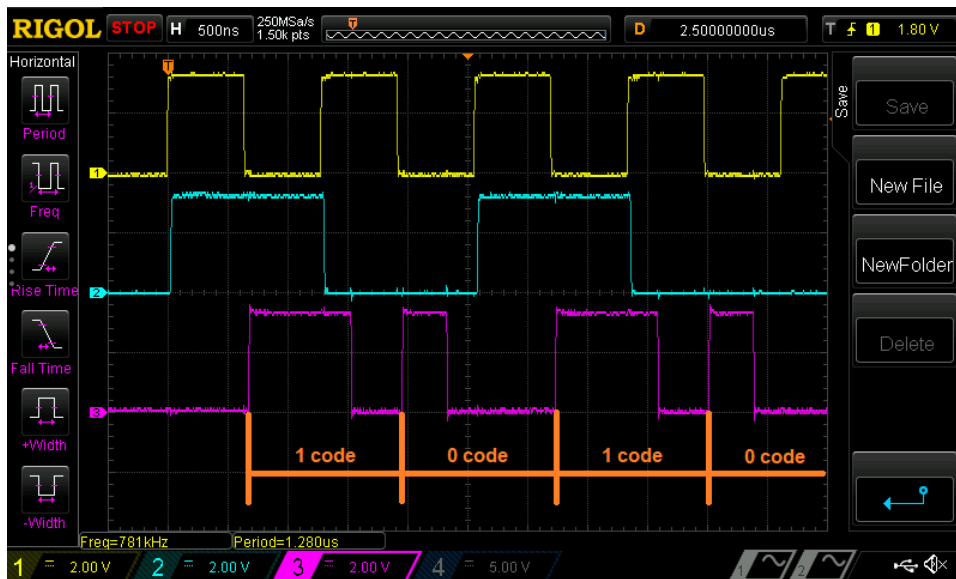


Note: The magenta signal (Channel 3) shows the data stream that will be written to the LED matrix.

- Channel 1 (yellow/top line) – PIN# 18 (EPG\_CLK)
- Channel 2 (light blue/2nd line) – PIN# 19 (EPG\_DATA)
- Channel 3 (magenta/3rd line) – PIN# 24 (D\_OUT)

2. Design functionality. PWM converter operation





Note: As shown in the waveforms, the PWM converter works as expected (see Figure 9).



Figure 12. 8x8 LED Matrix, all LEDs ON After Sending the First Fragment of Data

To see the demonstration of the design functioning in all modes, please follow the link: [Video](#).

## 7. Conclusion

This application note describes how to create a pattern generator of decorative visual effects using the AnalogPAK SLG47003 and a matrix of WS2812B LEDs.

The flexibility of AnalogPAK makes it possible to implement in a single chip with low power consumption functions such as debounce for encoder outputs, a state machine for controlling the LED matrix, storing the color data of 20 LEDs, creating a visual effect of running colors, and converting data and to control WS2812B LEDs.

## 8. Revision History

Revision	Date	Description
1.00	September 10, 2024	Initial release.

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