Offset and Gain Trim with AnalogPAK
SLG47003V

Contents

1. References

For related documents and software, please visit:

AnalogPAK™ | Renesas

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics
[2] AN-CM-385 Offset and gain trim with AnalogPAK, Design File, Renesas Electronics
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics
[5] SLG47003V Datasheet

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2. Terms and Definitions

I^2C	Inter-integrated circuit (bus)
LED	Light-emitting diode
MS ACMP	Multichannel Sampling Analog Comparator
MF	Multi-Function Macrocell
OpAmp	Operational Amplifier
PCB	Printed circuit board
Vref	Voltage reference

3. Introduction

This AnalogPAK design demonstrates the concept of offset and gain tuning for various analog circuits with the AnalogPAK. The main task of this application note is to demonstrate the basic concepts of analog technology, notably Offset and Gain and their correct application.

The purpose of this design (Figure 1) is to apply gain trim and offset to the input sinusoidal signal by changing the resistance of the rheostats RH0 and RH1 so that it does not go beyond the limits defined by the MS-ACMP. The condition of the output signal is displayed using red and green LEDs (Figure 2).

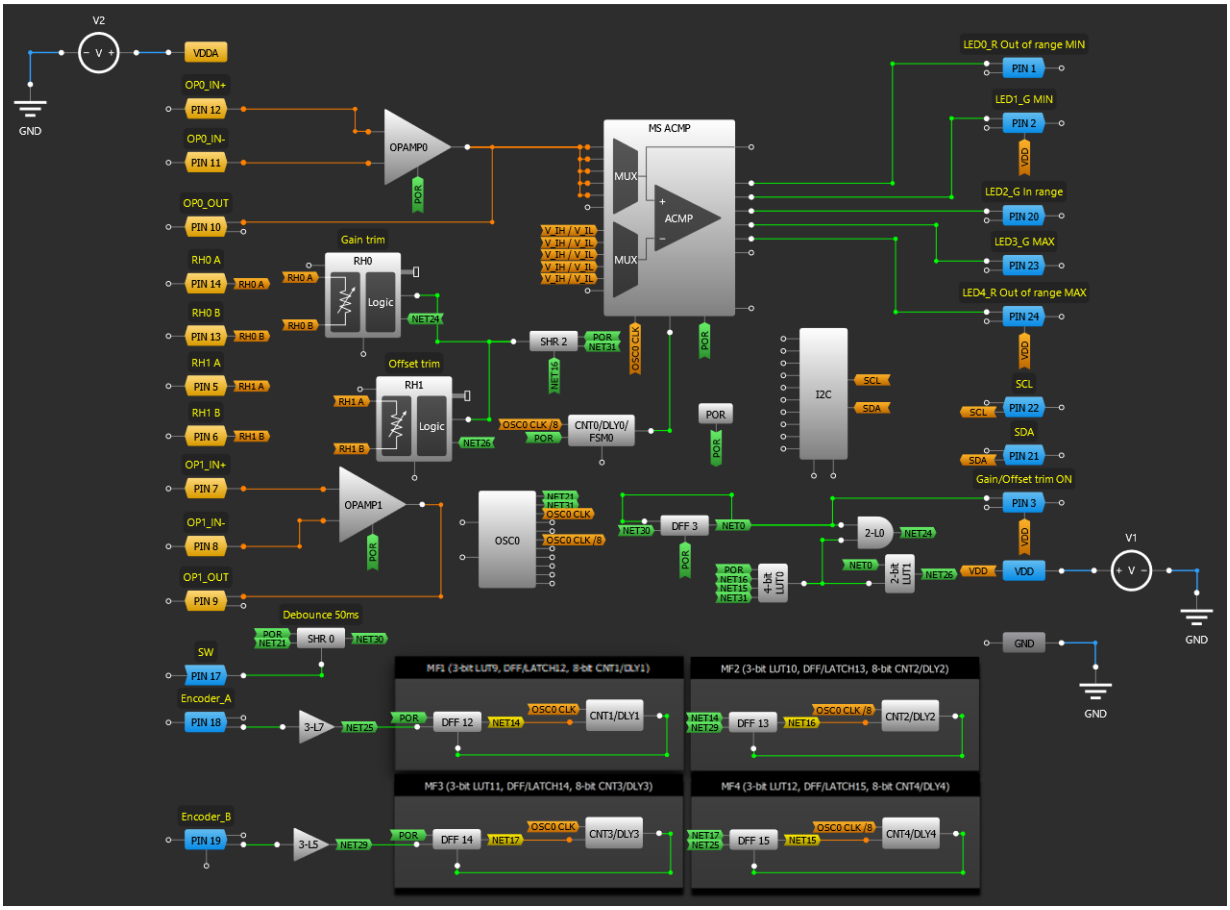

Figure 1. Offset and gain trim design block diagram

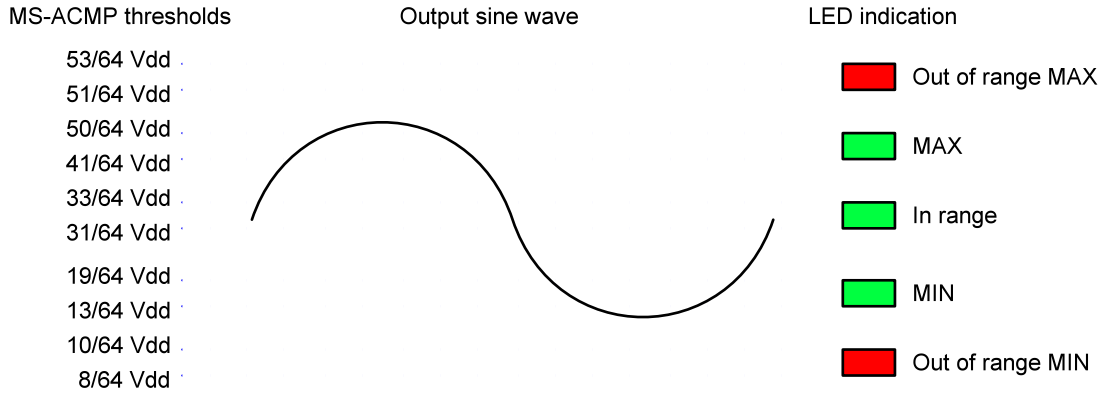

Figure 2. MS ACMP thresholds

4. Design operation

Conventionally, this design can be divided into the following functional parts (Figure 1 and Figure 3):

- **Signal processing channel:**

  Includes a voltage follower with OpAmp1 that operates as a buffer for the resistive divider R-RH1 to offset compensation trimming, and for operational amplifier OpAmp0 with rheostat RH0 for inverting input for gain trimming.

- **Devices and macrocells for adjusting the gain and offset:**

  Includes an Encoder with a button, and encoding logic with the multifunctional macrocells MF1 through MF4. Also, includes set of logic elements for mode switching and trimming Gain and Offset.

- **Visualization devices and macrocells:**

  To visualize the Gain and Offset trimming process, an MS-ACMP is used as a multi-channel comparator in Range mode with five threshold voltages. In Range mode, one analog input is compared with a maximum of six thresholds and the result is latched at the output of each activated channel by the pulse(s) at the CLK input. At the same time each output of the MS-ACMP turns on the corresponding LED (D3 - D7) (Figure 1 - Figure 3). The Encoder's button and the Gain/Offset trim “ON” LED are used to switch from Gain trim to Offset trim and back.

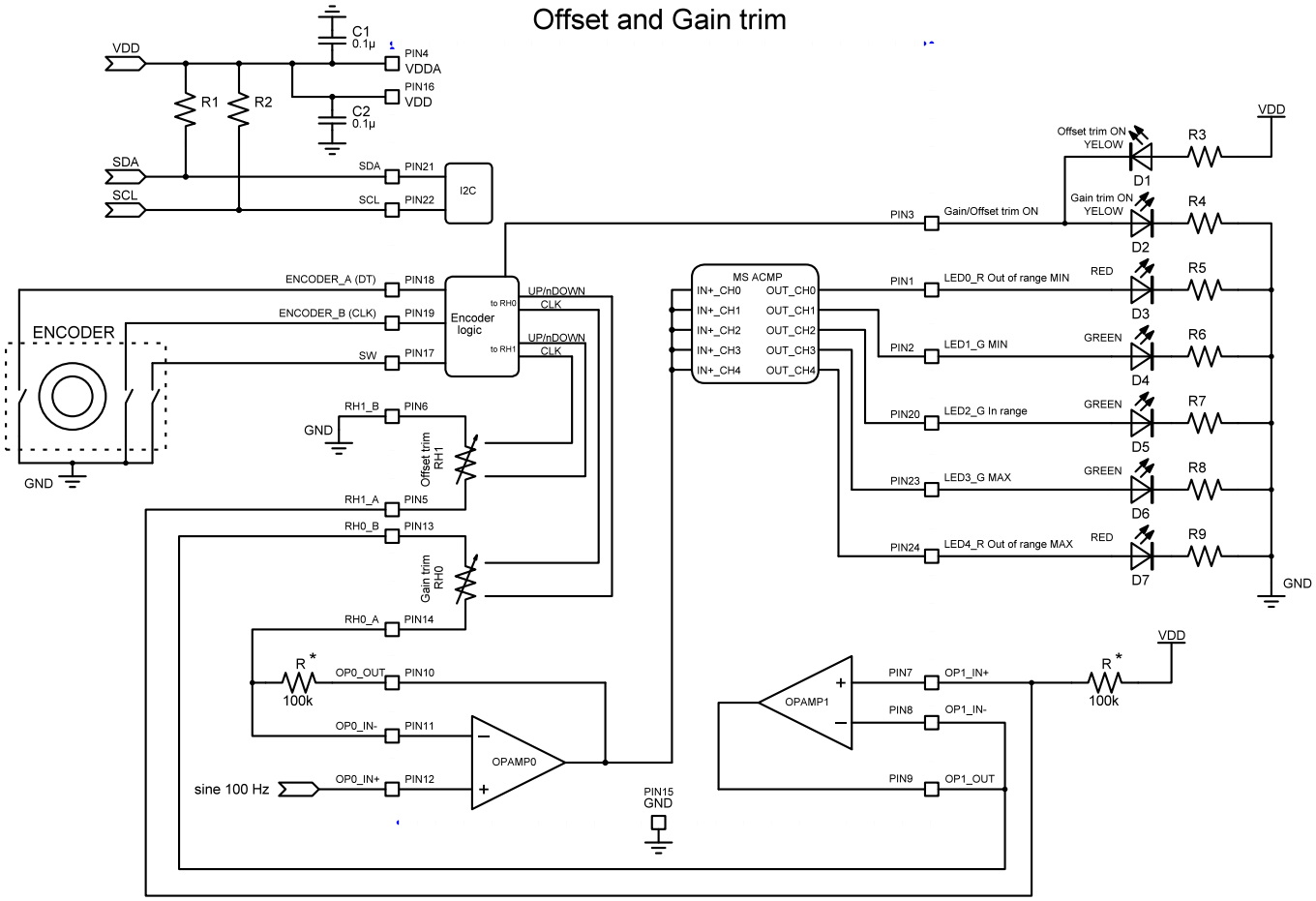

Figure 3. Offset and gain trim typical application circuit

After turning on the power supply by turning the encoder clockwise/counterclockwise, and switching between Gain and Offset trim modes with the encoder button, the OpAmp0 output signal needs to adjusted so that all the green LEDs light up (Figure 3). This indicates that the output sine wave is within the specified limits as shown in Figure 2.

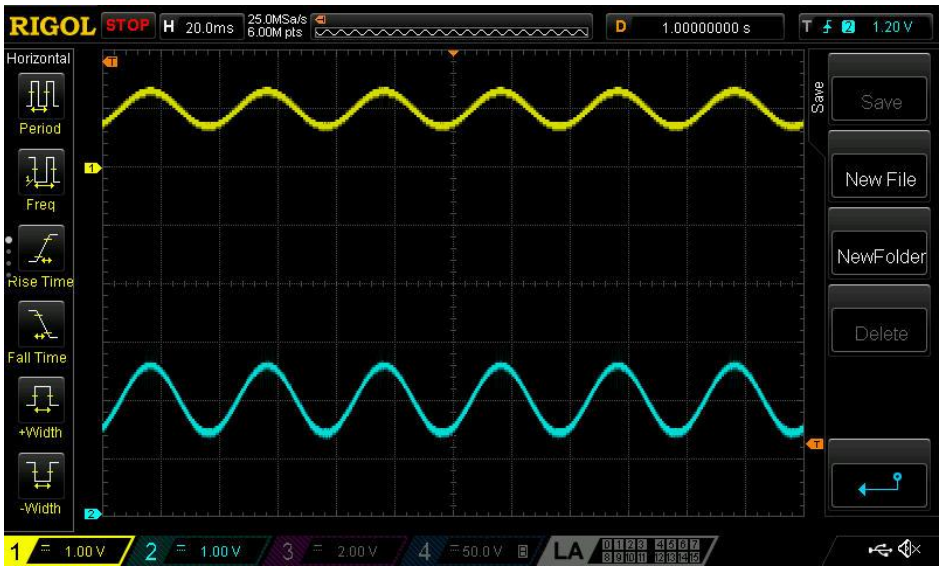

Figure 4. Initial design condition

In the initial state after turning on, Offset compensation voltage is 0 V and OpAmp1 gain is 2, as shown in Figure 4 where CH1 is the input sinewave with offset 1 V and CH2 is the output signal.

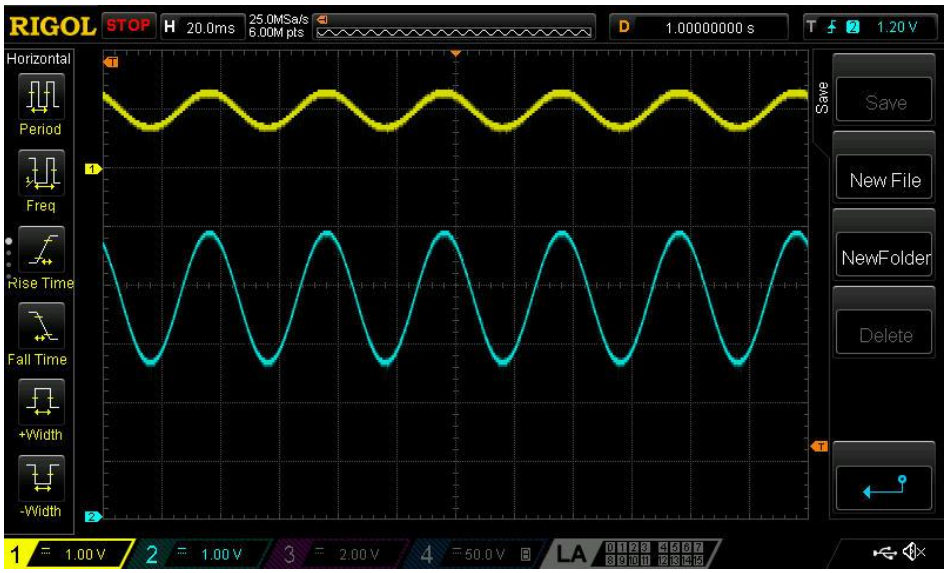

Figure 5. Design condition after Gain timing

As shown in Figure 5, when the gain of OpAmp0 is increased, the initial offset of the input signal also increases, which must then be reduced by switching to the offset trimming mode and increasing the offset compensation voltage using the encoder (Figure 6).

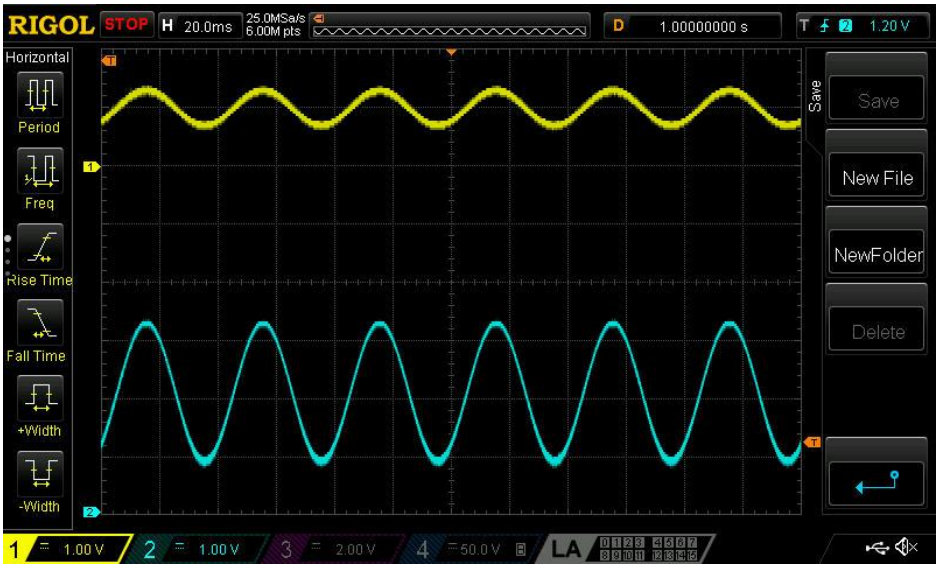

Figure 6. Design condition after Offset compensation trimming (in range)

5. Conclusion

As described in this Application Note, thanks to the convenient control and visualization features of the Go Configure Software Hub, the presented design is perfectly suitable for studying and mastering the basics and principles of analog logic using Renesas' AnalogPAK.

6. Revision History

Revision	Date	Description
1.00	September 10, 2024	Initial release

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