

Sinewave Generator with AnalogPAK SLG47003V

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1. References

For related documents and software, please visit:

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Download our free Go Configure Software Hub [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

- [1] [Go Configure Software Hub](#), Software Download and User Guide, Renesas Electronics
- [2] [AN-CM-386 Sinewave Generator with AnalogPAK](#), Design File, Renesas Electronics
- [3] [GreenPAK Development Tools](#), GreenPAK Development Tools Webpage, Renesas Electronics
- [4] [GreenPAK Application Notes](#), GreenPAK Application Notes, Renesas Electronics
- [5] SLG47003V Datasheet

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2. Terms and Definitions

EPG	Extended Pattern Generator
MF	Multi-Function Macrocell
OpAmp	Operational Amplifier
Vref	Voltage reference

3. Introduction

This design is developed to be an analog sine wave source that can be used in a variety of devices which might require a sinewave reference, for example a stand-alone, hybrid solar DC/AC converter. Also, because of the availability of the Extended Pattern Generator (EPG) it is possible to specify other waveforms (rectangular, triangular, and trapezoidal). In this Application Note is we will consider the use of a sinusoidal waveform, since this waveform is perhaps the most common.

The generation of a sinusoidal signal occurs by means of a cyclic recording of data from the EPG to the rheostat (RH0), which is included on the low side of the voltage divider R3-RH0 (see Figure 1 and Figure 2).

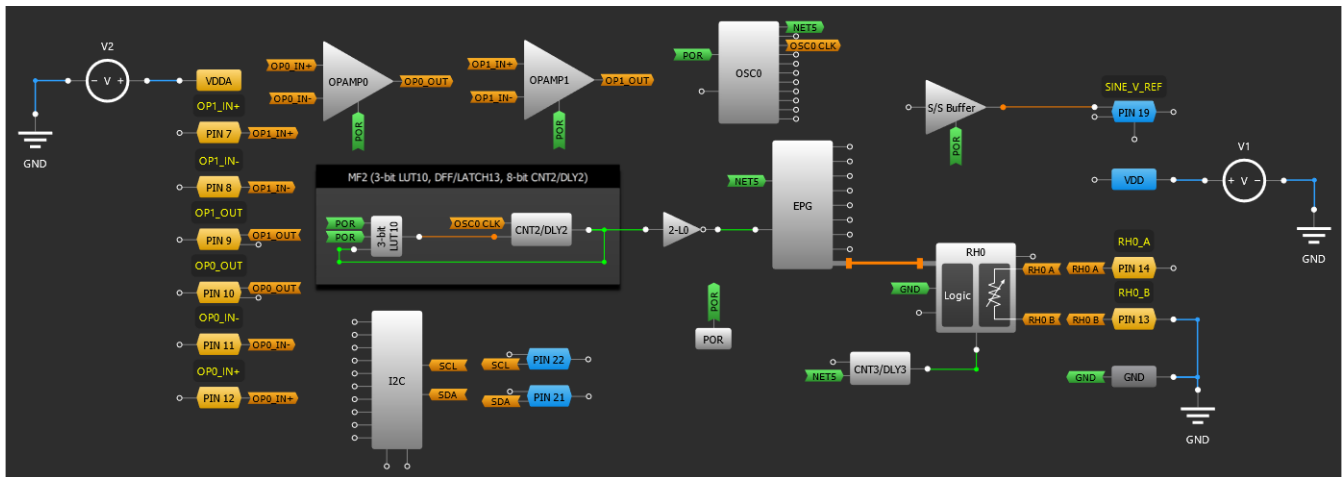


Figure 1. Sinewave Generator Design Block Diagram

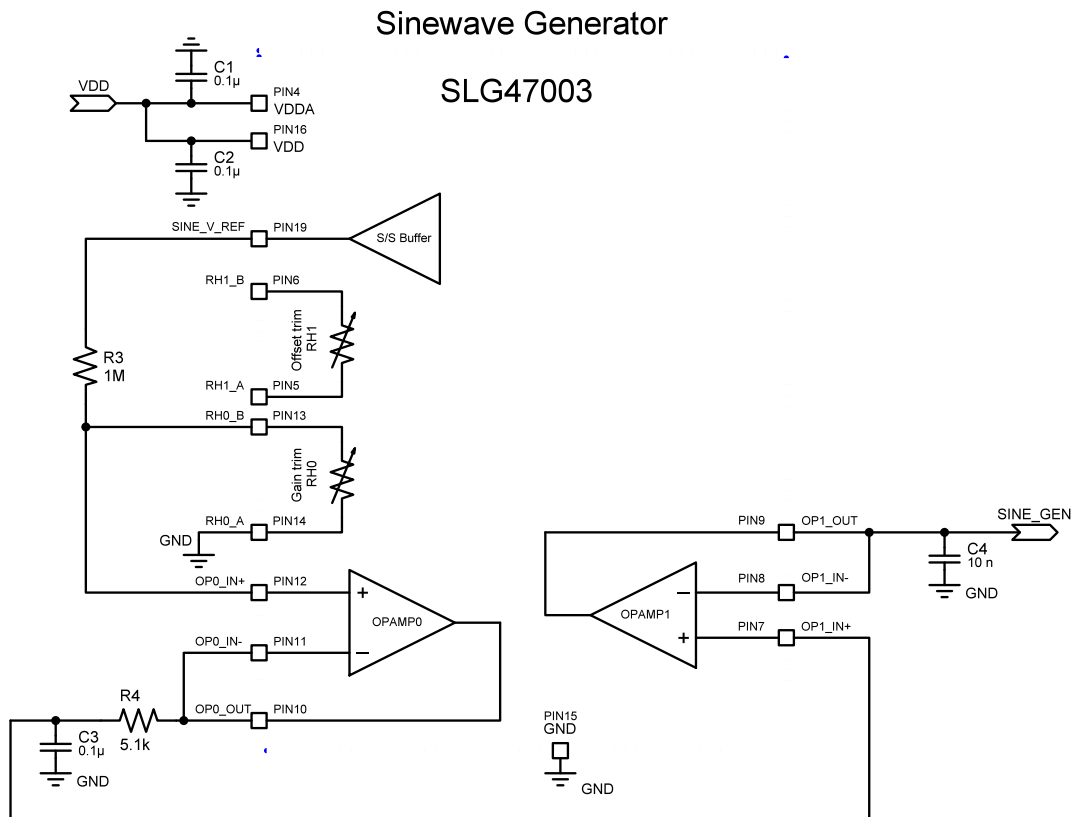


Figure 2. Sinewave Generator Typical Application Circuit

4. Design Operation

The operation of the signal generator is based on the ability to control the rheostat (RH0) by writing data to its counter from the EPG via an 8-bit parallel output (a new function implemented in AnalogPAK).

56 values that determine the shape of the output signal (sinusoidal) are recorded in the EPG memory (see [Figure 3](#) and [Figure 4](#)).

ID (dec)	[OUT7:OUT0]	Value (hex)	Value (dec)
0	1 0 0 0 0 0 0 0	0x80	128
1	1 0 0 0 1 1 1 0	0x8E	142
2	1 0 0 1 1 1 0 0	0x9C	156
3	1 0 1 0 1 0 1 0	0xAA	170
4	1 0 1 1 0 1 1 1	0xB7	183
5	1 1 0 0 0 0 1 1	0xC3	195
6	1 1 0 0 1 1 1 1	0xCF	207
7	1 1 0 1 1 0 1 0	0xDA	218
8	1 1 1 0 0 0 1 1	0xE3	227
9	1 1 1 0 1 0 1 1	0xEB	235
10	1 1 1 1 0 0 1 0	0xF2	242
11	1 1 1 1 1 0 0 0	0xF8	248
12	1 1 1 1 1 1 0 0	0xFC	252
13	1 1 1 1 1 1 1 0	0xFE	254
14	1 1 1 1 1 1 1 1	0xFF	255
15	1 1 1 1 1 1 1 0	0xFE	254
16	1 1 1 1 1 1 0 0	0xFC	252
17	1 1 1 1 1 0 0 0	0xF8	248
18	1 1 1 1 0 0 1 0	0xF2	242
19	1 1 1 0 1 0 1 1	0xEB	235
20	1 1 1 0 0 0 1 1	0xE3	227
21	1 1 0 1 1 0 1 0	0xDA	218
22	1 1 0 0 1 1 1 1	0xCF	207
23	1 1 0 0 0 0 1 1	0xC3	195
24	1 0 1 1 0 1 1 1	0xB7	183
25	1 0 1 0 1 0 1 0	0xAA	170
26	1 0 0 1 1 1 0 0	0x9C	156
27	1 0 0 0 1 1 1 0	0x8E	142

Figure 3. PGA Data Table for Values 0 to 27

ID (dec)	[OUT7:OUT0]	Value (hex)	Value (dec)
28	1 0 0 0 0 0 0 0	0x80	128
29	0 1 1 1 0 0 0 1	0x71	113
30	0 1 1 0 0 0 1 1	0x63	99
31	0 1 0 1 0 1 0 1	0x55	85
32	0 1 0 0 1 0 0 0	0x48	72
33	0 0 1 1 1 1 0 0	0x3C	60
34	0 0 1 1 0 0 0 0	0x30	48
35	0 0 1 0 0 1 0 1	0x25	37
36	0 0 0 1 1 1 0 0	0x1C	28
37	0 0 0 1 0 1 0 0	0x14	20
38	0 0 0 0 1 1 0 1	0x0D	13
39	0 0 0 0 0 1 1 1	0x07	7
40	0 0 0 0 0 0 1 1	0x03	3
41	0 0 0 0 0 0 0 1	0x01	1
42	0 0 0 0 0 0 0 0	0x00	0
43	0 0 0 0 0 0 0 1	0x01	1
44	0 0 0 0 0 0 1 1	0x03	3
45	0 0 0 0 0 1 1 1	0x07	7
46	0 0 0 0 1 1 0 1	0x0D	13
47	0 0 0 1 0 1 0 0	0x14	20
48	0 0 0 1 1 1 0 0	0x1C	28
49	0 0 1 0 0 1 0 1	0x25	37
50	0 0 1 1 0 0 0 0	0x30	48
51	0 0 1 1 1 1 0 0	0x3C	60
52	0 1 0 0 1 0 0 0	0x48	72
53	0 1 0 1 0 1 0 1	0x55	85
54	0 1 1 0 0 0 1 1	0x63	99
55	0 1 1 1 0 0 0 1	0x71	113

Figure 4. PGA Data Table for Values 28 to 55

Since the rheostat RH0 is included in the low side of the R3-RH0 voltage divider at the non-inverting input of the buffer on OpAmp0, the resistance of RH0 will determine the shape and offset of the output voltage of the buffer relative to the ground.

The maximum value of the amplitude of the output sinusoidal signal is determined by the value of the output voltage of the S/S Buffer macrocell and the resistance of R3 on the high side of the voltage divider R3-RH0 (see Figure 2).

Thanks to the new method of signal formation from the EPG using the patterns set in advance, the output sinusoidal signal does not contain significant noise, higher-order harmonics, etc. Additionally, for the final processing of the signal, a second-order filter R4C3, with a voltage follower on OpAmp1 is used (see Figure 2 and Figure 5).

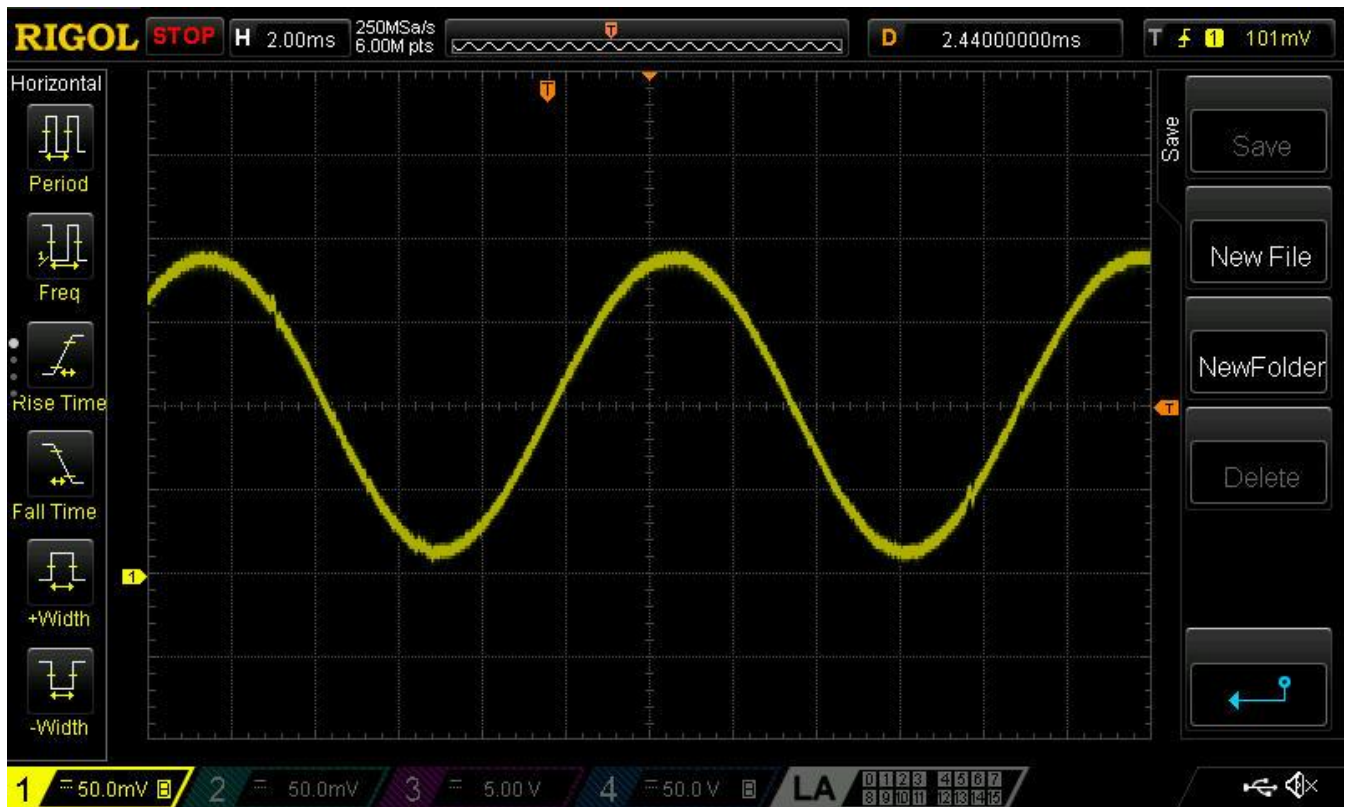


Figure 5. The Main Design Functionality

In addition, if the circuit is updated as shown in [Figure 6](#), R3 can be used to adjust the amplitude and R5 can be used to adjust the offset of the output signal. I²C commands can also set the maximum amplitude of the output signal (the output voltage of the S/S Buffer macrocell) and the output voltage frequency (the oscillator frequency and counter data of the DLY2 macrocell).

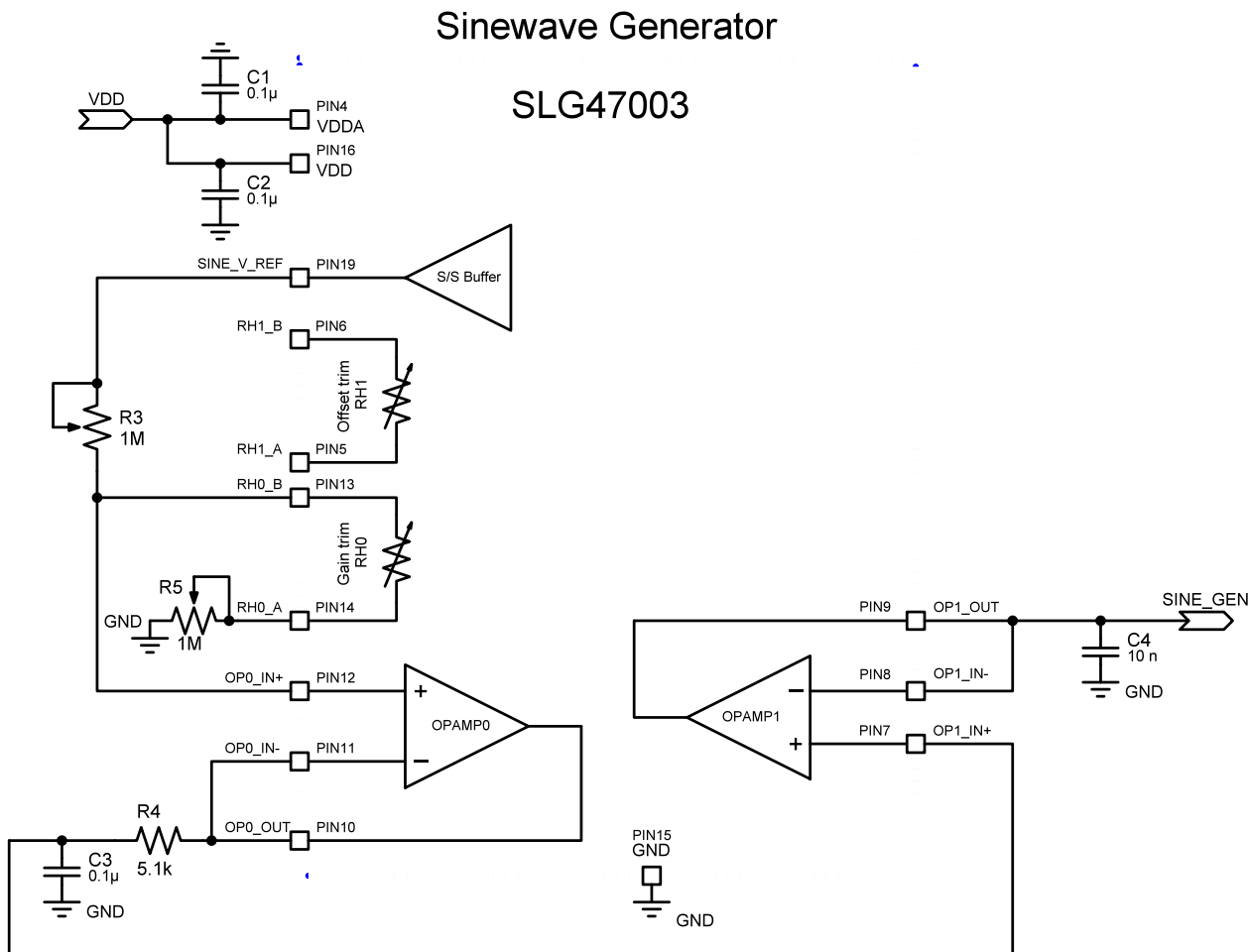


Figure 6. Updated Sinewave Generator typical Application Circuit

5. Conclusion

New functions introduced in AnalogPAK SLG47003 make it possible to create a universal signal generator (sinusoidal, rectangular, triangular, trapezoidal, etc.) with the help of a trivial amount of resources with the opportunity to adjust the frequency, amplitude, and offset using I²C commands and other additional external elements.

6. Revision History

Revision	Date	Description
1.00	September 10, 2024	Initial release.

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