# Dot/Bar Display Driver using SLG47011
# SLG47011

This application note describes how to design and build a Dot/Bar Display Driver, which drives 12 (up to 13) LEDs providing a linear, logarithmic, or any other type of analog display.

The device is built on the SLG47011. The IC is equipped with the PGA (gain up to 64x), 14-bit ADC (12-bit mode is used in this case), Data Buffers (used to average measurements), Memory Table (used to convert ADC data to data required for the specific display type) and Width Converter which forms the output signal. In addition, the SLG47011 contains a huge amount of different macrocells, allowing almost any additional function to be added.

The application note comes complete with a design file that can be found in the Reference section.

## Contents

# 1. Terms and Definitions

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| CNT/DLY | Counter-Delay |
| CLK | Clock |
| DAC | Digital to Analog Converter |
| DCMP | Digital Comparator |
| DFF | D-Flip-Flop |
| GPIO | General-purpose Input/Output |
| IC | Integrated Circuit |
| LED | Light Emitting Diode |
| LSB | Least-significant Bit |
| LUT | Look Up Table |
| MUX | Multiplexer |
| NVM | Non-volatile Memory |
| OSC | Oscillator |
| PGA | Programable Gain Amplifier |
| PWM | Pulse-width Modulation |
| RAM | Random-access Memory |
| ROM | Read-only Memory |
| WCN | Width Converter |

# 2. References

For related documents and software, please visit:

AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the *.aap files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-396 Dot/Bar Display Driver, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

*Author: Nazar Sliunchenko, Technical Documentation Manager, Renesas Electronics*

# 3. Introduction

The device described in this document is a circuit that senses analog voltage levels and drives up to 13 LEDs, providing a linear, logarithmic, or any other type of analog dot/bar display. It contains an internal voltage reference of 1.62 V. The input signal goes through the PGA providing a very high input impedance and user-selectable gain of 1x, 2x, 4x, 8x, 16x, 32x, and 64x. This allows for a high flexibility of the design.

The applications of a linear display include voltage, temperature (using a built-in temp sensor) indicator, or indication of the voltage from any analog sensor.

Audio (logarithmic display) applications include average or peak level indicators and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

See Figure 1 for the block diagram and Figure 2 for the circuit diagram of the device.

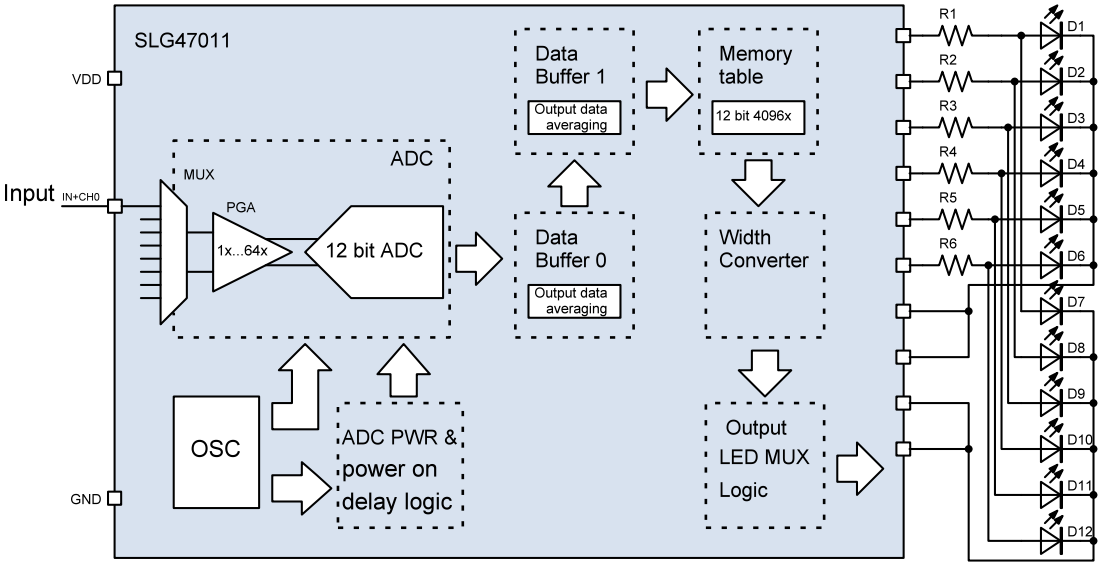


**Figure 1: Block Diagram of the Dot/Bar Display**

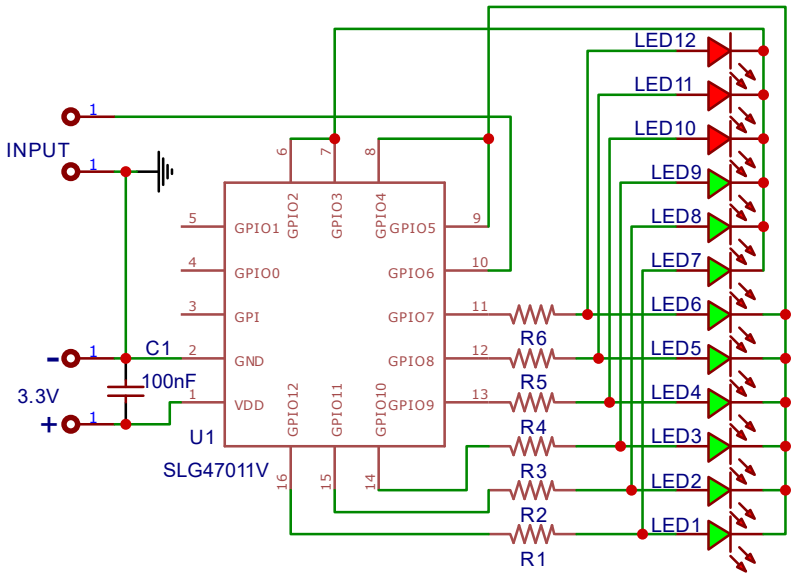


**Figure 2: Block Diagram of the Dot/Bar Display**

# 4. Theory of Operation

The SLG47011 has a collection of internal macro cells that allow the creation of a circuit that senses analog voltage levels and drives up to 13 LEDs, providing a linear, logarithmic, or any other type of analog dot/bar display.

## 4.1 Programmable Gain Amplifier

The input signal goes through the PGA. It has a 7-bit gain selection. Possible gain settings are 2x, 4x, 8x, 16x, 32x, 64x. It is also possible to bypass the PGA and measure signals directly with ADC or use it as a high input impedance buffer with 1x gain. The PGA is rail-to-rail input and output and has a variety of different modes and settings. But in this project, only one of four channels is used. It is set to Single-ended input buffer mode.

## 4.2 Analog-to-Digital Converter

The SLG47011 has a successive approximation Analog-to-Digital Converter (SAR ADC) macrocell with a configurable resolution of 14-bit, 12-bit, 10-bit, and 8-bit (12-bit mode is used in this project). It has an internal Sampling Engine block that switches input analog MUX and controls the ADC data receivers (Data Buffers or Memory Table macrocell). ADC can sample up to four logical channels. Each logical channel is configured to operate with any possible analog input.

ADC data destination options are:

- Data Buffers (Data Buffer 0 to Data Buffer 1 option used in this project)
- Address input of Memory Table macrocell (ROM mode used in this project)
- Data input of Memory Table macrocell (RAM mode)
- MathCore inputs
- Internal one-word buffer accessible via I²C/SPI Host interface

ADC voltage reference sources are:

- External source (GPIO11)
- Internal reference 1.62 V (used in this project)
- AVDD divider.

ADC clock sources are:

- Internal OSC 20/40 MHz (20 MHz used in this project)
- External clock from matrix
- Configurable clock divider (/16 divider is used in this project)

## 4.3 Counter Delay (CNT/DLY)

This design uses two CNT/DLYs each part of a separate Multifunction Macrocell. CNT3/DLY3 makes a 20 ms ADC power-on delay to ensure its proper start-up initialization. CNT2/DLY2 creates a 40 ms delayed High-level signal that starts the conversion. This technique ensures accurate measurements in a variable environment.

## 4.4 Data Buffers

The SLG47011 has four Data Buffers (two used in this project) designed to store or process data from the ADC, Math Core, or CNT/DLY. In this project, the input sources for Data Buffers are:

- Data Buffer 0 – ADC Data
- Data Buffer 1 – Data Buffer 0 (daisy chain with Data Buffer 0)

The user can select Data Buffer length 1, 2, 4, or 8 words, as well as the initial data of Data Buffers (0000h or FFFFh).

The basic modes for Data Buffer are:

- Storage mode
- Moving Average mode (used in this project)
- Oversampling mode

In Moving Average mode, the number of samples, N, are taken from the Data Buffer DATA, added together, and the result is divided by N and written to the Buffer Result. The result is updated after each new data is loaded to the Data Buffer. This feature allows for eliminating noise in the measured signal.

## 4.5 Memory Table

The Memory Table macrocell is a memory block that consists of 4096 12-bit words. It has 12-bit address and a 12-bit data port. The address of each particular word comes from the address input, and its content is available after some propagation delay and access time at the output. Memory Table can work in two modes: read-only memory (ROM; data in which is taken from NVM at chip startup) and randomized access memory (RAM; works as a storage block). Data in all modes can be rewritten via the I²C or SPI interfaces.

The address input source for the Memory Table can be selected from:

- Data Buffer0
- Data Buffer1 (used in this project)
- Internal counter (must be selected when operating in RAM mode only)
- ADC channels 0 to 3
- Memory control counter
- I²C/SPI host interface.

The data input source can be selected from:

- Data Buffer 0
- ADC channels 0 to 3
- NVM (used in this project)
- I²C/SPI host interface

Data output can be sourced to:

- DAC
- PWM
- CNT/DLY 9
- MathCore DCMP
- Width Converter (used in this project)

In this design, the Memory Table is set to ROM mode in which data from Data Buffer 1 is converted to the Memory Table address. Output data of the Memory Table will be the contents of the pre-written addressed cell.

## 4.6 Width Converter

The SLG47011 has one 12-bit Width Converter (WCN) macrocell designed to provide data from the Memory Table macrocell to the connection matrix. The macrocell takes 12-bit data from the Memory Parallel Output. The Width Converter clock is synchronized with the 12-bit Memory Control CNT block using the internal block Sync, which is a frequency divider. The width Converter's initial value is defined by the register (in this project it is 0). This value appears at the output of the macrocell after the power-up and after applying a low level at the Reset input of Memory Control CNT. If the memory control counter is configured in two ranges mode, then the Width Converter initial value for the first and second ranges is configured separately. The clock input of the memory control CNT and the clock input of the Width Converter are shared and connected to the same matrix output. When the Width Converter is enabled, the clock for the memory control CNT comes from the Width Converter. When WCN is disabled the clock from the memory control CNT comes directly to the CLK input of the memory control CNT. The basic modes for the Width Converter are as follows:

- 12-to-12 mode (12-bit parallel output, used in this project)
- 12-to-4 mode (12-bit word to three 4-bit words)
- 12-to-2 mode (12-bit word to six 2-bit words)
- 12-to-1 mode (12-bit word to serial bit stream).

If the memory control counter works with the WCN, the maximal clock frequency of the memory control counter is the following:

- If WCN is turned on with 12-to-12 mode, maximum CLK frequency is 20 MHz.
- If WCN is turned on with 12-to-4, 12-to-2, 12-to-1 mode, maximum CLK frequency is 40 MHz. A maximum clock frequency of 40 MHz is guaranteed.

In 12-to-12 mode Width Converter converts data from memory to 12 parallel outputs, as shown in Figure 3.

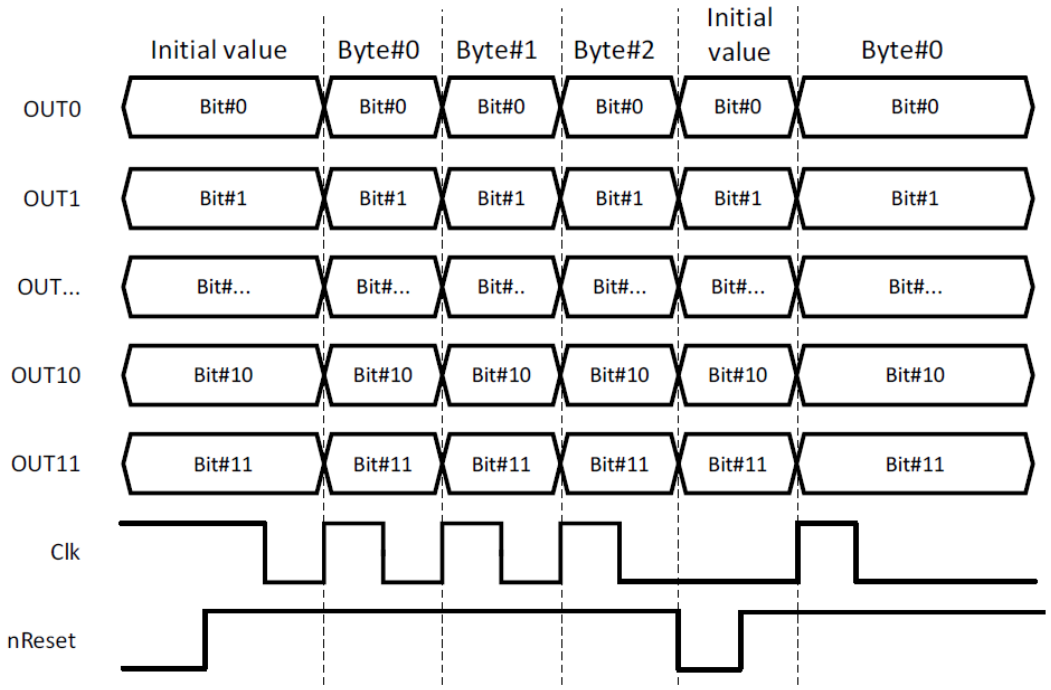


**Figure 3: Width Converter in 12-to-12 Mode Output Waveforms**

## 4.7 LUTs and DFF

Each Width Converter's output goes to 6 LUTs configured multiplexers. This allows using only 6 pins to drive 12 LEDs instead of 12. Also, two pairs of pins connected in parallel are used as a common output for each of the 6

LED cathodes. This increases the loading capability eliminating the need for external transistors. Since those two common outputs must alternate, one of them must receive an inverted clock signal. 2-bit LUT1 configured as an inverter serves the purpose.

The DFF 14 serves as an additional clock divider and ensures a 50% duty cycle for the MUXs and common outputs. It sources its clock from the Memory Table Data ready output.

## 4.8 Oscillators

There are two oscillators within the SLG47011, but only one is used in this project. OSC1 is set to 20 MHz with predivider 4 and is used as a CNT clock as well as an ADC clock with its own divider set to 2.

# 5. Go Configure Software Hub Project

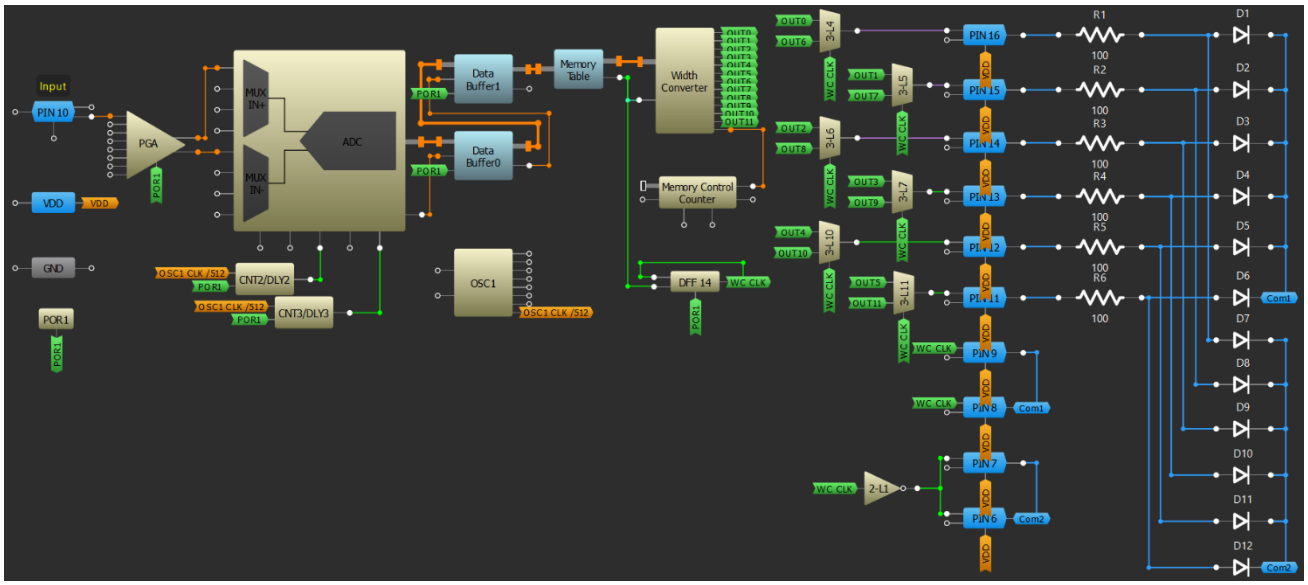


**Figure 4: Dot/Bar Display Driver, Go Configure Software Hub Screenshot**

All programming, configurations, and settings are made using the Go Configure Software Hub via the graphical user interface (GUI), see Figure 4. So, no programming skills are required. The whole process comes down to configuring the macrocells. For the specific function of each macrocell refer to section 3. Theory of Operation.

## 5.1 PIN Configuration

All pins used in this design are configured as Digital Output 1x push-pull except for PIN 10, which serves as signal input, so it must be configured as Analog input/output.

## 5.2 PGA Configuration

Output+ to PIN 13 (GPIO9) – Disable

Output- to PIN 14 (GPIO10) – Disable

PGA/ADC manual mode enable – Disable

Manual channel selection – Channel 0

**Table 1. Channel Configuration**

| Setting | Channel 0 | Channel 1 | Channel 2 | Channel 3 |
|---|---|---|---|---|
| Input mode | Single ended input | Disable | Disable | Disable |
| Mode | Buffer | PGA bypass | PGA bypass | PGA bypass |
| Gain | 1x | - | - | - |
| IN+ source | PIN 10 (GPIO6) | GND (PIN 2) | GND (PIN 2) | GND (PIN 2) |
| IN- source | AGND | AGND | AGND | AGND |

## 5.3 ADC Configuration

Clock selection – OSC1

Vref selection – 1.62 V internal Vref

Resolution – 12-bit

Sample per channel – 8

Channel 0 system calibration – Disable

Channel 2 system calibration – Disable

Clock divider – /2

Delay between channels – 1

Delay between channels predivider – 1

Data alignment – LSB

All other settings should be left by default.

## 5.4 CNT/DLY Configuration

Both CNT/DLYs used in this design are set to Dalay mode, Rising edge mode, Clock source – OSC1/512, Counter data 390 (40 ms) for CNT2/DLY2 and 195 (20 ms) for CNT3/DLY3. All other settings are by default.

## 5.5 Data Buffers Configuration

**Table 2. Data Buffers Configuration**

| Setting | Buffer 0 | Buffer 1 |
|---|---|---|
| Mode | Moving Average | Moving Average |
| Length | 8 words | 8 words |
| Initial data | 0000h | 0000h |
| Input source | ADC | Buffer 0 OUT |
| Load source | ADC ready 0 | Buffer 0 Ready |
| Load en sync | ADC clk | No sync |
| OUT sourse | Result | Result |
| Buffer ready | 8 | 8 |

## 5.6 Memory Table Configuration

Mode – ROM

Address source select – Buffer 1

Table size – 4095, Memory truncate – LSB

Skip NVM load memory – No skip

Initial value – Disable

However, in order to function as intended, the Memory Table must be preloaded with specific data to an address sourced from Buffer 1. This is to convert 12-bit buffered ADC data for the With Converter so it can properly output information via the LED bar/dot display, see Table 3 for linear scale display and Table 4 for audio VU meter (logarithmic scale display).

**Table 3. Linear Display Memory Table Data**

| Input Voltage, V | ADC Data, bit | Memory Table Word for Bar Display, hex | Memory Table Word for Dot Display, hex |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0.125 | 316 | 1 | 1 |
| 0.249 | 629 | 3 | 2 |
| 0.374 | 945 | 7 | 4 |
| 0.498 | 1259 | F | 8 |
| 0.623 | 1575 | 1F | 10 |
| 0.748 | 1891 | 3F | 20 |
| 0.872 | 2204 | 7F | 40 |
| 0.997 | 2520 | FF | 80 |
| 1.122 | 2836 | 1FF | 100 |
| 1.246 | 3150 | 3FF | 200 |
| 1.371 | 3466 | 7FF | 400 |
| 1.495 | 3779 | FFF | 800 |
| 1.620 | 4096 | FFF | 0 |

**Table 4. Audio VU Meter Memory Table Data**

| Input Level (dBu), dB | Input Voltage, V | ADC Data, bit | Memory Table Word for Bar Display, hex | Memory Table Word for Dot Display, hex |
|---|---|---|---|---|
| -∞ | 0 | 0 | 0 | 0 |
| -20 | 0.078 | 197 | 1 | 1 |
| -12 | 0.195 | 493 | 3 | 2 |
| -9 | 0.275 | 695 | 7 | 4 |
| -6 | 0.388 | 981 | F | 8 |
| -4 | 0.489 | 1236 | 1F | 10 |

| | | | | |
|---|---|---|---|---|
| -2 | 0.615 | 1555 | 3F | 20 |
| -1 | 0.690 | 1744 | 7F | 40 |
| 0 | 0.775 | 1959 | FF | 80 |
| 1 | 0.869 | 2197 | 1FF | 100 |
| 2 | 0.975 | 2465 | 3FF | 200 |
| 3 | 1.094 | 2765 | 7FF | 400 |
| 4 | 1.228 | 3104 | FFF | 800 |
| Over 4 | 1.620 | 4096 | FFF | 0 |

After loading the data, the Memory Table Editor should display the following, see Figure 5 and Figure 6.

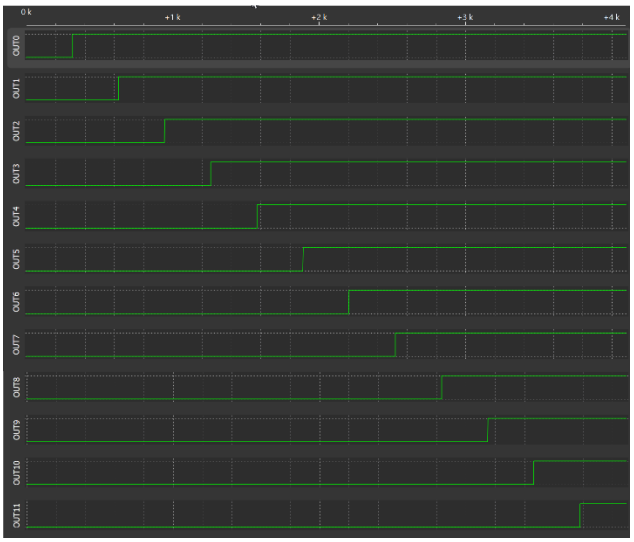

**Figure 5: Bar Display Memory Table Editor Screenshot**

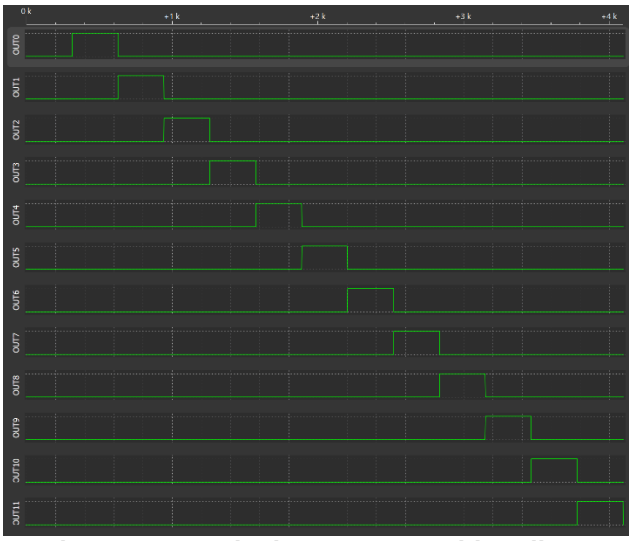

**Figure 6: Dot Display Memory Table Editor Screenshot**

## 5.7 LUT and DFF Configuration

3-bit LUTs 4, 5, 6, 7, 10, and 11 are configured as MUX. 2-bit LUT1 serves as an inverter and 3-bit LUT12 is reconfigured as DFF (DFF 14) with inverted output.

## 5.8 Memory Control Counter

Memory Control Counter is tied up to the Width Converter but it is not used in this project.

## 5.9 Connecting LEDs

As can be seen from Figures 1, 2, and 4, the 12 LEDs are connected directly to the IC's outputs through current limiting resistors. This has its pros and cons. Pros – no external switches, cons – limited loading capability. From the datasheet, we know the maximum average or DC current through PIN cannot exceed 8 mA. So, the current through the common cathode PINs 6 through 9 must be considered. Since there are two outputs connected in parallel for each common cathode, the current can be doubled and since the duty cycle is 50%, the current can be doubled again resulting in 32 mA per common cathode output. Each common cathode output drives 6 LEDs, 5 mA for each LED in bar mode, and up to 32 mA in dot mode display.

# 6. Upgrading the Design to 13 LEDs

Some real-life applications might require a 13 LED bar/dot indicator. In this case, the design can be modified by using an ACMP to sense voltage above ADC's Vref (1.62 V), see Figure 7.

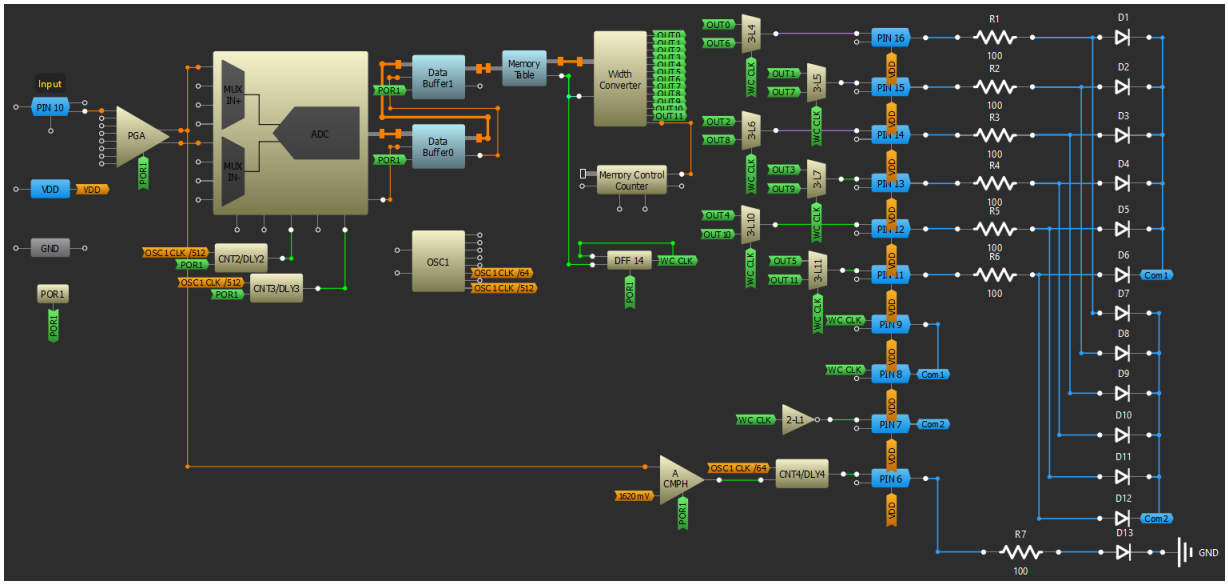


**Figure 7: 13 LED Dot/Bar Display Driver, Go Configure Software Hab Screenshot**

The ACMP input sources are:

IN+ – PGA OUT

IN- – 1620 mV

The rest of the settings are by default.

There also must be a delay after the ACMP to prevent the 13th LED from fading out quicker than it can be observed. The CNT4/DLY4 serves this purpose. It is set to Delay mode, Counter data 3906 (50 ms), falling edge mode. All other settings are by default.

This design modification has a downside, as it uses one of the pins that was used for common cathodes (Com2). This will reduce the output current by half (current limiting resistors must be doubled in value). So, there might be a need for an external switch if 2.5 mA per LED is not enough.

# 7. Design Simulation

The design described in section 4 can be simulated using the Simulation Software within the Go Configure Software Hub. However, some modifications should be made. The ground node and signal sources (V1 and V2) must be added for the simulation to function properly. V1 must be set to 3.3 V with a minimum 1 ms ramp. For V2 settings see Figure 8. The probes are connected to both V1 and V2 and all Width Converter outputs. See the screenshot of the modified design in Figure 9. For the 12 LED Dot Display Driver simulation results see Figure 10.

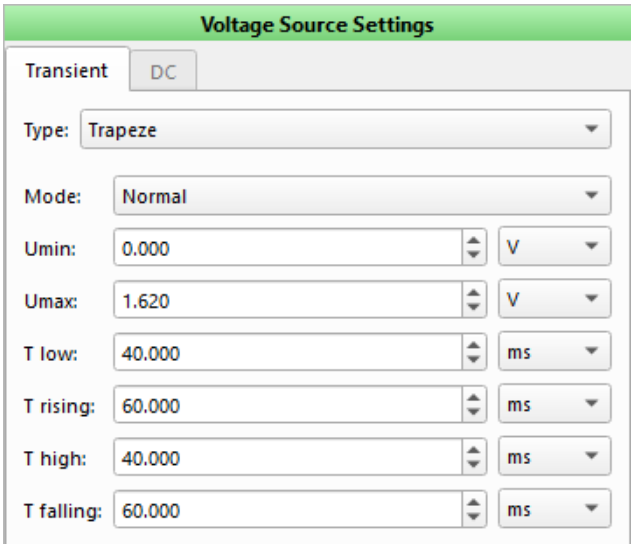


**Figure 8: V2 Voltage Source Settings**

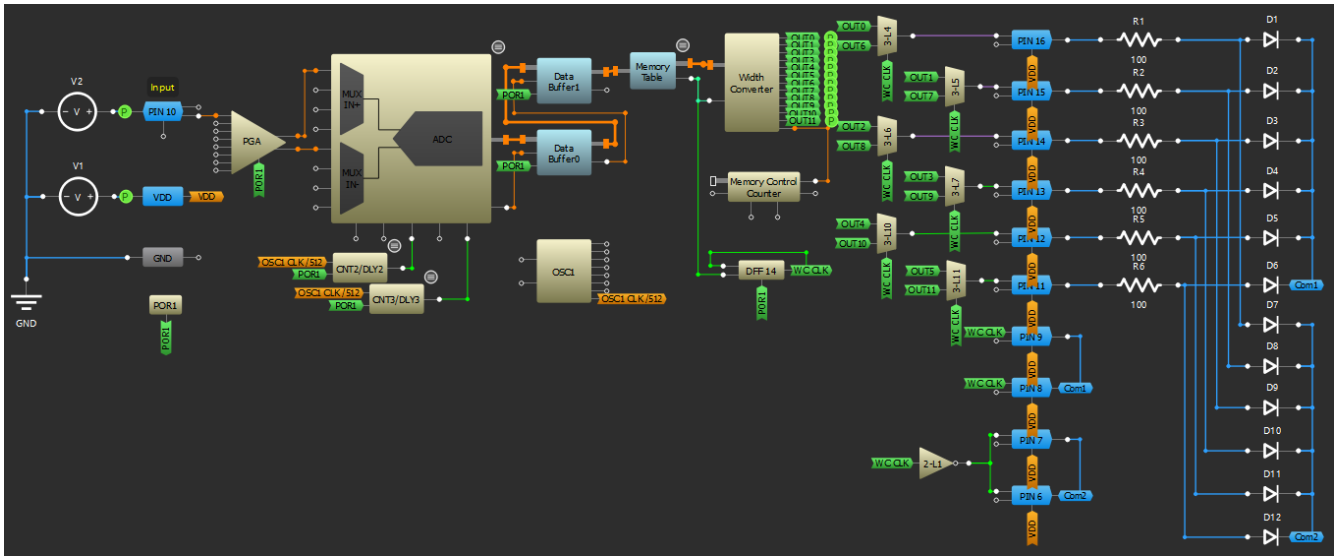


**Figure 9: Simulation Design, Go Configure Software Hub Screenshot**

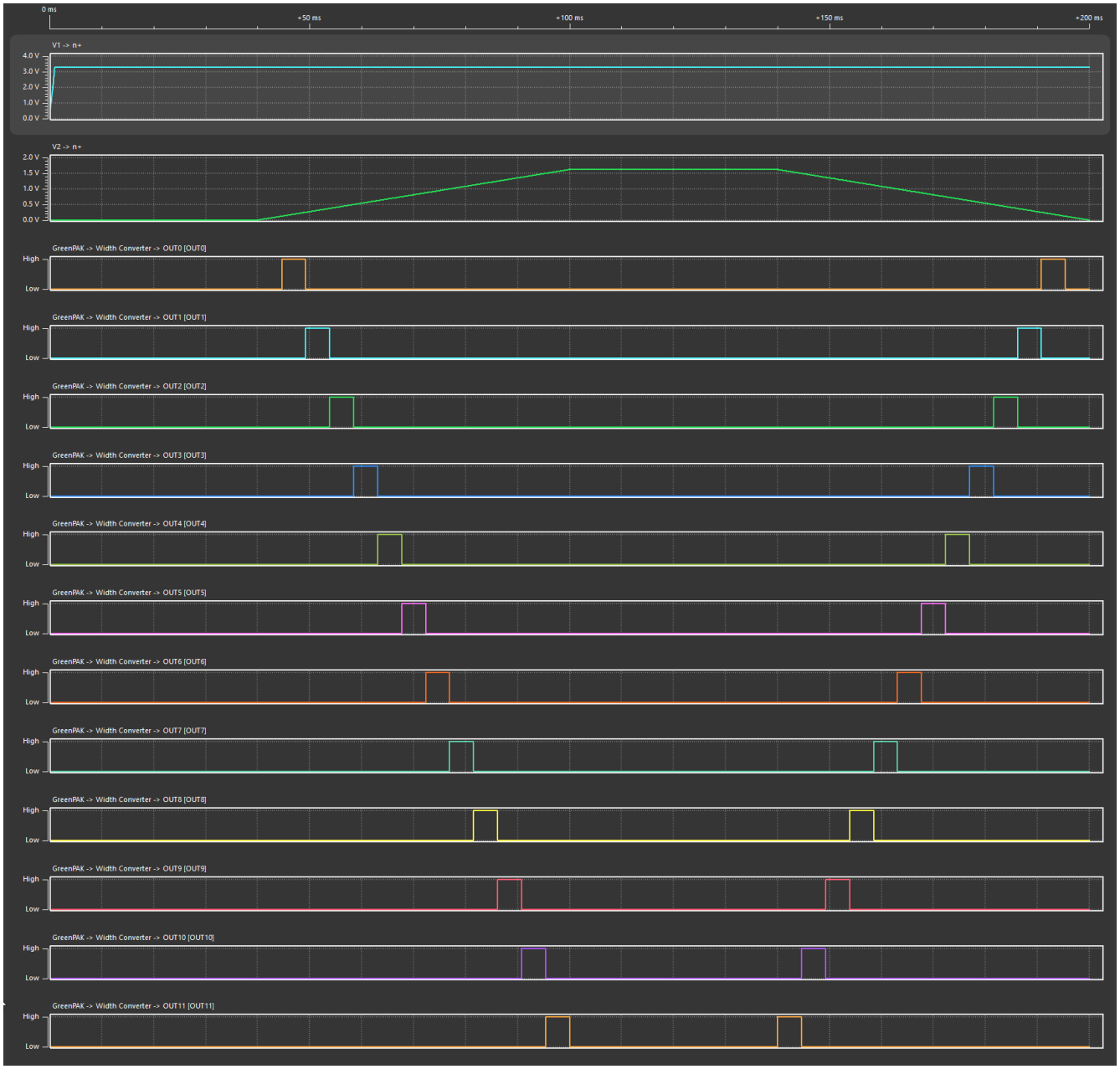


**Figure 10: Simulation Results, Go Configure Software Hub Screenshot**

# 8. Conclusions

The theory behind the design of this circuit does not only apply to voltage indicators and VU meters, but also to field strength indicators, tachometers, level sensors, and other related instruments and equipment with linear, logarithmic, or any other scale type. When used for VU meter applications, the audio power levels in broadcast studios and recording are measured to determine the right amount of attenuation or amplification of signals for optimal outcomes.

In addition, the SLG47011 contains a huge amount of different macrocells, allowing almost any additional function to be added. The Go Configure Software Hub makes the designing process easy and fast.

# 9. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | Sep 24, 2024 | Initial release. |

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


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