PT100/1000 RTD Interface
SLG47011

The application note gives step-by-step guidelines for creating a PT100/1000 RTD Interface design using the SLG47011. A unique set of the ADC, DAC Vref Buffer, Data Buffers, and additional internal logic of the SLG47011 is used to achieve the best precision of this analog interface. The application note contains a complete schematic of an analog front end for a PT1000 sensor with noise canceling.

The application note comes complete with design files which can be found in the Reference section.

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1. Terms and Definitions

DFF	D Flip-Flop
GBWP	Gain Bandwidth Product
LUT	Look-up Table
MF	Multi-Function
OSC	Oscillator

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2. References

For related documents and software, please visit:

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Download our free Go Configure Software Hub [1] to open the *.aap files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-397 PT100 PT1000 RTD Interface, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

[5] SLG47011 Datasheet, Renesas Electroncis

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3. Introduction

In the following application note, the AnalogPAK SLG47011 is used as the Signal Conditioner for a PT1000 sensor with noise canceling.

The PT1000 sensor contains a pure platinum element that has a resistance of 1000 ohms at 0°C. Its resistance increases with increasing temperature. The variation of platinum resistance with temperature is quite linear, making the PT1000 very accurate for temperature measurement. The advantage of the PT1000 sensor is its accuracy, stability, and linearity, making it ideal for precision measurements in many applications.

4. Input Parameters

This section shows the specifications of the SLG47011 and PT1000 sensor used in this application note.

SLG47011 Characteristics

Parameter	Possible Value	Value in this Design
V_{DD} Input Range	1.8 V or 3.3 V	3.3 V
ADC	12/14-bit	14-bit
ADC Vref	1.8 V, V_{DD}/2, or 1.62 V	1.62 V

PT1000 Characteristics

Temperature, C	Resistance, Ω
-50	803.1
-40	842.7
-30	882.2
-20	921.6
-10	960.9
0	1000.0
10	1039.0
20	1077.9
30	1116.7
40	1155.4
50	1194.0
60	1232.0
70	1270.0
80	1308.9
90	1347.0
100	1385.0
110	1422.0
120	1460.6
130	1498.2
140	1535.8
150	1573.1

5. Operating Principle

The PT1000 Interface Simplified Block Diagram is shown in Figure 1.

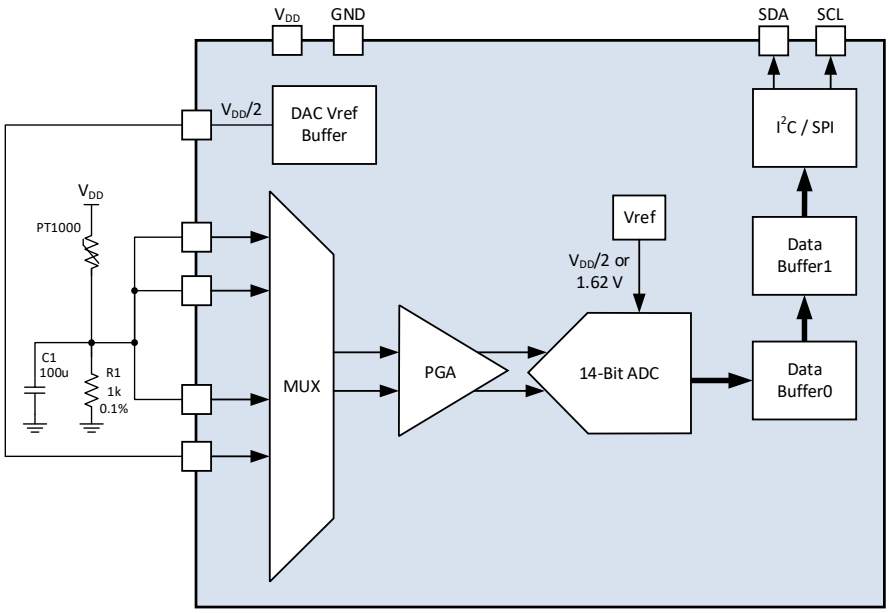

Figure 1. PT1000 Interface Simplified Block Diagram

The resistance of the PT1000 sensor is 1 kΩ at 0°C and it increases with increasing temperature.

Note: it is possible to connect a PT100 sensor: the reference resistor in the divider must be changed to 100 Ohm instead of 1 kOhm.

The PT1000 sensor is connected in series with a 1kΩ ±0.1% resistor forming a resistive voltage divider. The voltage from the divider is supplied to Channel 0 and Channel 1 IN+ of the PGA and ADC. DAC Vref Buffer provides a voltage of VDD/2 and goes to Channel 1 of PGA and ADC with 1x gain.

Channel 0 is used for internal calibration, reducing PGA offset and noise error.

Channel 1 is used for temperature measurement. Since the resistance of the sensor changes with temperature, the measured voltage on the resistive divider also changes. Thus, the ADC output will be the difference between VDD/2 and voltage on the resistive divider.

The resistance versus temperature relationship for PT1000 sensors is standardized and this relationship can be used to convert the measured voltage to a temperature value.

6. AnalogPAK Design

The AnalogPAK Design is shown in Figure 2.

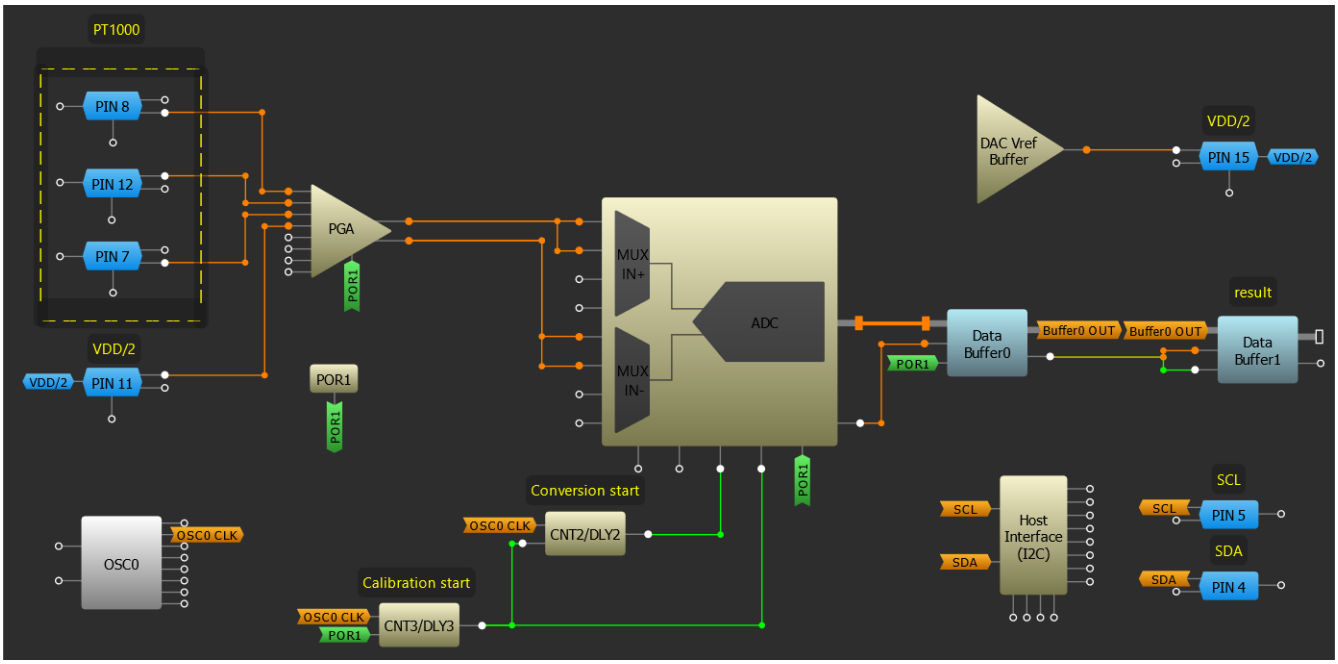

Figure 2. PT1000 Interface AnalogPAK Design

CNT2/DLY2 and CNT3/DLY3 are used to correctly turn on the ADC after the first turn-on when the POR arrives, as well as in further work when turning on and off the ADC. CNT3/DLY3 also ensures the internal calibration process before the conversion has started. CNT3/DLY3 creates a series of pulses that force the ADC to calibrate itself every 800 ms. This technique ensures accurate measurements in a variable environment.

The signal from the PT1000 resistive divider comes to PIN 8, PIN 12, and PIN 7. PIN 12 is connected to PIN 15, which in turn is connected to DAC Vref Buffer with VDD/2 reference voltage.

PIN 8 and PIN 12 are connected to the differential input of the PGA Channel 0 with 1x gain. This channel is used for internal calibration. Internal Calibration procedure is used to measure the ADC offset error and then to subtract (or add it) from the ADC data depending on the error sign. ADC offset error is the deviation between the first ideal code transition and the first actual code transition.

PIN 7 and PIN 12 are connected to the differential input of the PGA Channel 1 with 1x gain. This channel is used for temperature measurement. ADC samples the difference between the signals from PIN 11 and PIN 7 and sends

it to the noise-canceling stage formed by Data Buffer0 and Data Buffer1. These Data Buffers are connected in Daisy Chains and configured as Moving Average Mode.

ADC has a 14-bit resolution and 1.62 V Vref. Also, consider the closed-loop bandwidth (GBWP/Gain) when setting the delay time. See more in datasheet section 3.8 Programmable Gain Amplifier Specifications ([5).

The software window I²C Virtual Inputs allows you to check the Data Buffer0 and Data Buffer1 outs:

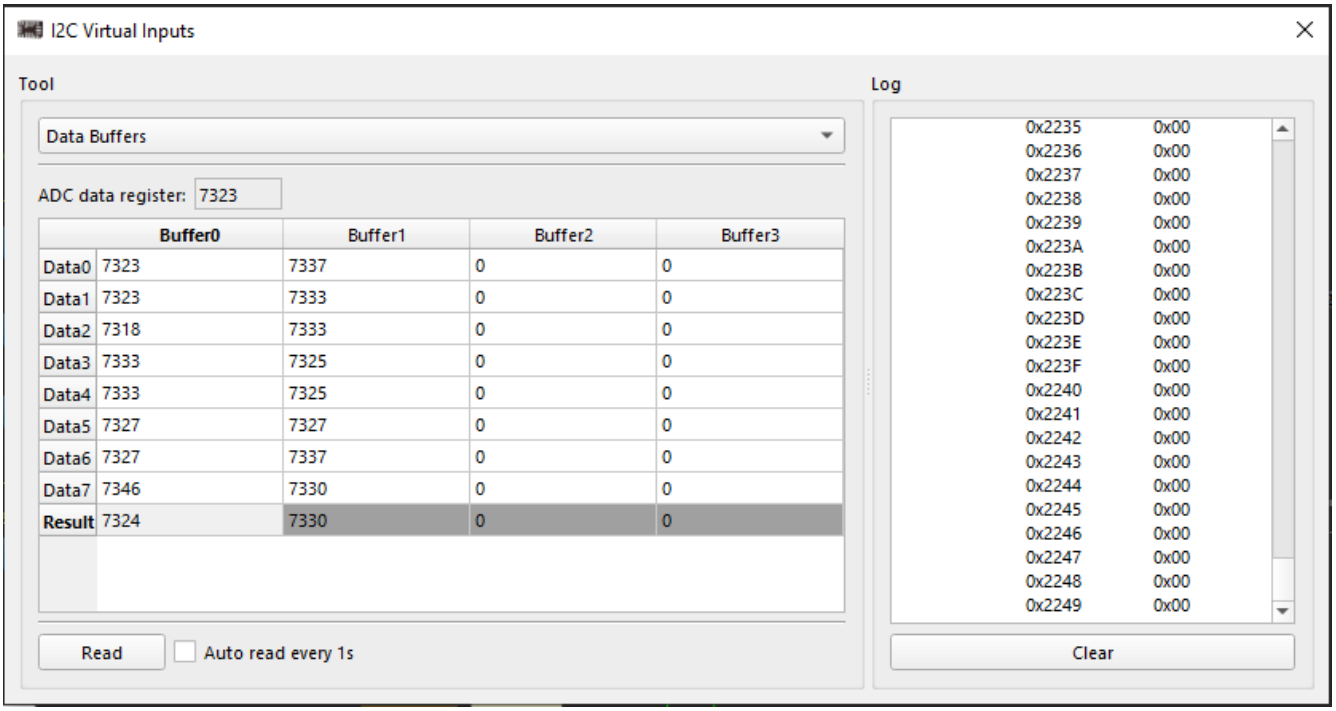

Figure 3. Data Buffers Values

The Data Buffer1 output is the final result, which now should be converted to the temperature.

Firstly, the following formula should be used to convert the decimal code to voltage:

$$ADC\_V_{IN} = (code_{dec} – 8192) * Vref / 16384,$$

where 8192 – middle point of PGA differential input;

Vref = 1.62 V;

16384 – 2^{14}, ADC has a 14-bit resolution.

This ADC_V_{IN} is the voltage between the PT1000 voltage divider and $V_{DD}/2$. Thus, $V_{DD}/2$ should be added to the found voltage to obtain the voltage at the divider node.

$$V_{divider} = ADC\_V_{IN} + V_{DD}/2$$

The PT1000 resistance is calculated using the formula:

$$R_{PT1000} = (V_{DD} – V_{divider}) * 1000\ \Omega / V_{divider}$$

Having a PT1000 sensor resistance, the temperature determination can be easily done with the sensor characteristics table (see section 4. Input Parameters).

7. Test Results

To evaluate the performance of the PT1000 Interface on SLG47011, three measurements were performed for boiling water and room temperatures.

To compare the obtained results, a precision 0.1% accuracy measurement module with the same PT1000 sensor was used.

In all cases, the resistance of the PT1000 sensor was measured and converted into temperature according to the PT1000 Characteristics table in section 4. Input Parameters.

#	SLG47011			Measurement Module	
	Data Buffer1, dec	Resistance, Ohm	Temperature, °C	Resistance, Ohm	Temperature, °C
Boiling water temperature					
1	5529	1379.77	98.6	1380.54	98.8
2	5530	1379.60	98.6	1379.53	98.6
3	5527	1380.11	98.7	1379.86	98.6
Room temperature					
1	7432	1095.43	24.5	1095.31	24.5
2	7430	1095.70	24.6	1095.24	24.5
3	7429	1095.83	24.6	1095.01	24.4

As can be seen from the table above, the PT1000 Interface error on the SLG47011 relative to the measurement module is ±0.2 °C.

8. Conclusion

This application note gives step-by-step guidelines for creating a PT100/1000 Interface design using the SLG47011. A unique set of the ADC, DAC Vref Buffer, Data Buffers, and additional internal logic of the SLG47011 is used to achieve the best precision of this analog interface. The application note contains a complete schematic of an analog front end for a PT1000 sensor with noise canceling.

The variation of platinum resistance with temperature is quite linear, making the PT1000 very accurate for temperature measurement. The PT1000 Interface error on the SLG47011 relative to the measurement module is only ±0.2 °C.

The AnalogPAK's internal resources, including the PGA, ADC, Data Buffers, DAC Vref Buffer, oscillators, logic, and GPIOs are easy to configure to implement the desired functionality for this design.

9. Revision History

Revision	Date	Description
1.00	Sep 24, 2024	Initial release.

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