RX Family

Comparison of the Differences Among the RIICHS Module, the RI3C Module, and the RIIC Module

Introduction

This application note is a reference material for confirming the differences among the following modules: the RIIC and RI3C modules of the RX26T Group, and the RIICHS module of the RX671 Group. The differences covered include general differences and register differences.

Target Devices

RX Family

If you want to use this application note for a device of another family, modify the content according to the specifications of the device and conduct thorough evaluation before use.

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1. Comparison of Differences Between the RIICHS Module and the RIIC Module

1.1 Comparison of General Differences

Table 1.1 shows Comparison of General Differences Between the RIICHS Module and the RIIC Module.

Table 1.1 Comparison of General Differences Between the RIICHS Module and the RIIC Module

Item	RIICHS	RIIC
Communication format	• I²C bus format • System Management Bus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format • System Management Bus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	• I²C bus format — Standard mode (Sm): 0 to 100 kbps — Fast mode (Fm): 0 to 400 kbps — Fast-mode plus (Fm+): 0 to 1 Mbps — High-speed mode (Hs mode): 0 to 3.4 Mbps • System Management Bus format: 10 to 100 kbps	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL is selectable in the range from 4 to 96%.	For master operation, the duty cycle of the SCL is selectable in the range from 4 to 96%.
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Address detection	• Slave address (static address) (a maximum of 3 types) • 7-bit and 10-bit address formats are supported. • General call address • Device ID • Host address • Hs mode master code	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.

Item	RIICHS	RIIC
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL line at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer	• In reception, the following periods of waiting can be obtained by holding the SCL line at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Change timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Change timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RIICHS	RIIC
Arbitration	• For multi-master operation — Operation to synchronize the SCL in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Arbitration loss can be detected when data mismatch occurs during slave transmission.	• For multi-master operation — Operation to synchronize the SCL in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Arbitration loss can be detected when data mismatch occurs during slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL.	The internal timeout function is capable of detecting long-interval stop of the SCL.
Noise cancellation	• Analog noise filter • Digital noise filter	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.

Item	RIICHS	RIIC
Interrupt sources	4 types • Occurrence of a communication error/event interrupt (EEI) — Arbitration loss — NACK detection — Timeout detection — Detection of a start condition (detection of a restart condition included) — Detection of a stop condition • Receive data full interrupt (RXI) • Transmit data empty interrupt (TXI) • Transmit end interrupt (TEI)	4 types • Communication errors/ communication events — Detection of arbitration loss — Detection of NACK — Detection of a timeout — Detection of a start condition (detection of a restart condition included) — Detection of a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
RIIC operating modes	• 4 modes: — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode	• 4 modes: — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode
Event link function (output)	• Occurrence of a communication error/event • Receive data full • Transmit data empty • Transmit end	Four sources (RIIC0): • Occurrence of a communication error/communication event — Detection of arbitration loss — Detection of NACK — Detection of a timeout — Detection of a start condition (detection of a restart condition included) — Detection of a stop condition • Receive data full (slave address match included) • Transmit data empty (slave address match included) • Transmit end

1.2 Comparison of Register Differences

Table 1.2 shows Comparison of Register Differences Between the RIICHS Module and the RIIC Module.

Table 1.2 Comparison of Register Differences Between the RIICHS Module and the RIIC Module

Register	Bit	RIICHS	RIIC
ICCR (RIICHS) ICCR1 (RIIC)	—	Control register Register of the 32-bit length	I²C bus control register 1 Register of the 8-bit length
	SDAI	—	SDA line monitoring bit
	SCLI	—	SCL line monitoring bit
	SDAO	—	SDA output control/monitor bit
	SCLO	—	SCL output control/monitor bit
	SOWP	—	SCLO/SDAO write protect bit
	CLO	—	Additional SCL output bit
	IICRST	—	I²C bus interface internal reset bit
	ICE	Bus interface enable bit (b31)	I²C bus interface enable bit (b7)
ICCR2	—	—	I²C bus control register 2
ICRCR	—	Reset control register	—
ICMMR	—	Operating mode monitor register	—
ICMR1	—	—	I²C bus mode register 1
ICMR2	—	—	I²C bus mode register 2
ICMR3	—	—	I²C bus mode register 3
ICFER	—	Function enable register Register of the 32-bit length	I²C bus function enable register Register of the 8-bit length
	TMOE	—	Timeout function enable bit
	MALE	Master arbitration loss detection enable bit (b0)	Master arbitration loss detection enable bit (b1)
	NALE	NACK transmission arbitration loss detection enable bit (b1)	NACK transmission arbitration loss detection enable bit (b2)
	SALE	Slave arbitration loss detection enable bit (b2)	Slave arbitration loss detection enable bit (b3)
	NACKE	—	NACK reception transfer suspension enable bit
	NFE	—	Digital noise filter enable bit
	SCLE	SCL synchronization enable bit (b8)	SCL synchronization enable bit (b6)
	SMBS	System Management Bus/I2C bus selection bit	—
	FMPE	Fast-mode plus enable bit	—
	HSME	Hs mode enable bit	—
ICSCR	—	Slave mode control register	—
ICRCCR	—	Reference clock control register	—
ICFBR	—	F/S mode bit rate register	—
ICHBR	—	Hs mode bit rate register	—

Register	Bit	RIICHS	RIIC
ICBFTR	—	Bus-free time setting register	—
ICOCR	—	Output signal control register	—
ICICR	—	Input signal control register	—
ICTOR	—	Timeout control register	—
ICACKR	—	Acknowledge bit control register	—
ICCSCR	—	Clock stretch control register	—
ICCGR	—	Condition generation request register	—
ICDR	—	Transmit/receive data register	—
ICSR1	—	—	I²C bus status register 1
ICSR2	—	Status register 2 Register of the 32-bit length	I²C bus status register 2 Register of the 8-bit length
	START	Start condition detection flag (b0)	Start condition detection flag (b2)
	STOP	Stop condition detection flag (b1)	Stop condition detection flag (b3)
	RDRF	—	Receive data full flag
	TEND	Transmission end flag (b8)	Transmission end flag (b6)
	TDRE	—	Transmit data empty flag
	AL	Arbitration loss flag (b18)	Arbitration loss flag (b1)
	TMOF	Timeout detection flag (b20)	Timeout detection flag (b0)
ICSER	—	Status detection enable register Register of the 32-bit length	I²C bus status enable register Register of the 8-bit length
	STDE	Start condition detection enable bit	—
	SPDE	Stop condition detection enable bit	—
	NAKDE	NACK detection enable bit	—
	TEDE	Transmission end detection enable bit	—
	ALE	Arbitration loss detection enable bit	—
	TMOE	Timeout detection enable bit	—
	SAR0E	—	Slave address register 0 enable bit
	SAR1E	—	Slave address register 1 enable bit
	SAR2E	—	Slave address register 2 enable bit
	GCAE	—	General call address enable bit
	DIDE	—	Device ID address detection enable bit
	HOAE	—	Host address enable bit
ICSIER	—	Status interrupt enable register	—
ICCSR	—	Communication status register	—
ICCSER	—	Communication status detection enable register	—
ICCSIER	—	Communication status interrupt enable register	—
ICBSR	—	Bus status register	—
ICSSR	—	Slave mode status register	—

Register	Bit	RIICHS	RIIC
SARy	—	Slave address register y (y = 0 to 2)	—
SARLy	—	—	Slave address register Ly (y = 0 to 2)
SARUy	—	—	Slave address register Uy (y = 0 to 2)
SAMRy	—	Slave address monitor register y (y = 0 to 2)	—
ICBCR	—	Bit count register	—
ICIMR	—	Internal status monitor register	—
ICIER	—	—	I²C bus interrupt enable register
ICBRL	—	—	I²C bus bit rate Low register
ICBRH	—	—	I²C bus bit rate High register
ICDRT	—	—	I²C bus transmit data register
ICDRR	—	—	I²C bus receive data register
ICDRS	—	—	I²C bus shift register

2. Comparison of the Differences Between the RI3C Module and the RIIC Module

2.1 Comparison of General Differences

Table 2.1 shows Comparison of General Differences Between the RI3C Module and the RIIC Module.

Table 2.1 Comparison of General Differences Between the RI3C Module and the RIIC Module

Item	RI3C	RIIC
Operating mode	• Controller mode — Primary controller — Secondary controller • Target mode	• Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode
Data handler (RI3C) Communication format (RIIC)	• Controller: — FIFO buffer transfer • Target: — FIFO buffer transfer	• I^2C bus format • System Management Bus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Communication protocol (RI3C) Transfer rate (RIIC)	• SDR (I3C single data rate) mode — Private message — Broadcast message (common command code (CCC)) — Direct message (common command code (CCC)) • Legacy I^2C message — Fast mode (Fm): 0 to 400 kbps — Fast-mode plus (Fm+): 0 to 1 Mbps	Fast-mode is supported (up to 400 kbps)
IBI	• Target interrupt request (TIR) • Controller role request (CRR) (secondary controller only) • Hot-Join event	—
SCL clock	—	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.

Item	RI3C	RIIC
Issuing and detecting conditions	—	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Address format	7-bit address	7-bit and 10-bit address formats are supported (coexistence of these formats is allowed).
Address detection (RI3C) Slave address (RIIC)	• Target address — Static address — Dynamic address • Broadcast address (7Eh)	• Up to three different slave addresses can be set. • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	—	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Clock stall (RI3C) Wait function (RIIC)	• The I3C bus can be stopped while the SCL line is driven Low.	• In reception, the following periods of waiting can be obtained by holding the SCL line at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	—	Change timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RI3C	RIIC
Arbitration	—	• For multi-master operation — Operation to synchronize the SCL in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Arbitration loss can be detected when data mismatch occurs during slave transmission.
Timeout function	—	The internal timeout function is capable of detecting long-interval stop of the SCL.
Noise cancellation	—	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.

Item	RI3C	RIIC
Interrupt sources	7 types • Response queue full (RESPI) • Command queue empty (CMDI) • IBI queue empty/full (IBII) • Receive status queue full (RCVI) • Receive data full interrupt (RXI) • Transmit data empty interrupt (TXI) • Communication error/ communication event (EEI) — Detection of a start condition (detection of a restart condition included) — Detection of a stop condition — Detection of the HDR exit pattern — Detection of a timeout — Detection of a buffer access error — Abort of a data transfer — Data transfer error	4 types • Receive data full (slave address match included) • Transmit data empty (slave address match included) • Communication error/ communication event — Detection of a start condition (detection of a restart condition included) — Detection of a stop condition — Detection of arbitration loss, — Detection of NACK, — Detection of a timeout, • Transmit end
Low power consumption function	—	Ability to transition to module stop state
Error detection	• Buffer access error • Address header error • Address NACK/dynamic address allocation NACK • Receive overflow error/transmit underflow error • Abort of a transfer • Reception of NACK during an I^2C write data transfer • Timeout error	—

Item	RI3C	RIIC
Event link function (output)	• Occurrence of a communication error/event • Receive data full • Transmit data empty	Four sources (RIIC0): • Occurrence of a communication error/communication event — Detection of arbitration loss, — Detection of NACK — Detection of a timeout — Detection of a start condition (detection of a restart condition included) — Detection of a stop condition • Receive data full (slave address match included) • Transmit data empty (slave address match included) • Transmit end

2.2 Comparison of Register Differences

Table 2.2 shows Comparison of Register Differences Between the RI3C Module and the RIIC Module.

Table 2.2 Comparison of Register Differences Between the RI3C Module and the RIIC Module

Register	Bit	RI3C	RIIC
ICMR	—	Mode register	—
ICMR1	—	—	I²C bus mode register 1
ICMR2	—	—	I²C bus mode register 2
ICMR3	—	—	I²C bus mode register 3
ICCR (RI3C) ICCR1 (RIIC)	—	Control register Register of the 32-bit length	I²C bus control register 1 Register of the 8-bit length
	IBAINC	I3C broadcast address include bit	—
	HJC	Hot-Join control bit	—
	ABORT	Host controller abort bit	—
	RESUME	Host controller resume bit	—
	ICE	Bus interface enable bit (b31)	Bus interface enable bit (b7)
	SDAI	—	SDA line monitor bit
	SCLI	—	SCL line monitor bit
	SDAO	—	SDA output control/monitor bit
	SCLO	—	SCL output control/monitor bit
	SOWP	—	SCLO/SDAO write protect bit
	CLO	—	Additional SCL output bit
	IICRST	—	I²C bus interface internal reset bit
ICCR2	—	—	I²C bus control register 2
ICCAR	—	Controller device address register	—
ICRCR	—	Reset control register	—
ICMMR	—	Operating mode monitor register	—
ICISR	—	Internal status register	—
ICISER	—	Internal status detection enable register	—
ICISIER	—	Internal status interrupt enable register	—
ICDCTIR	—	Device characteristics table index Register	—
ICINCR	—	IBI notification control register	—
ICTCR	—	Target mode control register	—
ICSBR	—	Standard bit rate register	—
ICEBR	—	Extended bit rate register	—
ICBFTR	—	Bus-free time setting register	—
ICBATR	—	Bus available time setting register	—
ICBITR	—	Bus idle time setting register	—
ICOCR	—	Output signal control register	—
ICTOR	—	Timeout control register	—

Register	Bit	RI3C	RIIC
ICSTCR	—	Clock stall control register	—
ICTDLR	—	Target transmit/receive data length register	—
ICCQR	—	Command queue register	—
ICRQR	—	Response queue register	—
ICDR	—	Transmit/receive data register	—
ICIQR	—	IBI queue register	—
ICSQR	—	Receive status queue register	—
ICQBTCR	—	Queue buffer threshold control register	—
ICDBTCR	—	Data buffer threshold control register	—
ICSQTCR	—	Receive status queue threshold control register	—
ICSR2	—	Status register 2 Register of the 32-bit length	I^2C bus status register 2 Register of the 8-bit length
	START	Start condition detection flag (b0)	Start condition detection flag (b2)
	STOP	Stop condition detection flag (b1)	Stop condition detection flag (b3)
	HDRXDF	HDR exit pattern detection flag	—
	TMOF	Timeout detection flag (b20)	Timeout detection flag (b0)
	AL	—	Arbitration loss flag
	NACKF	—	NACK detection flag
	RDRF	—	Receive data full flag
	TEND	—	Transmission end flag
	TDRE	—	Transmit data empty flag
ICSER	—	Status detection enable register Register of the 32-bit length	I^2C bus status enable register Register of the 8-bit length
	STDE	Start condition detection enable bit	—
	SPDE	Stop condition detection enable bit	—
	HDRXDE	HDR exit pattern detection enable bit	—
	TMOE	Timeout detection enable bit	—
	SAR0E	—	Slave address register 0 enable bit
	SAR1E	—	Slave address register 1 enable bit
	SAR2E	—	Slave address register 2 enable bit
	GCAE	—	General call address enable bit
	DIDE	—	Device ID address detection enable bit
	HOAE	—	Host address enable bit
ICSIER	—	Status interrupt enable register	—
ICCSR	—	Communication status register	—
ICCSER	—	Communication status detection enable register	—
ICCSIER	—	Communication status interrupt enable register	—

Register	Bit	RI3C	RIIC
ICBSR	—	Bus status register	—
ICTDATRm	—	Target device address table register m (m = 0 to 3)	—
ICEDATR	—	Extended target device address table register	—
ICDAR0	—	Device address register 0	—
ICTDCTRm	—	Target device address characteristics table register m (m = 0 to 3)	—
ICDCTR	—	Device characteristics table register	—
ICPIDLR	—	Provisioned ID Low register	—
ICPIDHR	—	Provisioned ID High register	—
ICDAMR0	—	Device address monitor register 0	—
ICTEVR	—	Target event register	—
ICASR	—	Activity state register	—
ICMWLR	—	Maximum write length register	—
ICMRLR	—	Maximum read length register	—
ICTMR	—	Test mode register	—
ICDSR	—	Device status register	—
ICMWSR	—	Maximum write speed register	—
ICMRSR	—	Maximum read speed register	—
ICMTTR	—	Maximum read turnaround time register	—
ICTSIR	—	Timing support information register	—
ICBCR	—	Bit count register	—
ICQBSR	—	Queue buffer status register	—
ICDBSR	—	Data buffer status register	—
ICSQSR	—	Receive status queue status register	—
ICIMR	—	Internal status monitor register	—
ICCECR	—	Controller error count register	—
ICFER	—	—	I^2C bus function enable register
ICIER	—	—	I^2C bus interrupt enable register
ICSR1	—	—	I^2C bus status register
SARLy	—	—	Slave address register Ly (y = 0 to 2)
SARUy	—	—	Slave address register Uy (y = 0 to 2)
ICBRL	—	—	I^2C bus bit rate Low-level register
ICBRH	—	—	I^2C bus bit rate High-level register
ICDRT	—	—	I^2C bus transmit data register
ICDRR	—	—	I^2C bus receive data register
ICDRS	—	—	I^2C bus shift register

3. Reference Documents

User's Manuals: Hardware

RX671 Group User's Manual: Hardware (R01UH0899EJ)

RX26T Group User's Manual: Hardware (R01UH0979EJ)

If you use a product of a group for which none of the above manuals are applicable, refer to the applicable hardware manual ("User's Manual: Hardware" for the relevant group).
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.21.23	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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