RX Family

Comparison of the Differences Between the RSCI Module and the SCI Module

Introduction

This application note is a reference material for confirming the differences between the SCI and RSCI modules of the RX26T Group. The differences covered include general differences and register differences.

Target Devices

RX Family

Contents

1. Comparison of the Differences Between the RSCI Module and the SCI Module

1.1 Comparison of General Differences

Table 1.1 shows Comparison of General Differences Between the SCI Module and the RSCI Module.

Table 1.1 Comparison of General Differences Between the SCI Module and the RSCI Module

Item	SCI	RSCI
Serial communications modes	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Manchester • Clock synchronous • Smart card interface • Simple I²C • Simple SPI bus (4-wire serial bus) • Extended serial
Transfer speed	Bit rate specifiable using an on-chip baud rate generator	Bit rate specifiable using an on-chip baud rate generator
Full-duplex communication	Transmitter: Continuous transmission is possible by using the double-buffer structure. Receiver: Continuous reception is possible by using the double-buffer structure.	Transmitter: Continuous transmission is possible by using the double-buffer structure. Receiver: Continuous reception is possible by using the double-buffer structure.
Half-duplex communication	Half-duplex communication using a single pin that doubles as the TXDX12 and RXDX12 pins (SCI12 only)	Half-duplex communication using the TXDn pin
Data transfer	LSB-first or MSB-first selectable as the byte order *1	LSB-first or MSB-first selectable as the byte order
I/O signal level inversion	The levels of input and output signals can be inverted independently.	The levels of input and output signals can be inverted independently.
RXD input signal select function	If the RXD signal on the transmission line is attenuated, a comparator can be used instead of a receiver. (supported by SCI5 only)	If the RXD signal on the transmission line is attenuated, a comparator can be used instead of a receiver.

Item		SCI	RSCI
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, and data match Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, receive data ready, and receive data match Detection/transmission of the Break Field, detection of a bus collision, and detection of the valid edge End of generating the start condition, restart condition, or stop condition
RS-485 driver control function		—	Outputs the DE signal that enables the transmission mode of the external transceiver.
Loopback function		—	Self-diagnosis of the communication function is possible by connecting the TXD and RXD in the internet protocol.
Low power consumption function		Transition to the module stop state is possible for each channel.	Transition to the module stop state is possible for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmitter/ receiver	—	Configuration selectable from 1-stage register or 32-stage FIFO buffer
	Data match detection	Ability to compare the received data against the content of the comparison data register, and generate an interrupt request when they match	Ability to compare the received data against the compare data, and output an interrupt request when they match
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge on the RXDn pin is selectable.
	Receive data sampling timing adjustment	The receive data sampling point can be shifted from the center of the data forward or backward to a base point.	The receive data sampling point can be shifted from the center of the data forward or backward to a base point.
	Transmit signal change timing adjustment	Either the falling or rising edge of the transmit data can be delayed.	Either the falling or rising edge of the transmit data is delayed.

Item		SCI	RSCI
Asynchronous mode	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.	When a framing error occurs, a break can be detected by reading the register.
	Clock source	The internal clock or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	The internal clock or external clock can be selected.
	Double-speed mode	Baud rate generator double-speed mode can be selected.	Baud rate generator double-speed mode can be selected.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
	HBS support mode	—	Transmission/reception using the RZI (Return-to-Zero, Inverted) code is possible.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive data sampling timing adjustment function	—	The receive sampling timing can be adjusted to a time later than the default timing (only when the internal clock is used).
	Receive error detection	Overrun error	Overrun error
	Clock source	—	The internal clock (master) or external clock (slave) can be selected.
	Double-speed mode	—	Baud rate generator double-speed mode can be selected.
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmitter/ receiver	—	Configuration selectable from 1-stage register or 32-stage FIFO buffer
Manchester mode	Data length	—	7, 8, or 9 bits
	Transmission stop bits	—	1 or 2 bits
	Receive error detection function	—	Parity error, overrun error, framing error, Manchester code error, preface error, start bit error, and receive sync error

Item		SCI	RSCI
Manchester mode	Hardware flow control	—	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Clock source	—	The internal clock is used. (In Manchester mode, the external clock must not be set because its operation is not guaranteed.)
	Double-speed mode	—	Baud rate generator double-speed mode can be selected.
	Multi-processor communications function	—	Serial communication among multiple processors
	Noise cancellation	—	The signal paths from input on the RXDn pins incorporate digital noise filters.
	Manchester encoding/ decoding function	—	Function that transmits/receives data as Manchester code by using Manchester encoding/decoding
	Preface setting/ detection function	—	Function that detects the beginning of a frame from the preface pattern. One of four preface patterns can be selected. The preface length can also be changed in the range from 0 to 15 bits.
	Start bit setting/ detection function	—	1 bit or 3 bits can be set as the start bit length. If 3 bits is set, the type of the subsequent data can be judged from two patterns.
	Receive retiming function	—	Function to perform timing correction for each bit center edge by using manchester code having edge at bit center
Smart card interface mode	Error processing	An error signal can be automatically transmitted when a parity error is detected during reception.	An error signal can be automatically transmitted when a parity error is detected during reception.
		Data is automatically retransmitted when an error signal is received during transmission.	Data is automatically retransmitted when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		SCI	RSCI
Extended serial mode	Start frame transmission	• Output of the Break Field low width / generation of an interrupt on completion of output • Detection of bus collision / generation of an interrupt on detection	• Ability to transmit Break Field and output the Break Field transmission end interrupt • Detection of bus collision and generation of an interrupt on detection of bus conflict
	Start frame reception	• Detection of the Break Field low width / generation of an interrupt on completion of detection • Data comparison of Control Fields 0 and 1 / generation of an interrupt when they match • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Support for start frames that do not include a Break Field • Support for start frames that do not include a Control Field 0 • Function for measuring bit rates	• Ability to detect Break Field and output the Break Field detection interrupt • Function that compares the data in Control Field 0 and the data in Control Field 1 • Two kinds of data for comparison (primary and secondary) can be set in Control Field 1. • A priority interrupt bit can be set in Control Field 1. • Function for measuring bit rates
	I/O control function	• Polarity can be selected for TXDX12 and RXDX12 signals. • Digital filtering can be specified for the RXDX12 signal. • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Receive data sampling timing of RXDX12 pin can be selected.	—
Simple I²C mode	Communication format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (multi-master operation is not possible)
	Transfer speed	Fast mode supported	Maximum of 400 kbps
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. The interval for noise cancellation is adjustable.	The signal paths from input on the SCL and SDA pins incorporate digital noise filters. The interval for noise cancellation is adjustable.

Item		SCI	RSCI
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	Clock source	—	The internal clock (master) or external clock (slave) can be selected.
	Double-speed mode	—	Baud rate generator double-speed mode can be selected.
	Receive data sampling timing adjustment function	—	The receive sampling timing can be adjusted to a time later than the default timing (only when the internal clock is used).
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
	Transmitter/ receiver	—	Configuration selectable from 1-stage register or 32-stage FIFO buffer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function		Error (receive error or error signal detection) event output	Error (receive error or error signal detection) event output
		Receive data full event output	Receive data full event output
		Transmit data empty event output	Transmit data empty event output
		Transmit end event output	Transmit end event output
		—	Receive data match event output
		—	Receive data mismatch event output
		—	Valid edge detection event output

Note: 1. In simple I^2C mode, data can be transmitted with MSB-first only.

1.2 Comparison of Functions Supported by Channels

Table 1.2 shows List of Functions Supported by Channels on the SCI Module and the RSCI Module.

Table 1.2 List of Functions Supported by Channels on the SCI Module and the RSCI Module

Item	SCI	RSCI
Asynchronous mode	SCI1, SCI5, SCI6, SCI12	RSCI8, RSCI9, RSCI11
Clock synchronous mode	SCI1, SCI5, SCI6, SCI12	RSCI8, RSCI9, RSCI11
Manchester mode	—	RSCI9, RSCI11
Smart card interface mode	SCI1, SCI5, SCI6, SCI12	RSCI8, RSCI9, RSCI11
Simple I^2C mode	SCI1, SCI5, SCI6, SCI12	RSCI8, RSCI9, RSCI11
Simple SPI mode	SCI1, SCI5, SCI6, SCI12	RSCI8, RSCI9, RSCI11
Extended serial mode	SCI12	RSCI9, RSCI11
Data match detection	SCI1, SCI5, SCI6, SCI12	—
FIFO buffer	—	RSCI11
TMR clock input	SCI5, SCI6, SCI12	—
Event link function	SCI5	RSCI11
Peripheral module clock	PCLKB: SCI1, SCI5, SCI6, SCI12	PCLKB: RSCI8, RSCI9 PCLKA: RSCI11

1.3 Comparison of Register Differences

Table 1.3 shows Comparison of Register Differences Between the SCI Module and the RSCI Module.

Table 1.3 Comparison of Register Differences Between the SCI Module and the RSCI Module

Register	Bit	SCI	RSCI
RDR	—	Receive data register Register of the 8-bit length	Receive data register Register of the 32-bit length
	RDAT[8:0]	—	Receive data bit
	MPB	—	Multi-processor bit monitor flag
	DR	—	Receive data ready flag
	PER	—	Parity error flag
	FER	—	Framing error flag
	ORER	—	Overrun error flag
	APER	—	Aggregate parity error flag
	AFER	—	Aggregate framing error flag
RDRH, RDRL, RDRHL	—	Receive data registers H, L, and HL	—
TDR	—	Transmit data register Register of the 8-bit length	Transmit data register Register of the 32-bit length
	TDAT[8:0]	—	Transmit data bit
	MPBT	—	Transmit multi-processor bit
	SYNC	—	Sync pulse select bit
TDRH, TDRL, TDRHL	—	Transmit data registers H, L, and HL	—
SMR	—	Serial mode register	—
SCR (SCI) SCR0 (RSCI)	—	Serial control register Register of the 8-bit length	Serial control register Register of the 32-bit length
	CKE[1:0]	Clock enable bits	—
	TEIE	Transmit end interrupt enable bit (b2)	Transmit end interrupt enable bit (b21)
	MPIE	Multi-processor interrupt enable bit (b3)	Multi-processor interrupt enable bit (b8)
	RE	Receive enable bit (b4)	Receive enable bit (b0)
	TE	Transmit enable bit (b5)	Transmit enable bit (b4)
	RIE	Receive interrupt enable bit (b6)	Receive interrupt enable bit (b16)
	TIE	Transmit interrupt enable bit (b7)	Transmit interrupt enable bit (b20)
	DCME	—	Data compare match enable bit
	IDSEL	—	ID frame select bit
	TEIE	—	Transmit end interrupt enable bit
	SSE	—	SSn# pin function enable bit
SCR1	—	—	Control register 1
SCR2	—	—	Control register 2

Register	Bit	SCI	RSCI
SCR3	—	—	Control register 3
SCR4	—	—	Control register 4
SSR	—	Serial status register 8-bit register length	Status register 32-bit register length
	MPBT	Multi-processor bit transfer bit	—
	MPB	Multi-processor bit	—
	TEND	Transmit end flag (b2) 0: Character transmission is in progress. 1: Character transmission ended.	Transmit end flag (b30) 0: A character is being transmitted or standing by for transmission. 1: Completed character transmission or now transmitting Break Field.
	PER	Parity error flag	—
	FER	Framing error flag	—
	ORER	Overrun error flag (b5)	Overrun error flag (b24)
	RDRF	Receive data full flag (b6)	Receive data full flag (b31)
	TDRE	Transmit data empty flag (b7)	Transmit data empty flag (b29)
	RXDMON	—	RXD line monitoring flag
	DCMF	—	Data match flag
	DPER	—	Matched data parity error flag
	DFER	—	Matched data framing error flag
	MFF	—	Mode fault flag
	APER	—	Aggregate parity error flag
	AFER	—	Aggregate framing error flag
SCMR	—	Smart card mode register	—
BRR	—	Bit rate register	—
MDDR	—	Modulation duty register	—
SEMR	—	Serial extended mode register	—
SNFR	—	Noise filter configuration register	—
SIMR1	—	I^2C mode register 1	—
SIMR2	—	I^2C mode register 2	—
SIMR3	—	I^2C mode register 3	—
SIMR	—	—	I^2C mode register
SISR	IICSTIF	—	Condition generation completion flag
SPMR	—	SPI mode register	—
CDR	—	Comparison data register	—
DCCR	—	Data comparison control register	—
SPTR	—	Serial port register	—
TMGR	—	Transmit/receive timing select register	—
ESMER	—	Extended serial mode enable register	—
CR0	—	Control register 0	—
CR1	—	Control register 1	—

Register	Bit	SCI	RSCI
CR2	—	Control register 2	—
CR3	—	Control register 3	—
PCR	—	Port control register	—
ICR	—	Interrupt control register	—
STR	—	Status register	—
STCR	—	Status clear register	—
CF0DR	—	Control Field 0 data register	—
CF0CR	—	Control Field 0 compare enable register	—
CF0RR	—	Control Field 0 receive data register	—
PCF1DR	2014	Primary Control Field 1 data register	—
SCF1DR	—	Secondary Control Field 1 data register	—
CF1CR	—	Control Field 1 compare enable register	—
CF1RR	—	Control Field 1 receive data register	—
TCR	—	Timer control register	—
TMR	—	Timer mode register	—
TPRE	—	Timer prescaler register	—
TCNT	—	Timer count register	—
FCR	—	—	FIFO control register
MMCR	—	—	Manchester mode control register
DECR	—	—	DE signal control register
XCR0	—	—	Extended serial mode control register 0
XCR1	—	—	Extended serial mode control register 1
XCR2	—	—	Extended serial mode control register 2
RFSR	—	—	Receive FIFO status register
TFSR	—	—	Transmit FIFO status register
MMSR	—	—	Manchester mode status register
XSR0	—	—	Extended serial mode status register 0
XSR1	—	—	Extended serial mode status register 1
SSCR	—	—	Status clear register
SISCR	—	—	I2C status clear register
RFSCR	—	—	Receive FIFO status clear register
MMSCR	—	—	Manchester mode status clear register
XSCR	—	—	Extended serial mode status clear register
HBSCR	—	—	HBS support mode control register

2. Reference Documents

User's Manual: Hardware

RX26T Group User's Manual: Hardware (R01UH0979EJ)

If you use a product of a group other than the RX26T Group, refer to the applicable hardware manual ("User's Manual: Hardware" for the relevant group).

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Revision History

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		Page	Summary
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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