RX Family

Comparison of the Differences Between the RSPId Module and the RSPIA Module

Introduction

This application note is a reference material for confirming the differences between the RSPId and RSPIA modules of the RX26T Group. The differences covered include general differences and register differences.

Target Devices

RX Family

If you want to use this application note for a device of another family, modify the content according to the specifications of the device and conduct thorough evaluation before use.

Contents

1. Comparison Between the RSPId Module and the RSPIA Module

1.1 Comparison of General Differences

Table 1.1 shows Comparison of General Differences Between the RSPId Module and the RSPIA Module.

Table 1.1 Comparison of General Differences Between the RSPId Module and the RSPIA Module

Item	RSPId	RSPIA
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Full-duplex or simplex (transmit-only or reception-only) can be selected. • Serial communication in master or slave mode is possible. • The polarity of the serial transfer clock can be switched. • The phase of the serial transfer clock can be switched.
Data format	• Switching between MSB-first and LSB-first is possible. • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transmitted or received at one time (frame size: 32 bits, max.). • Byte swapping of transmit and receive data is possible. • Ability to invert the logic level of transmit/receive data	• Switching between MSB-first and LSB-first is possible. • The transfer bit length can be changed in the range from 4 to 32 bits. • FIFO buffer of four 32-bit stages are available for transmission and for reception. • Up to four frames can be transmitted or received at one time (frame size: 32 bits, max.). • Byte swapping of transmit/receive data is possible. • Ability to invert the logic level of transmit/receive data

Item	RSPId	RSPIA
Bit rate	In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 1/2 to 1/4096). In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). High-level width: 2 cycles of PCLK Low-level width: 2 cycles of PCLK	In master mode, the on-chip baud rate generator generates RSPCK by dividing the frequency of PCLKA. The division ratio can be set in the range from 1/2 to 1/4096. In slave mode, the external input clock is used as the serial clock. The maximum frequency is PCLKA/2. (High-level width: 1 cycle of PCLKA Low-level width: 1 cycle of PCLKA)
Buffer configuration	The transmit and receive buffers are in a double buffer configuration. The length of each buffer is 128 bits.	The transmit buffer and the receive buffer are different buffers.
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection *1 • Parity error detection	• Mode fault error detection • Underrun error detection • Overrun error detection • Parity error detection • Receive data ready detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, signals are output from the SSLA0 to SSLA3 pins. • In multi-master mode: The SSLA0 pin is used for input; the SSLA1 to SSLA3 pins are unused or used for output. • In slave mode: SSLA0 pin is used for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • Function for changing SSL polarity	[Motorola SPI settings] • Four SSL pins (SSL00 to SSL03) for each RSPIA channel • In single-master mode, the SSL00 to SSL03 signals are output. • In multi-master mode: The SSL00 signal is input and the SSL01 to SSL03 signals are output or Hi-Z. • In slave mode: The SSL00 signal is input and the SSL01 to SSL03 signals are Hi-Z (not used). • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • Function for changing SSL polarity

Item	RSPId	RSPIA
SSL control function		[TI SSP settings] • Four SSL signals (SSL00 to SSL03) for each RSPIA channel • In single-master mode, the SSL00 to SSL03 signals are output. • In multi-master mode: The SSL00 signal is input and the SSL01 to SSL03 signals are output or Hi-Z. • In slave mode: The SSL00 signal is input and the SSL01 to SSL03 signals are Hi-Z (not used). • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 0 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • A delay to wait since RSPCK stops until data output is placed in the Hi-Z state (OE negation delay) can be set. Range: 1 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK clock cycles Minimum unit: 1 RSPCK clock cycle • Function for changing SSL polarity
Communication protocol	—	Motorola SPI TI SSP (Synchronous Serial Protocol)
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB-first/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value can be specified in SSL negation. • RSPCK auto-stop function	[Motorola SPI settings] • A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB-first/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value can be specified in SSL negation. • RSPCK auto-stop function (This function can be enabled or disabled.)

Item	RSPId	RSPIA
Control in master transfer	• The delay between data bytes can be shortened during burst transfers.	• The delay between data bytes can be shortened during burst transfers. [TI SSP settings] • A transfer of up to eight commands can be executed sequentially in looped execution. • The following items can be specified for each command: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB-first/MSB-first, burst, RSPCK delay, SSL negation delay (OE negation delay), and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value can be specified in SSL negation. • RSPCK auto-stop function (this function can be enabled or disabled) • The delay between data bytes can be shortened during burst transfers.
Interrupt sources	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • Error interrupt — Mode fault — Underrun — Overrun — Parity error • Idle interrupt • Communication end interrupt	Five sources • Receive buffer full/receive data ready interrupt • Transmit buffer empty interrupt • Error interrupt — Mode fault — Underrun — Overrun — Parity error — Receive data ready • Idle interrupt • Communication end interrupt
Event link function (output)	The following events can be output to the event link controller (RSPI0): • Receive buffer full event • Transmit buffer empty event • Error event — Mode fault — Overrun — Underrun — Parity error • Idle event • Communication end event	Five events can be output to the event link controller. • Receive buffer full/receive data ready event signal • Transmit buffer empty event signal • Mode fault/underrun/overrun/parity error/receive data ready event signal • Idle event signal • Communication end event signal

Item	RSPId	RSPIA
Other functions	Function for initializing the RSPI Loopback mode function	Function for disabling (initializing) the RSPI Loopback mode function Function that polls the status of the SPE bit
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Note: 1. If the RSPCK auto-stop function is enabled in master receive mode, no overrun error occurs because the transfer clock stops upon detection of an overrun error.

1.2 Comparison of Register Differences

Table 1.2 shows Comparison of Register Differences Between the RSPId Module and the RSPIA Module.

Table 1.2 Comparison of Register Differences Between the RSPId Module and the RSPIA Module

Register	Bit	RSPId	RSPIA
SPCR	—	RSPI control register Register of the 8-bit length	RSPI control register Register of the 32-bit length
	SPMS	RSPI mode select bit (b0)	RSPI mode select bit (b24)
	TXMD	Communications Operating mode select bit	—
	MODFEN	Mode fault error detection enable bit (b2)	Mode fault error detection enable bit (b14)
	MSTR	RSPI master/slave mode select bit (b3)	RSPI master/slave mode select bit (b30)
	SPEIE	Error interrupt enable bit (b4)	Error interrupt enable bit (b16)
	SPTIE	Transmit buffer empty interrupt enable bit (b5)	Transmit buffer empty interrupt enable bit (b20)
	SPE	RSPI function enable bit (b6)	RSPI function enable bit (b0)
	SPRIE	Receive buffer full interrupt enable bit (b7)	Receive buffer full interrupt enable bit (b17)
	MRCKS	—	Master receive clock select bit
	SPPE	—	Parity enable bit
	SPOE	—	Parity mode bit
	PTE	—	Parity self-diagnosis bit
	SCKASE	—	RSPCK auto-stop function enable bit
	SCKDDIS	—	Bit for disabling an RSPCK delay between data bytes
	MODFEN	—	Mode fault error detection enable bit
	SPIIE	—	Idle interrupt enable bit
	RDRIS	—	Receive data ready interrupt select bit
	SPCIE	—	Communication end interrupt enable bit
	FRFS	—	Frame format select bit
	CMMD[1:0]	—	Communication mode select bits
	SYNDIS	—	Synchronizer disable bit
SSLP	SSL0P	SSL0 signal polarity setting bit 0: SSL0 signal is active-low. 1: SSL0 signal is active-high.	SSL00 signal polarity setting bit [In the case of Motorola SPI] 0: SSL00 signal is active-low. 1: SSL00 signal is active-high. [In the case of TI SSP] 0: SSL00 signal is active-high. 1: SSL00 signal is active-low.

Register	Bit	RSPId	RSPIA
SSLP	SSL1P	SSL1 signal polarity setting bit 0: SSL1 signal is active-low. 1: SSL1 signal is active-high.	SSL01 signal polarity setting bit [In the case of Motorola SPI] 0: SSL01 signal is active-low. 1: SSL01 signal is active-high. [In the case of TI SSP] 0: SSL01 signal is active-high. 1: SSL01 signal is active-low.
	SSL2P	SSL2 signal polarity setting bit 0: SSL2 signal is active-low. 1: SSL2 signal is active-high.	SSL02 signal polarity setting bit [In the case of Motorola SPI] 0: SSL02 signal is active-low. 1: SSL02 signal is active-high. [In the case of TI SSP] 0: SSL02 signal is active-high. 1: SSL02 signal is active-low.
	SSL3P	SSL3 signal polarity setting bit 0: SSL3 signal is active-low. 1: SSL3 signal is active-high.	SSL03 signal polarity setting bit [In the case of Motorola SPI] 0: SSL03 signal is active-low. 1: SSL03 signal is active-high. [In the case of TI SSP] 0: SSL03 signal is active-high. 1: SSL03 signal is active-low.
SPSR	—	RSPI status register Register of the 8-bit length	RSPI status register Register of the 16-bit length
	RRDYF	—	Receive data ready flag
	OVRF	Overrun error flag (b0)	Overrun error flag (b8)
	IDLNF	Idle flag (b1)	Idle flag (b9)
	MODF	Mode fault error flag (b2)	Mode fault error flag (b10)
	PERF	Parity error flag (b3)	Parity error flag (b11)
	UDRF	Underrun error flag (b4)	Underrun error flag (b12)
	SPTEF	Transmit buffer empty flag (b5)	Transmit buffer empty flag (b13)
	SPCF	Communication end flag (b6)	Communication end flag (b14)
	SPRF	Receive buffer full flag (b7)	Receive buffer full flag (b15)
SPDR	—	RSPI data register Longword access Word access Byte access	RSPI data register

Register	Bit	RSPId	RSPIA
SPDCR	—	RSPI data control register Register of the 8-bit length	RSPI data control register Register of the 16-bit length
	SPFC[1:0]	Number of frames specification bits	—
	BYSW	—	Byte swap bit
SPDCR	SPRDTD	RSPI receive/transmit data select bit (b4)	RSPI receive/transmit data select bit (b3)
	DINV	—	Transfer data invert bit
	SPFC[1:0]	—	Number of frames setting bits
	SPLW	RSPI longword access/word access specification bit	—
	SPBYT	RSPI byte access specification bit	—
SSLND	SLNDL[2:0]	SSL negation delay setting bit b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	SSL negation delay setting bit b2 b0 [Master mode] 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK [Slave TI SSP mode] 0 0 0: 1 PCLKA 0 0 1: 2 PCLKA 0 1 0: 3 PCLKA 0 1 1: 4 PCLKA 1 0 0: 5 PCLKA 1 0 1: 6 PCLKA 1 1 0: 7 PCLKA 1 1 1: 8 PCLKA
SPND	SPNDL [2:0]	RSPI next-access delay register b2 b0 0 0 0: 1 RSPCK + 2 PCLK 0 0 1: 2 RSPCK + 2 PCLK 0 1 0: 3 RSPCK + 2 PCLK 0 1 1: 4 RSPCK + 2 PCLK 1 0 0: 5 RSPCK + 2 PCLK 1 0 1: 6 RSPCK + 2 PCLK 1 1 0: 7 RSPCK + 2 PCLK 1 1 1: 8 RSPCK + 2 PCLK	RSPI next-access delay register b2 b0 0 0 0: 1 RSPCK + 5 PCLKA 0 0 1: 2 RSPCK + 5 PCLKA 0 1 0: 3 RSPCK + 5 PCLKA 0 1 1: 4 RSPCK + 5 PCLKA 1 0 0: 5 RSPCK + 5 PCLKA 1 0 1: 6 RSPCK + 5 PCLKA 1 1 0: 7 RSPCK + 5 PCLKA 1 1 1: 8 RSPCK + 5 PCLKA
SPCR2	—	RSPI control register 2	—

Register	Bit	RSPId	RSPIA
SPCMDm	—	RSPI command register m Register of the 16-bit length	RSPI command register m Register of the 32-bit length
	SSLA[2:0]	SSL signal assertion setting bits (b6-b4)	SSL signal assertion setting bits (b26-b24)
	SPB[3:0] (RSPId) SPB[4:0] (RSPIA)	RSPI data length setting bit b11 b8 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0 0 1 0: 32 bits 0 0 1 1: 32 bits 0 1 0 0 to 0 1 1 1: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits	RSPI data length setting bit b20 b16 0 0 0 0 0 to 0 0 0 1 0: Setting prohibited 0 0 0 1 1: 4 bits 0 0 1 0 0: 5 bits 0 0 1 0 1: 6 bits : : 1 1 1 1 0: 31 bits 1 1 1 1 1: 32 bits
	SPNDEN	RSPI next-access delay enable bit 0: A delay of “RSPCK × 1 + PCLK × 2” is used as the next-access delay. 1: A delay set by the RSPI next-access delay register (SPND) is used as the next-access delay.	RSPI next-access delay enable bit 0: A delay of “RSPCK × 1 + PCLKA × 5” is used as the next-access delay. 1: A delay set by the RSPI next-access delay register (SPND) is used as the next-access delay.
	SLNDEN	SSL negation delay setting enable bit 0: A delay of “RSPCK × 1” is used as the SSL negation delay. 1: A delay set by the RSPI slave select negation delay register (SSLND) is used as the SSL negation delay.	SSL negation delay setting enable bit 0: Master: A delay of “RSPCK × 1” is used as the SSL negation delay. Slave TI SSP: A delay of “PCLKA × 1” is used as the SSL negation delay. 1: A delay set by the slave select negation delay register (SSLND) is used as the SSL negation delay.
	SCKDEN	RSPCK delay setting enable bit 0: A delay of “RSPCK × 1” is used as the RSPCK delay. 1: A delay set by the RSPI clock delay register (SPCKD) is used as the RSPCK delay.	RSPCK delay setting enable bit 0: Motorola SPI: A delay of “RSPCK × 1” is used as the RSPCK delay. TI SSP: A delay of “RSPCK × 0” is used as the RSPCK delay. 1: A delay set by the RSPCK delay register (SPCKD) is used as the RSPCK delay.

Register	Bit	RSPId	RSPIA
SPDCR2	—	RSPI data control register 2	—
SPCR3	—	RSPI control register 3	—
SPRMCR			
SPDRCSR			
SPFCR			RSPI FIFO control register
SPTFSR			RSPI transmit FIFO status register
SPRFSR			RSPI receive FIFO status register
SPSCLR			RSPI status clear register
SPFCLR			RSPI FIFO clear register

2. Reference Documents

User's Manuals: Hardware

RX26T Group User's Manual: Hardware (R01UH0979EJ)

If you use a product of a group other than the RX26T Group, refer to the applicable hardware manual ("User's Manual: Hardware" for the relevant group).

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sep.15.23	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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