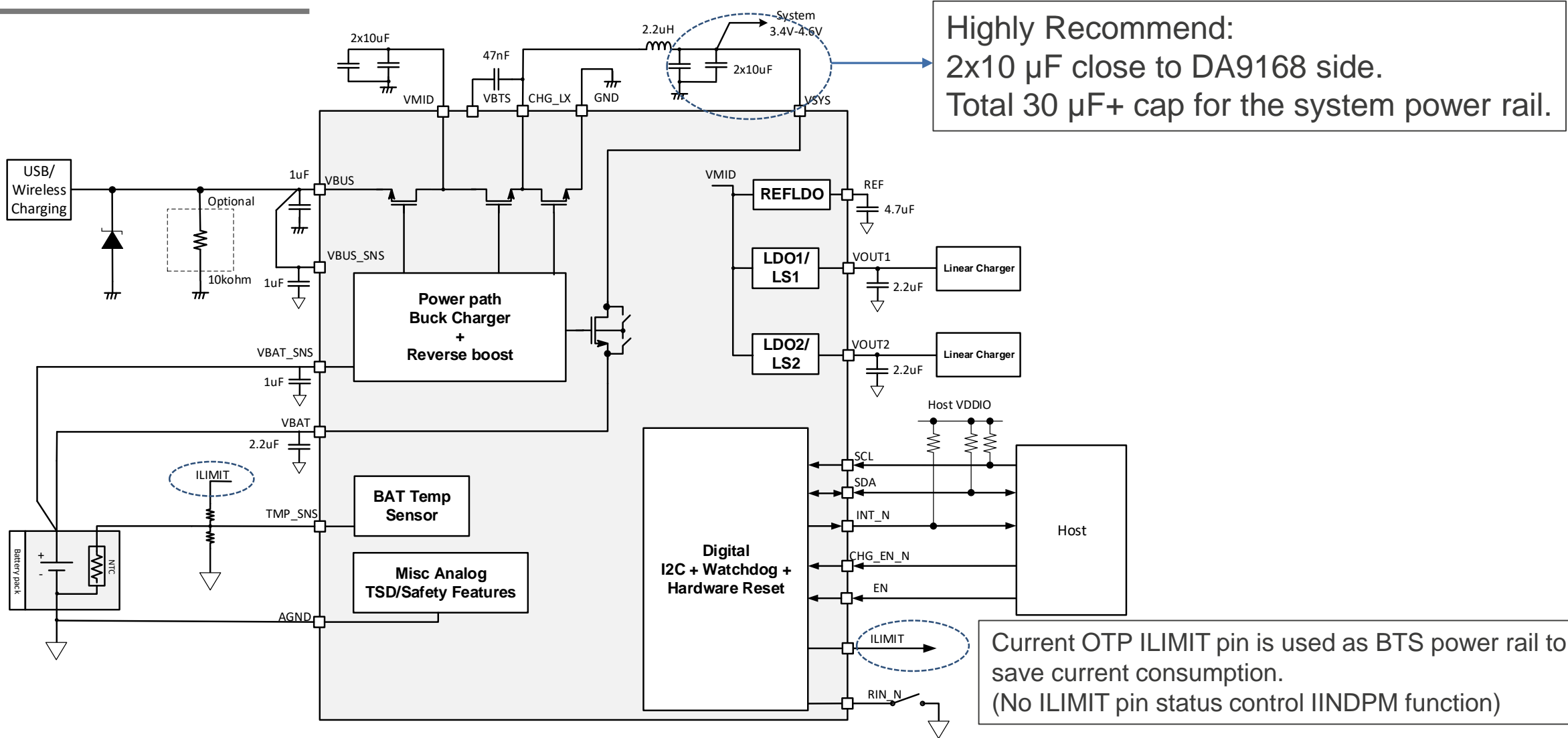


DA9168BC APPLICATION NOTE

FEB 2022

RENESAS ELECTRONICS CORPORATION

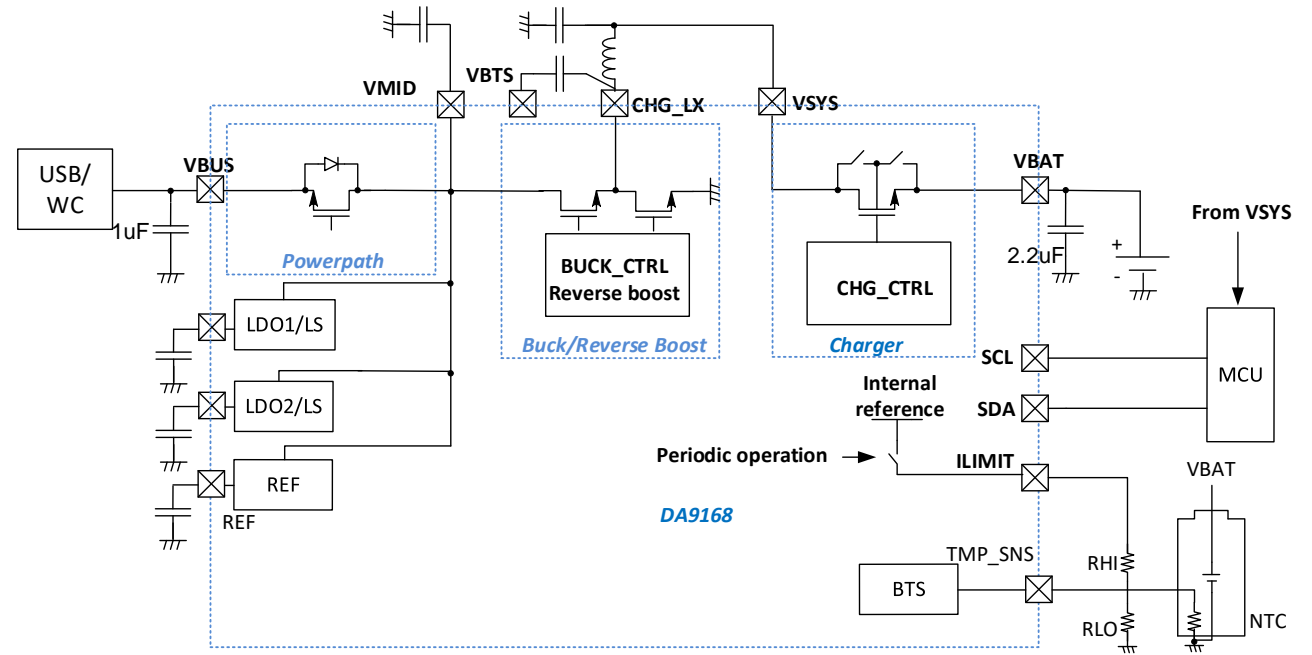
TYPICAL TWS APPLICATION WITH CURRENT OTP



DA9168 BTS WITH ILIMIT PIN

BTS WITH ILIMIT - VBUS IQ

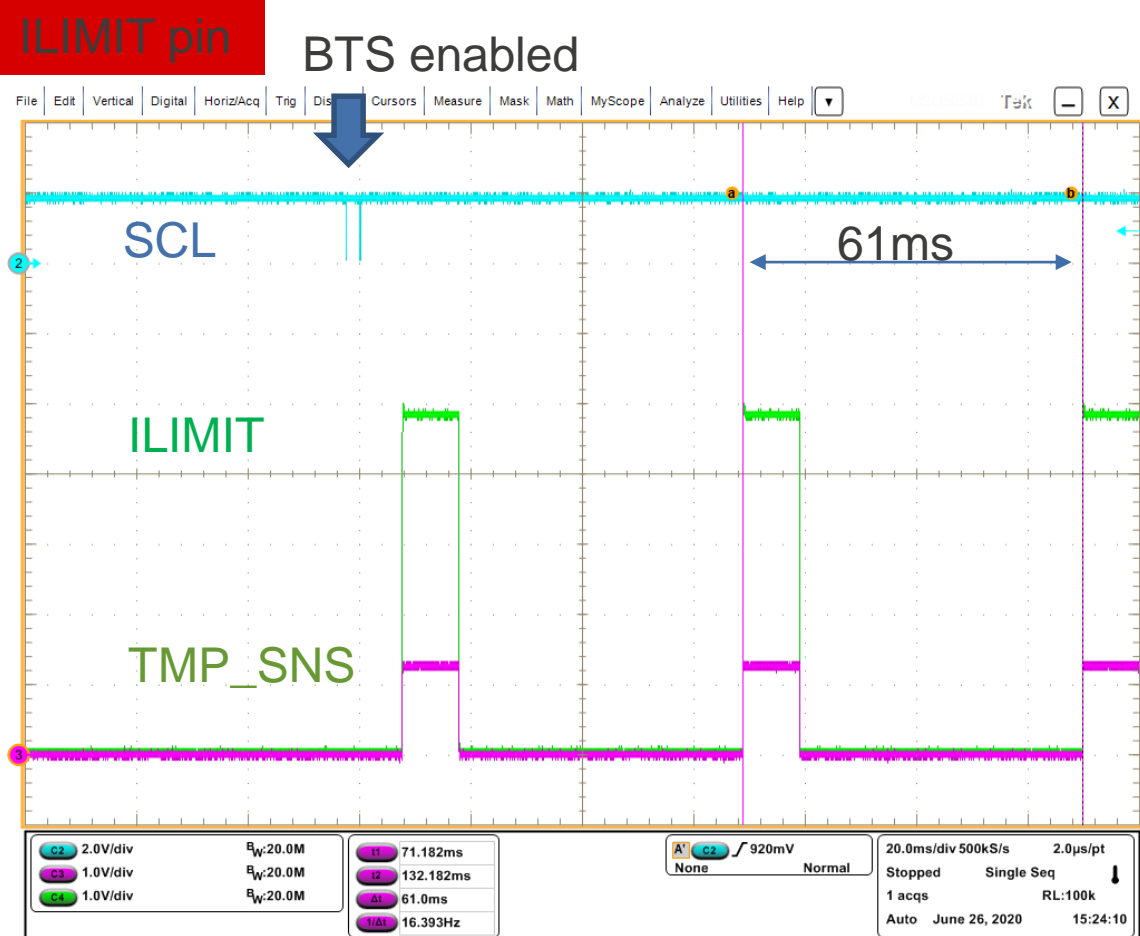
Using ILIMIT pin (instead of REF) for BTS has large I_Q savings



BTS Reference	BTS	Condition	I_Q from VBAT (μA)	Savings (μA)
REF	Disabled	Reverse boost + REFLDO	377	-
REF	Enabled	Reverse boost + REFLDO + BTS (50msec)	380	-
REF	Enabled	Reverse boost + REFLDO + BTS (2 sec)	377	-
ILIMIT	Disabled	Standby (boost disable)	10	I_Q increase from BTS just $\sim 1 \mu\text{A}$
ILIMIT	Enabled	Standby (boost disable) + BTS (50 msec)	41	
ILIMIT	Enabled	Standby (boost disable) + BTS (2 sec)	11	

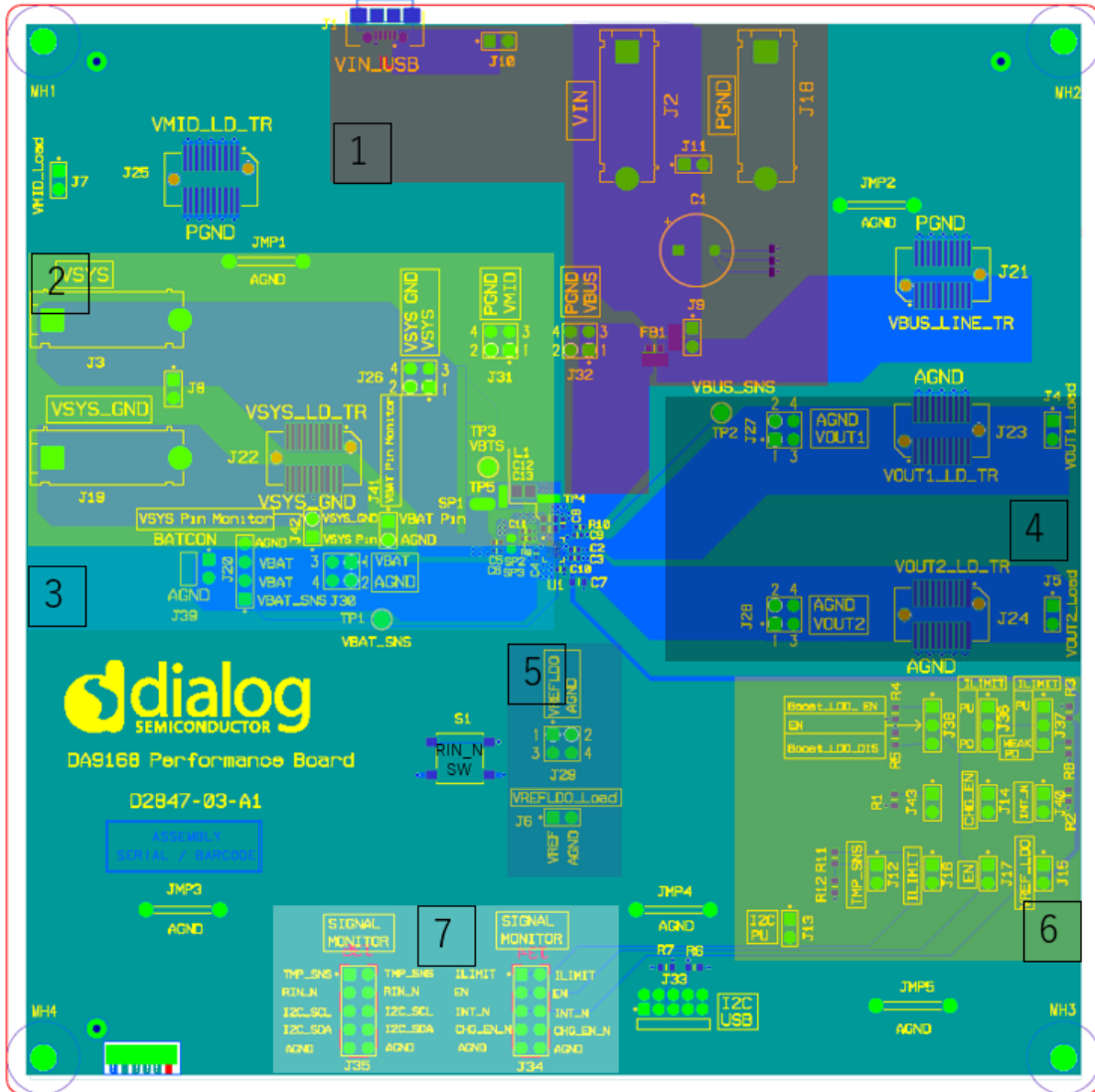
BTS WITH ILIMIT - PERIODIC OPERATION

✓ BTS periodic operation working as expected



DA9168 PERFORMANCE BOARD

PERFORMANCE BOARD OVERVIEW

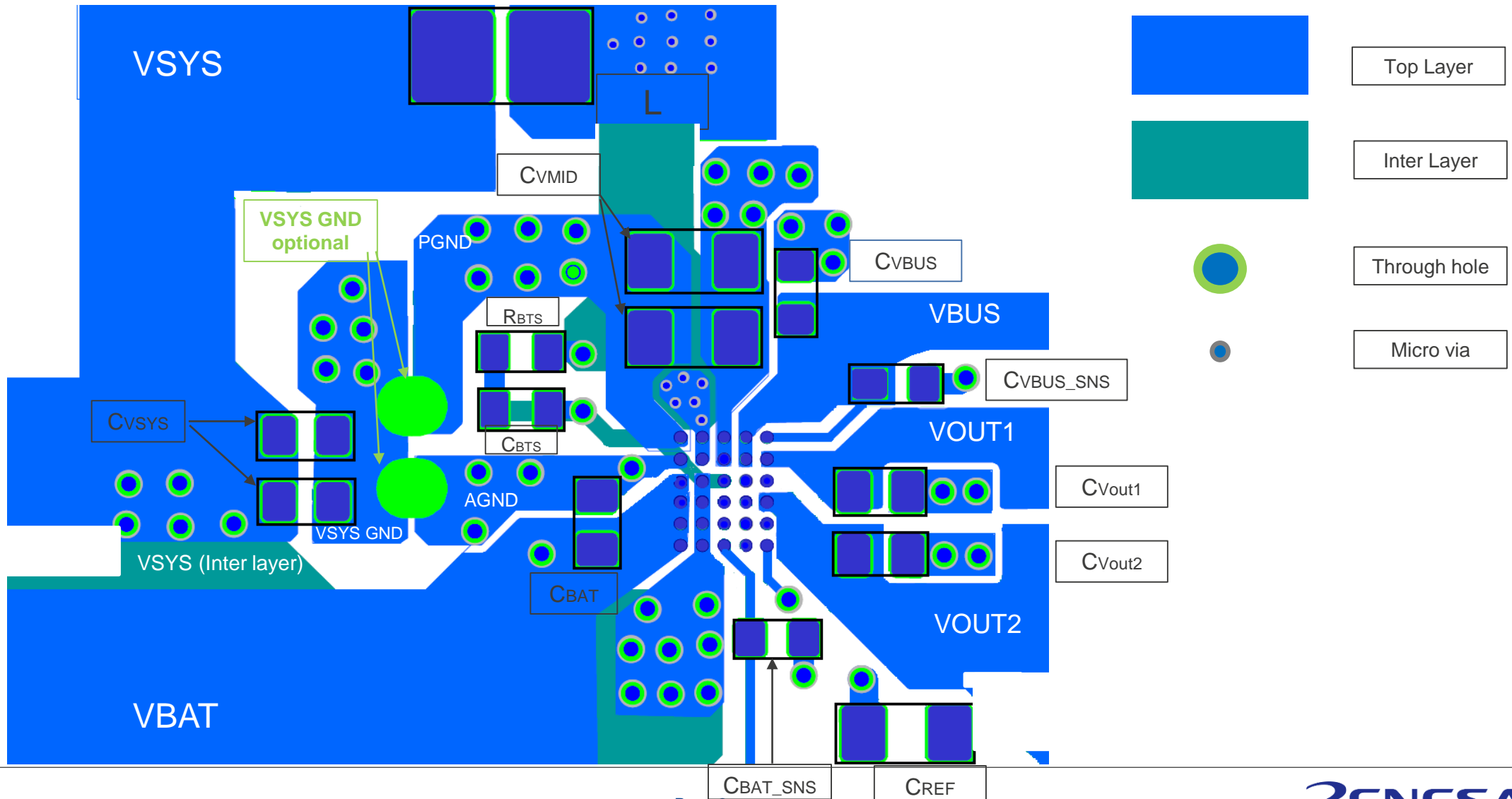


CAUTION

Apply high current to J26, J27, J28, J29, J30, J31, J32, J41 and J42 headers pin 1 and 2 may causes the voltage sensing traces burn out.

1. VBUS input section: Power supply and USB power supply connectors.
2. VSYS output section.
3. VBAT input/output section.
4. VOUT1 and VOUT2 outputs section.
5. REFLDO output section.
6. GPIOs network section.
7. GPIOs signal monitors section.

DA9168 PERFORMANCE BOARD LAYOUT CONCEPT



LAYOUT GUIDELINES

1. Minimize high frequency current path loop (VMID – CHG_LX – VSYS – GND and CHG_LX – VSYS - GND) to reduce EMI.
2. The two VMID capacitors (2x10 μ F) need to be placed as close as possible to the device DA9168.
3. The inductor input pin connected to GHG_LX pin should be as short as possible to reduce switching noise.
4. Make sure decoupling capacitors trace to the device pins as short as possible.
5. Split AGND (analog ground) and GND (power ground), and tie the analog ground and power ground with single ground connection.
6. For high current paths, ensure that the vias number and copper area is enough to support the operation current.

Note:

1. *Currently, there are two options for VSYS GND connection. Based on device evaluation results, recommend VSYS GND connect to AGND.*
2. *VBAT_SNS Capacitor can be removed if the battery connection is short enough.*

PERFORMANCE BOARD EXTERNAL COMPONENTS LIST

▪ Inductors

Manufacturers	Part #	Size (mm)	Inductance (μH)	Rdc (mΩ)		Heat Rating Current (A)		Saturation Current (A)	
				Typ	Max	Typ	Max	Typ	Max
Cyntec	HTEH20160H-1R0MSR	L = 2.0; W = 1.6 T = 0.8 (max)	1.0	29	35	4.4	4.0	4.0	3.6
Cyntec	HTEH20160H-2R2MSR	L = 2.0; W = 1.6 T = 0.8 (max)	2.2	75	90	2.6	2.3	2.9	2.7

PERFORMANCE BOARD EXTERNAL COMPONENTS LIST

▪ MLCC

Manufacturers	Part #	Size (mm)	Height (mm)	Capacitance (μF)	Rated voltage	Temp characteristics	ESR @1 MHz (Ω)	Position
Murata	GRM155R6YA105KE11	1005	0.5 ±0.1	1.0 ±10%	35 V	X5R	0.01	VBUS VBUS_SNS (*VBAT_SNS)
Murata	GRM155R61A106ME11	1005	0.5 ±0.2	10.0 ±20%	10 V	X5R	-	VSYS(2x)
Murata	GRM188R61E106MA73D	1608	0.8 ±0.2	10.0 ±20%	25 V	X5R	-	VMID (2x)
Taiyo Yuden	TMK105BJ473KV-F	1005	0.55 (Max)	0.047±10%	25 V	X5R	0.1	VBTS
Murata	GRM155R61C225KE11	1005	0.5 ±0.2	2.2 ±10%	16 V	X5R	0.008	VBAT VOUT1 VOUT2
Murata	GRM155R61C105KA12	1005	0.5 ±0.05	1.0 ±10%	16 V	X5R	0.02	VBAT_SNS
Murata	GRM185R61C475KE11	1608	0.5 ±0.05	4.7 ±10%	16 V	X5R	0.006	VREF

DA9168 GUI

For GUI Install and Setup, please refer to document:
“UM_PM_051_DA9168_Performance_Board_User_Manual”

SYSTEM STATUS REGISTERS

System Status

Register	Bitfield	Value
PMC_STATUS_00	S_VBUS_VINDPM	VBUS not in VINDPM
PMC_STATUS_00	S_VBUS_IINDPM	VBUS not in IINDPM
PMC_STATUS_00	S_VMID_OC	VMID not in OC
PMC_STATUS_00	S_VBAT_OC	VBAT not in OC
PMC_STATUS_00	S_VBUS_OK	VBUS not OK
PMC_STATUS_00	S_VMID_OK	VMID OK
PMC_STATUS_00	S_VSYS_OK	VSYS OK
PMC_STATUS_00	S_VBAT_OK	VBAT OK
0x0000	0x07	
PMC_STATUS_01	S_VBUS_OV	VBUS not in OV
PMC_STATUS_01	S_VMID_OV	VMID not in OV
PMC_STATUS_01	S_VSYS_OV	VSYS not in OV
PMC_STATUS_01	S_VBAT_OV	VBAT not in OV
PMC_STATUS_01	S_VBUS_UV	VBUS in UV
PMC_STATUS_01	S_VMID_UV	VMID not in UV
PMC_STATUS_01	S_VSYS_UV	VSYS not in UV
PMC_STATUS_01	S_VBAT_UV	VBAT not in UV
0x0001	0x08	
PMC_STATUS_02	S_TSD_CRIT	Below
PMC_STATUS_02	S_TSD_WARN	Below
PMC_STATUS_02	S_WD_TIMER	Watch-dog timer not
PMC_STATUS_02	S_TS_HOT	Battery temp sens...
PMC_STATUS_02	S_TS_WARM	Battery temp sens...
PMC_STATUS_02	S_TS_COOL	Battery temp sens...
PMC_STATUS_02	S_TS_COLD	Battery temp sens...
PMC_STATUS_02	S_TS_OFF	Battery temp sens...
0x0002	0x00	
PMC_STATUS_03	S_CHG_SLEEP	VBUS higher
PMC_STATUS_03	S_CHG_SPLMT	VBAT fet not
PMC_STATUS_03	S_CHG_TIMER	Charge timer not
PMC_STATUS_03	S_CHG_TRICKLE	Charger not in trickle
PMC_STATUS_03	S_CHG_PRE	Charger not
PMC_STATUS_03	S_CHG_CC	Charger not
PMC_STATUS_03	S_CHG_CV	Charger not
PMC_STATUS_03	S_CHG_DONE	Charge termination...
0x0003	0x00	
PMC_STATUS_04	S_VSYS_SHUTDOWN	VSYS not in SHUTDOWN
PMC_STATUS_04	S_REF_OC	REF not in OC
PMC_STATUS_04	S_LDO2_IMON1	LDO2 not in IMON1
PMC_STATUS_04	S_LDO2_IMON2	LDO2 not in IMON2
PMC_STATUS_04	S_LDO2_OC	LDO2 not in OC
PMC_STATUS_04	S_LDO1_IMON1	LDO1 not in IMON1
PMC_STATUS_04	S_LDO1_IMON2	LDO1 not in IMON2
PMC_STATUS_04	S_LDO1_OC	LDO1 not in OC
0x0004	0x00	

Note:
Beside normal VBUS plug in/out condition, S_VBUS_OK and S_VBUS_UV status flags by REV_VBUS on/off

Example: Rev-boost operation status

Read-only registers indicate device current status

Console Log:

```

2021-12-14, 10:52:32 [INFO] poller stopped
2021-12-14, 10:53:08 [INFO] starting poller
2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0000, value: 0x0b <-
2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0001, value: 0x00 <-
2021-12-14, 10:53:13 [INFO] poller stopped
2021-12-14, 10:53:30 [INFO] DA9168 addr: 0x0013, value: 0x39 -->
2021-12-14, 10:53:35 [INFO] starting poller
2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0000, value: 0x07 <-
2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0001, value: 0x08 <-
2021-12-14, 10:53:37 [INFO] poller stopped
    
```

Bitfield Info:

```

Bitfield: S_VSYS_UV
Register: PMC_STATUS_01 (0x1)
Bit: [1]
Access: R
POR: 0
Current Value: 0
Enumerated Value: VSYS not in UV
Chipmodel Blocks:
  PMC: S_VSYS_UV
Description:
  VSYS UV Status
    
```

SYSTEM EVENTS REGISTERS

The screenshot displays the DA9168BC register configuration tool. The main window is titled 'DA9168BC' and has a menu bar with 'File', 'Tools', 'Search', 'View', and 'Help'. Below the menu bar, there are tabs for 'FUNCTIONAL REGISTERS', 'SYSTEM', 'CHARGER', and 'LDO', with 'SYSTEM' selected. The 'SYSTEM' tab shows a 'Table View' of system events registers.

The registers are organized into columns:

- PMC_EVENT_00:** E_VBUS_VINDPM (VBUS not in VINDPM), E_VBUS_IINDPM (VBUS not in IINDPM), E_VMID_OC (VMID not in OC), E_VBAT_OC (VBAT not in OC), E_VBUS_OK (VBUS not OK), E_VMID_OK (VMID not OK), E_VSYS_OK (VSYS not OK), E_VBAT_OK (VBAT not OK), 0x0005 (0x00).
- PMC_EVENT_01:** E_VBUS_OV (VBUS not in OV), E_VMID_OV (VMID not in OV), E_VSYS_OV (VSYS not in OV), E_VBAT_OV (VBAT not in OV), E_VBUS_UV (VBUS not in UV), E_VMID_UV (VMID not in UV), E_VSYS_UV (VSYS not in UV), E_VBAT_UV (VBAT not in UV), 0x0006 (0x00).
- PMC_EVENT_02:** E_TSD_CRIT (Below), E_TSD_WARN (Below), E_WD_TIMER (Watch-dog timer not), E_TS_HOT (Battery temp sens...), E_TS_WARM (Battery temp sens...), E_TS_COOL (Battery temp sens...), E_TS_COLD (Battery temp sens...), E_TS_OFF (Battery temp sens...), 0x0007 (0x00).
- PMC_EVENT_03:** E_CHG_SLEEP (VBUS higher), E_CHG_SPLMT (VBAT fet not), E_CHG_TIMER (Charge timer not), E_CHG_TRICKLE (Charger not in trickle), E_CHG_PRE (Charger not), E_CHG_CC (Charger not), E_CHG_CV (Charger not), E_CHG_DONE (Charge termination...), 0x0008 (0x00).
- PMC_EVENT_04:** E_VSYS_SHUTDOWN (VSYS not in SHUTD...), E_REF_OC (REF not in OC), E_LDO2_IMON1 (LDO2 not in IMON1), E_LDO2_IMON2 (LDO2 not in IMON2), E_LDO2_OC (LDO2 not in OC), E_LDO1_IMON1 (LDO1 not in IMON1), E_LDO1_IMON2 (LDO1 not in IMON2), E_LDO1_OC (LDO1 not in OC), 0x0009 (0x00).

A yellow box highlights the PMC_EVENT_00 to PMC_EVENT_04 registers. A blue arrow points from this box to a text box that says 'Registers indicate device events, clear on read (Default)'. Another blue arrow points from this text box to the 'PMC SYS 00' register configuration window.

The 'PMC SYS 00' window shows the following settings:

- E_RD_CLR_DIS: Low
- VSYS_MIN: 3.7
- VINDPM: 4.2
- 0x000F: 0x38

The console window at the bottom shows a log of system events:

```

2021-12-14, 10:52:32 [INFO] poller stopped
2021-12-14, 10:53:08 [INFO] starting poller
2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0000, value: 0x0b <-
2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0001, value: 0x00 <-
2021-12-14, 10:53:13 [INFO] poller stopped
2021-12-14, 10:53:30 [INFO] DA9168 addr: 0x0013, value: 0x39 ->
2021-12-14, 10:53:35 [INFO] starting poller
2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0000, value: 0x07 <-
2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0001, value: 0x08 <-
2021-12-14, 10:53:37 [INFO] poller stopped
  
```

The 'Bitfield Info' window shows details for the E_VSYS_SHUTDOWN bitfield:

- Bitfield: E_VSYS_SHUTDOWN
- Register: PMC_EVENT_04 (0x9)
- Bit: [7]
- Access: EVENT
- POR: 0
- Current Value: 0
- Enumerated Value: VSYS not in SHUTDOWN
- Chipmodel Blocks: PMC: E_VSYS_SHUTDOWN
- Description: VSYS SHUTDOWN Event register.

Note:

Beside normal VBUS plug in/out condition, E_VBUS_OK and E_VBUS_UV events asserted by REV_VBUS on/off

INTERRUPT MASK REGISTERS

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

Interrupt mask bits

Register	Masked
M_VBUS_VINDPM	Masked
M_VBUS_IINDPM	Masked
M_VMID_OC	Masked
M_VBAT_OC	Masked
M_VBUS_OK	Masked
M_VMID_OK	Masked
M_VSYS_OK	Masked
M_VBAT_OK	Masked
0x000A	0xFF

Register	Masked
M_VBUS_OV	Masked
M_VMID_OV	Masked
M_VSYS_OV	Masked
M_VBAT_OV	Masked
M_VBUS_LUV	Masked
M_VMID_LUV	Masked
M_VSYS_LUV	Masked
M_VBAT_LUV	Masked
0x000B	0xFF

Register	Masked
M_TSD_CRIT	Masked
M_TSD_WARN	Masked
M_WD_TIMER	Masked
M_CHG_HOT	Masked
M_TS_WARM	Masked
M_TS_COOL	Masked
M_TS_COLD	Masked
M_TS_OFF	Masked
0x000C	0xFF

Register	Masked
M_CHG_SLEEP	Masked
M_CHG_SPLMT	Masked
M_CHG_TIMER	Masked
M_CHG_TRICKLE	Masked
M_CHG_PRE	Masked
M_CHG_CC	Masked
M_CHG_CV	Masked
M_CHG_DONE	Masked
0x000D	0xFF

Register	Masked
M_VSYS_SHUTDOWN	Masked
M_REF_OC	Masked
M_LDO2_IMON1	Masked
M_LDO2_IMON2	Masked
M_LDO2_OC	Masked
M_LDO1_IMON1	Masked
M_LDO1_IMON2	Masked
M_LDO1_OC	Masked
0x000E	0xFF

INT_N signal masked for all events (Default) which means INT_N no react while these events triggered.

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

Interrupt mask bits

Register	Masked
M_VBUS_VINDPM	Masked
M_VBUS_IINDPM	Masked
M_VMID_OC	Masked
M_VBAT_OC	Masked
M_VBUS_OK	Masked
M_VMID_OK	Masked
M_VSYS_OK	Masked
M_VBAT_OK	Masked
0x000A	0xFF

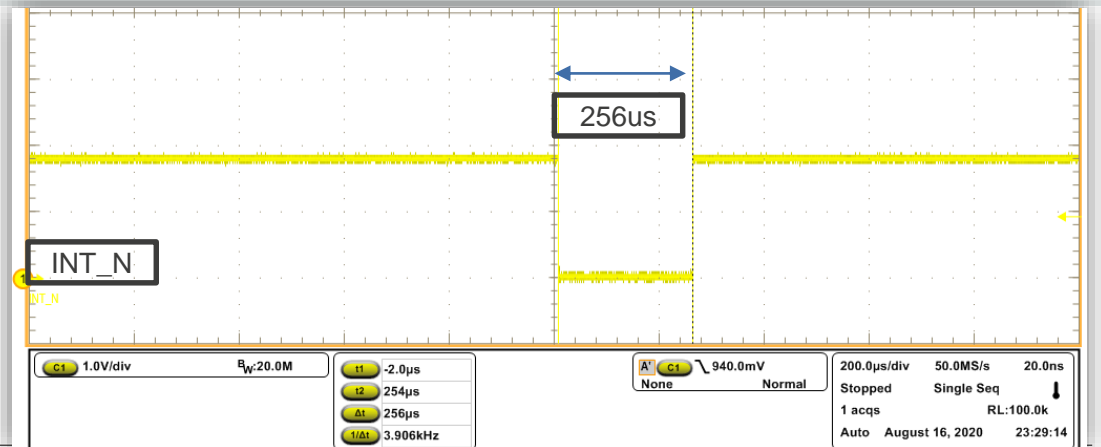
Register	Masked
M_VBUS_OV	Masked
M_VMID_OV	Masked
M_VSYS_OV	Masked
M_VBAT_OV	Masked
M_VBUS_LUV	Masked
M_VMID_LUV	Masked
M_VSYS_LUV	Masked
M_VBAT_LUV	Masked
0x000B	0xFF

Register	Masked
M_TSD_CRIT	Masked
M_TSD_WARN	Masked
M_WD_TIMER	Masked
M_TS_HOT	Masked
M_TS_WARM	Masked
M_TS_COOL	Masked
M_TS_COLD	Masked
M_TS_OFF	Masked
0x000C	0xFF

Register	Masked
M_CHG_SLEEP	Masked
M_CHG_SPLMT	Masked
M_CHG_TIMER	Masked
M_CHG_TRICKLE	Masked
M_CHG_PRE	Masked
M_CHG_CC	Masked
M_CHG_CV	Masked
M_CHG_DONE	Masked
0x000D	0xFF

Register	Masked
M_VSYS_SHUTDOWN	Masked
M_REF_OC	Masked
M_LDO2_IMON1	Masked
M_LDO2_IMON2	Masked
M_LDO2_OC	Masked
M_LDO1_IMON1	Masked
M_LDO1_IMON2	Masked
M_LDO1_OC	Masked
0x000E	0xFF

Example: M_CHG_DONE register is set as "Not masked"



SYSTEM REGISTERS

DA9168BC
File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

System

Chip ID

OTP_DEVICE_ID
DEV_ID: 215
0x0042 0xD7

OTP_VARIANT_ID
MRC: 1
VRC: 0
0x0043 0x10

OTP_CONFIG_ID
CONFIG_REV: 0
0x0044 0x00

System settings

PMC_SYS_00
E_RD_CLR_DIS: Low
VSYS_MIN: 3.7
VINDPM: 4.2
0x000F 0x38

PMC_SYS_01
VSYS_OV_SHUTDOWN_DIS: System
VSYS_UV_SHUTDOWN_DIS: System
ILIMIT_EN: No IINDPM update
IINDPM: 0.1
0x0010 0x00

PMC_SYS_02
BTS_VBAT_RATE: 50 ms
BTS_VBAT_EN: Disable
BTS_VBUS_RATE: 50 ms
BTS_VBUS_EN: Disable
VBAT_DEB: 100
VBUS_DEB: 100
0x0011 0x0A

PMC_SYS_03
SYS_WAIT: 1
WD_TMR: 160
WD_EN: No action
RST_TMR: 12
RST_REG: No action
0x0012 0x34

PMC_SYS_04
BOOST_PWM: Auto-mode
SEQ_BOOST: BOOST_EN is set w...
DLOAD_VMID_SEL: 30
DLOAD_VMID_EN: Disable
REV_VBUS_EN: Disable
BOOST_EN: Disable
0x0013 0x38

PMC_SYS_05
REV_VBUS_ILIM: 1.0
BOOST_VOUT: 5.0
0x0014 0x9A

PMC_SYS_06
RST_SYS: No action
RIN_N_SHIP_EXIT_TMR: 20 ms
VBUS_OVSEL: 5.6
HIZ_MODE: VBUS when available
SHIP_DLY: 10
SHIP_MODE: No action
0x0015 0x06

VSYS_OV_SHUTDOWN_DIS: Disable VSYS shutdown once VSYS_OV triggered
VSYS_UV_SHUTDOWN_DIS: Disable VSYS shutdown once VSYS_UV triggered
IINDPM_EN: IINDPM setting by ILIMIT pin option (Not support this function)
IINDPM setting: 0.1 A to 2.5 A with 0.1 A/step

BTS_VBAT_RATE: BAT temp sense interval @ battery operation
BTS_VBAT_EN: Enable BAT temp sense @ battery operation
BTS_VBUS_RATE: BAT temp sense interval @ VBUS supply present
BTS_VBUS_EN: Enable BAT temp sense @ VBUS supply present
VBAT_DEB: VBAT detection debounce time (ms)
VBUS_DEB: VBUS detection debounce time (ms)

Read-on-clear event register function enable/disable

VSYS minimum voltage setting: 3.4 V to 3.7 V with 0.1 V/step

VINDPM setting: 3.8 V to 4.8 V with 0.1 V/step

Boost operation mode option

Boost enable by EN pin option

VMID dummy-load setting (mA)

VMID dummy-load enable/disable

Reverse VBUS (OTG) enable/disable

Reverse boost enable/disable

Reverse boost VOUT setting: 4.0 V to 5.5 V with 0.1 V/step

Reverse VBUS (OTG) current limit setting: 0.1 A to 1 A with 0.1 A/step

SYS_WAIT: VSYS power-off time for system power recovery cycle (s)
WD_TMR: watch-dog timer expire time (s)
WD_EN: watch-dog timer enable/disable
RST_TMR: RIN_N button press time (s) to reset the system
RST_REG: Triggers registers initialization

System reset while set to high

RIN_N debounce time to exit from ship mode: 2 s/20 ms

VBUS over voltage threshold setting

HIZ mode option

Ship mode enter delay (s)

Ship mode enter/exit

Status

Console Log

Clear Mark Save to file Filter (reg expr): Log level: Info

2020-12-18, 10:43:42 [INFO] USB connected: U
2020-12-18, 10:43:42 [INFO] ready...
2020-12-18, 10:43:42 [INFO] Startup took: 0.90 sec
2020-12-18, 10:43:44 [INFO] no callables left to run...

Bitfield Info

Bitfield: WD_TMR
Register: PMC_SYS_03 (0x12)
Bits: [5:4]
Access: R/W
POR: 3
Current Value: 3
Enumerated Value: 160

CHARGER REGISTERS

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

Charger

Charger Settings

PMIC_CHG_00

BUCK_PWM PWM threshold unc...
 CHG_VRCHG 100
 CHG_TMR_HALF_EN Enable
 CHG_TMR_EN Enable
 CHG_TERM_EN Enable
 CHG_EN Disable

PMIC_CHG_01

CHG_TMR_SAFE 5
 CHG_TMR_PRE 30
 CHG_TOPOFF Disable-TOPOFF

PMIC_CHG_02

CHG_IPRE_MSB +0
 CHG_RANGE_TERM 5-25 mA, in 5
 CHG_RANGE_PRE 5-15 mA, in 5
 CHG_ITERM CHG_RANGE = 0 :
 CHG_IPRE CHG_RANGE = 0 :

PMIC_CHG_03

CHG_RANGE Fast-charge 20 mA...
 CHG_ICHG CHG_RANGE = 0 :

PMIC_CHG_04

CHG_VBATREG 4.20

PMIC_CHG_05

O_INT_N_PU Disable
 O_EN_PD Disable
 O_CHG_EN_N_PD Disable
 S_VBATREG_SHIFT 100
 CHG_TS_WARM_V Disable
 CHG_TS_COOL_I Disable

PMIC_CHG_06

S_ICHG CHG_RANGE = 0 :

0x0016 0x0E
 0x0017 0x00
 0x0018 0x0F
 0x0019 0x19
 0x001A 0x17
 0x001B 0x00
 0x001C 0x0C

BC Silicon New option at charging mode:

Recharge voltage threshold offset setting
 0: 100 mV; 1: 200 mV

Charger safety timer rate reduced to half while relevant events triggered.

Charger safety timer enable/disable

Charger termination enable/disable

Charger enable/disable
 (CHG_EN_N pin pulldown at the same time to enable charger)

CHG_TMR_SAFE: charger safty timer setting (h)
 CHG_TMR_PRE: Pre-charge safty timer setting (min)
 CHG_TOPOFF: Topoff timer setting (min) or disable

CHG_IPRE_MSB: Adds offset to pre-charge current setting (mA) while set to 1
 CHG_RANGE_TERM: Charging current range settings for CHG_ITERM. For Higher range, CHG_RANGE need set to 1
 CHG_RANGE_PRE: Charging current range settings for CHG_IPRE. For Higher range, CHG_RANGE need set to 1
 CHG_ITERM: Termination charge current setting (mA)
 CHG_IPRE: Pre-charge current setting(mA)

CHG_RANGE: Fast charge current range
 0: 20 mA to 500 mA
 1: 80 mA to 2000 mA
 CHG_ICHG: Fast charge current setting

Battery regulation voltage setting: 4.0V to 4.5V with 10mV/step

Fast charge current setting during TS event@ CHG_TS_COOL_I =1
 CHG_RANGE = 0: TS_ICHG 20 mA to 500 mA
 CHG_RANGE = 1: TS_ICHG 80 mA to 2000 mA

- IO_INT_N_PD: INT_N pin internal pull-up
- IO_EN_PD: EN pin internal pull-down
- IO_CHG_EN_N_PD: CHG_EN_N pin internal pull-down
- TS_VBATREG_SHIFT: Battery regulation voltage shift down 100 mV/200 mV during temp sense warm event triggered @ CHG_TS_WARN_V=1

Status Console Log

Clear Mark Save to file Filter (reg expr): Log level: Info

Bitfield Info

Bitfield: CHG_RANGE
 Register: PMIC_CHG_03 (0x19)
 Bit: [7]
 Access: R/W
 POR: 0

Current Value: 0
 Enumerated Value: Fast-charge 20 mA to 500 mA in 5 mA steps, also forces CHG_RANGE for CHG_ITERM and CHG_IPRE to 0

Chipmodel Blocks:
 PMC: CHG_RANGE

Description:

LDOs/LSWS REGISTERS

The screenshot displays the DA9168BC register configuration tool. The 'LDO' tab is active, showing settings for five LDOs: PMC_LDO_00, PMC_LDO_01, PMC_LDO_02, PMC_LDO_04, and PMC_LDO_05. Each LDO has a set of configuration options, including enable/disable buttons, sequence options, and current limit settings. A console window at the bottom shows log messages related to the configuration process.

LDOx OCP option:
 0: LDOx disable while trigger OCP
 1: LDOx hiccup while trigger OCP

LDOx PD SW option:
 0: LDOx PD switch disable
 1: LDOx PD switch enable

LDOx_LSW mode option:
 0: LDO mode
 1: Load SW mode

LDOx_EN:
 0: LDOx disable
 1: LDOx enable

LDOx sequence option:
 0: LDOx not enabled by EN pin
 1: Enable LDOx ASAP after EN pin rise
 2: Enable LDOx 0.25 ms after EN pin rise
 3: Enable LDOx 0.5 ms after EN pin rise

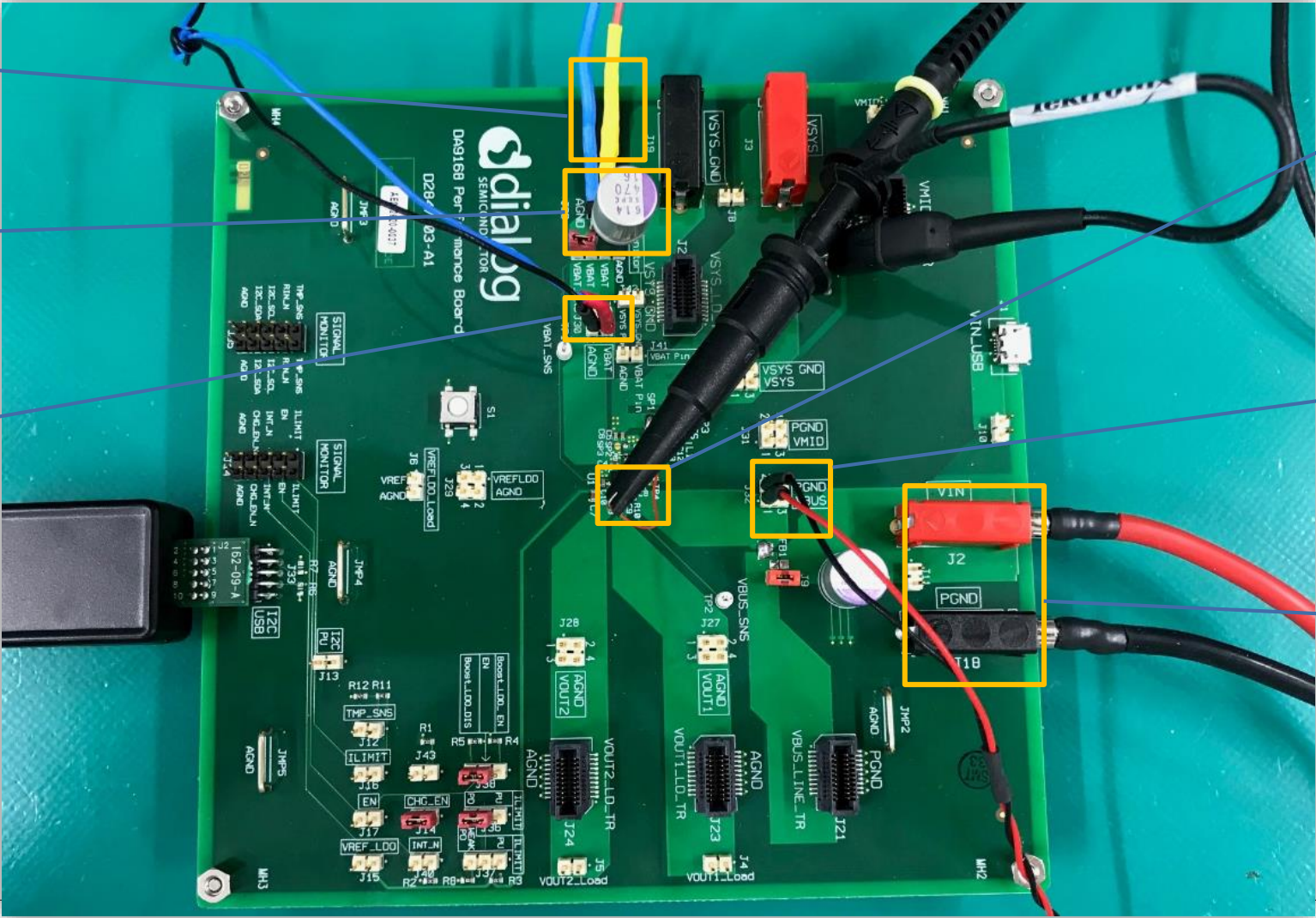
LDOx VOUT setting:
 1.6 V to 5.2 V with 0.1 V/step

LDOx current limit setting

New options for BC silicon

TEST BENCH SETUP

CHARGE MODE BOARD SETUP



VBAT Connection

VLX Signal

VBUS Sense

VBUS Connection

VBAT Sense

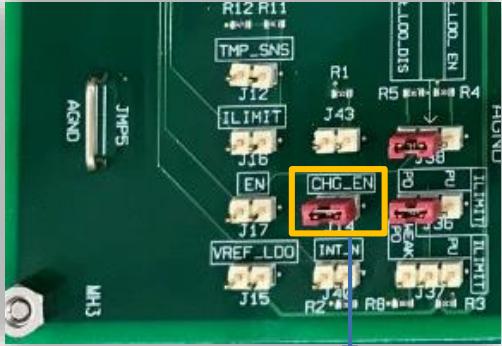
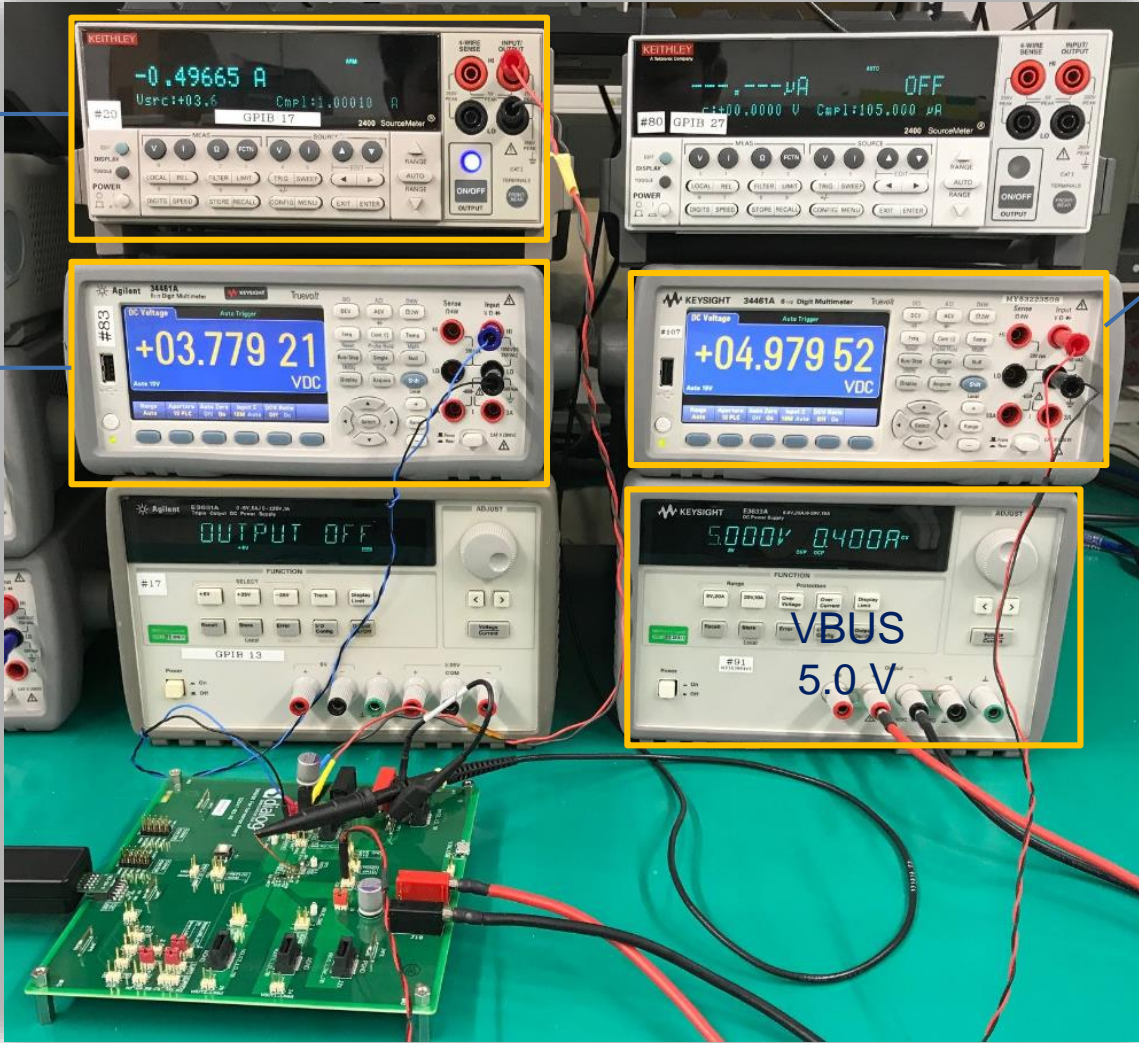
Highly recommend:
Bulk electrolytic cap for
VBAT connector to prevent
VBAT voltage oscillation due to
the long cable

CHARGE MODE TEST BENCH SETUP

VBAT charging current

VBAT Sense
3.779 V

VBUS Sense
4.979 V



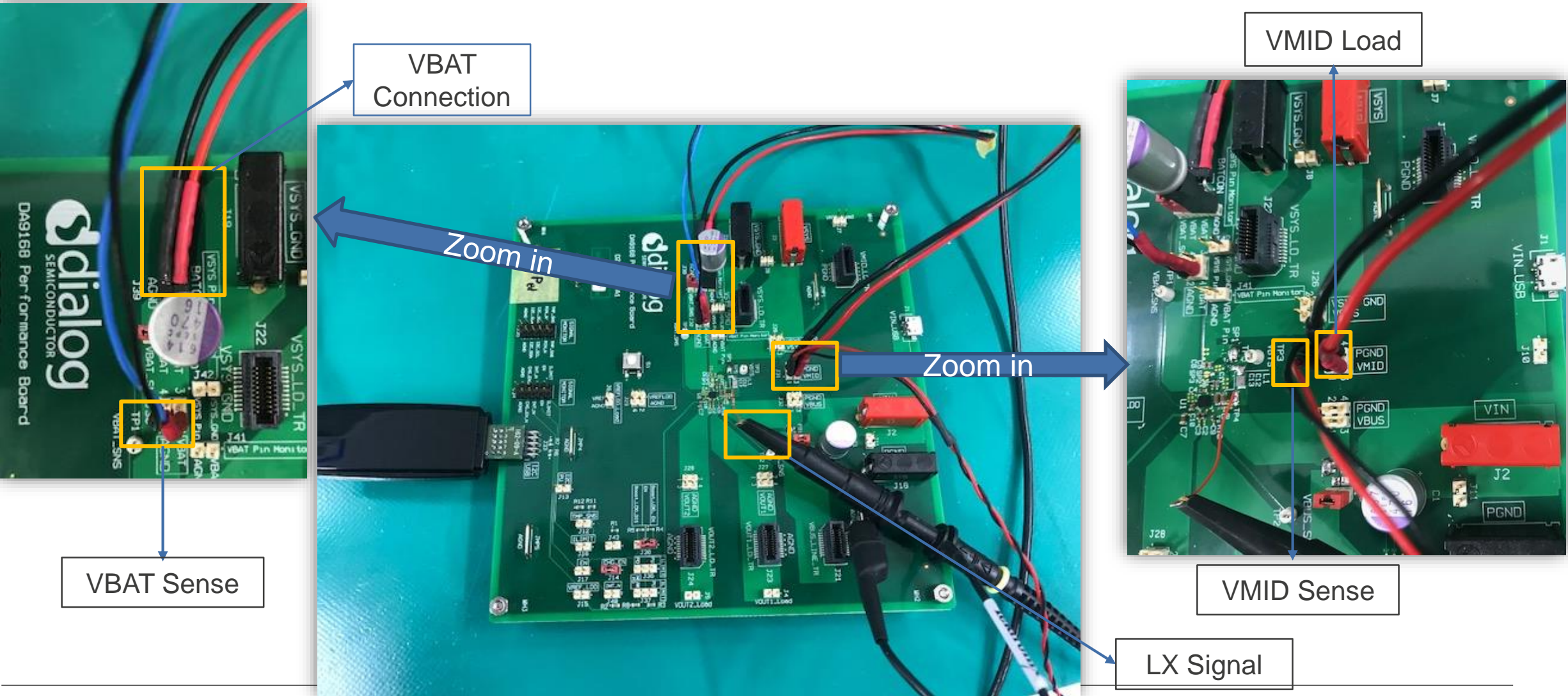
CHG_EN_N pin pulldown

PMC_CHG_00

BUCK_PWM	Auto-mode
CHG_VRCHG	100
CHG_TMR_HALF_EN	Enable
CHG_TMR_EN	Enable
CHG_TERM_EN	Enable
CHG_EN	Enable
0x0016	0x0F

CHG_EN set to High

REV-BOOST MODE BOARD SETUP



REV-BOOST MODE TEST BENCH SETUP

VMID Load (200 mA)

VMID Output 4.982 V

VBAT Sense 3.68 V

VBAT 3.7 V

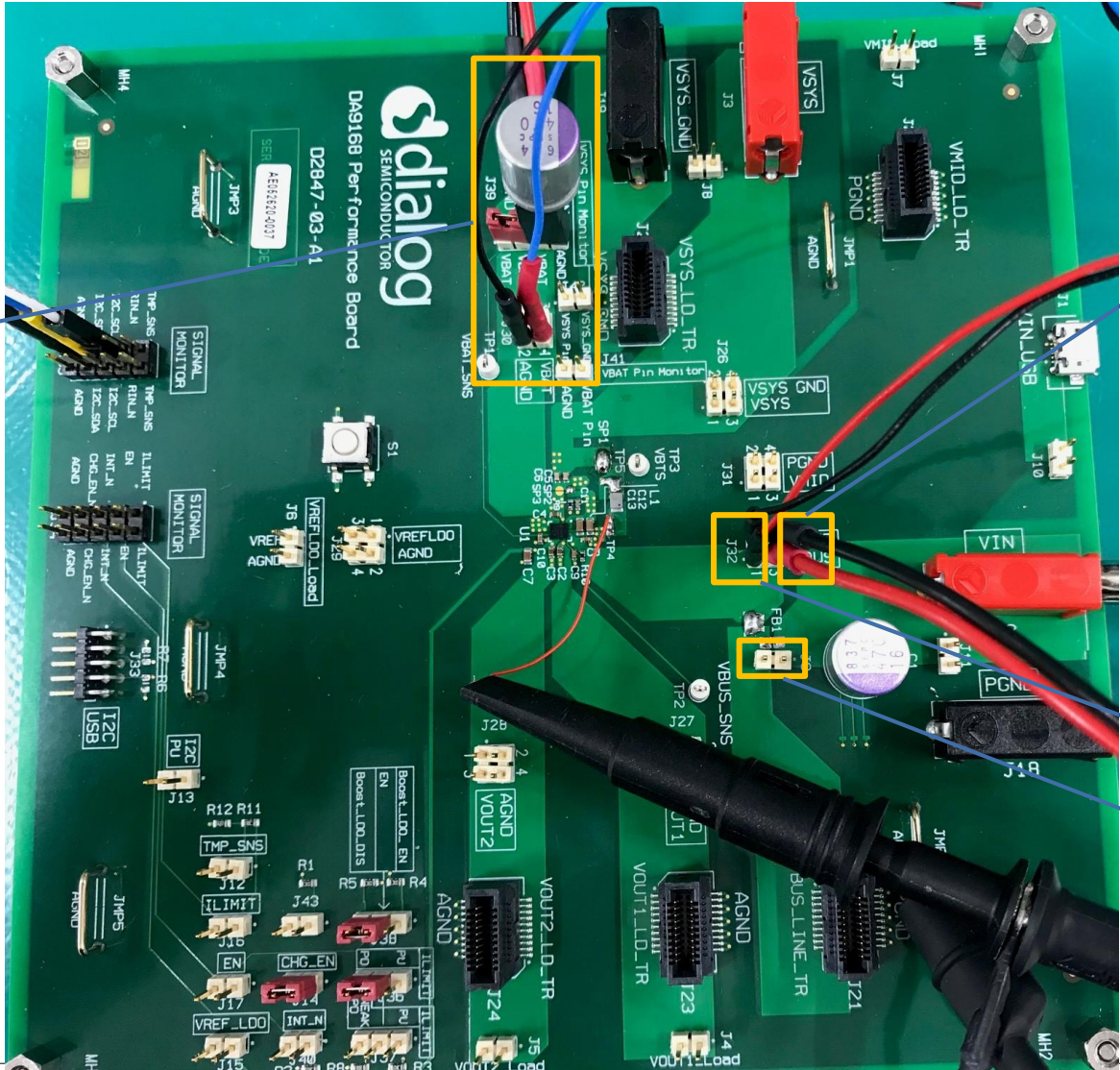
PMCSYS04

BOOST_PWM	Auto-mode
SEQ_BOOST	BOOST_EN is set w...
DLOAD_VMID_SEL	30
DLOAD_VMID_EN	Disable
REV_VBUS_EN	Disable
BOOST_EN	Enable
0x0013	0x39

BOOST_EN set to High

REV-VBUS (OTG) BOARD SETUP

VBAT and VBAT sense connections are same with Rev_boost setup

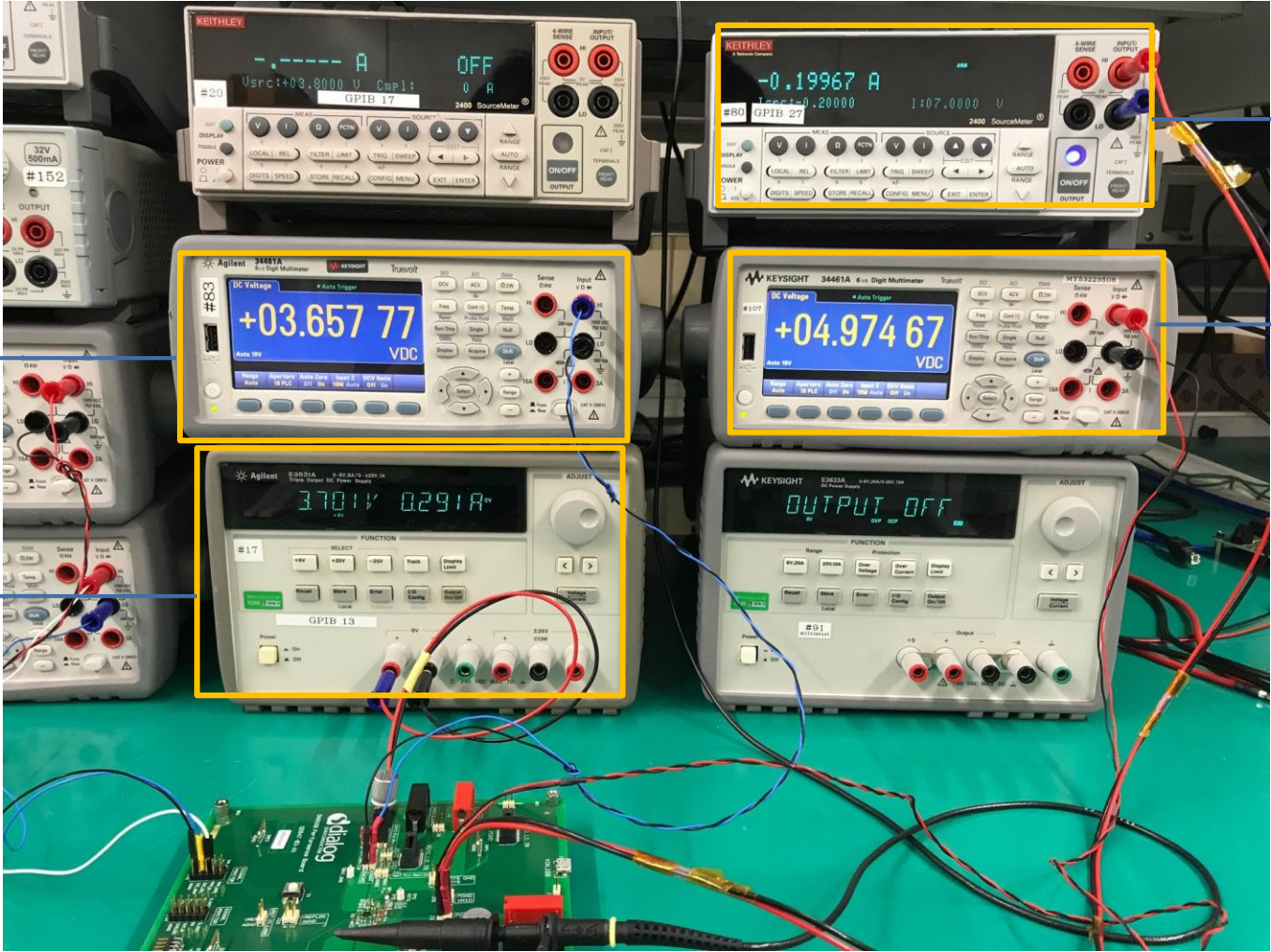


Rev-VBUS Load

Rev-VBUS Sense

Remove jumper J9

REV-VBUS (OTG) TEST BENCH SETUP



VBAT Sense
3.657 V

VBAT
3.7 V

Rev-VBUS Load
(200 mA)

Rev-VBUS Output
4.974 V

PMC_SYS_04

BOOST_PWM	Auto-mode
SEQ_BOOST	BOOST_EN is set w...
DLOAD_VMID_SEL	30
DLOAD_VMID_EN	Disable
REV_VBUS_EN	Enable
BOOST_EN	Enable
0x0013	0x3B

REV_VBUS_EN set to High
BOOST_EN set to High

[Renesas.com](https://www.renesas.com)