Application note

DA9210 automotive

42 VF-BGA Layout Recommendation

AN-PM-040

DA9210 PCB Layout Recommendation for 42 VF-BGA

Abstract

This application note provides recommendations for placing and routing the DA9210 device, 42 VF-BGA automotive variant. It also describes the passive components needed for proper functioning of the device. Application developers should treat this document as a guideline, not as a hard requirement, since target applications may have different requirements.

Contents

Figures

1. Revision history

Version	Date	Description
1.0	Sep 2014	Initial revision.

2. Terms and definitions

BGA	Ball Grid Array
PCB	Printed Circuit Board
PTH	Plate Through-Hole

3. References

1. DA9210, Data sheet, Dialog Semiconductor

4. Introduction

DA9210 is a 4-phase Buck converter, capable of delivering a 12 A output current with an input voltage range of 2.8 to 5.5 V and an output voltage range of 0.3 to 1.57 V. The basic recommended components and connections for single chip operation are shown in Figure 1.

The layout recommendations in section 5 are related to the schematic drawing below.

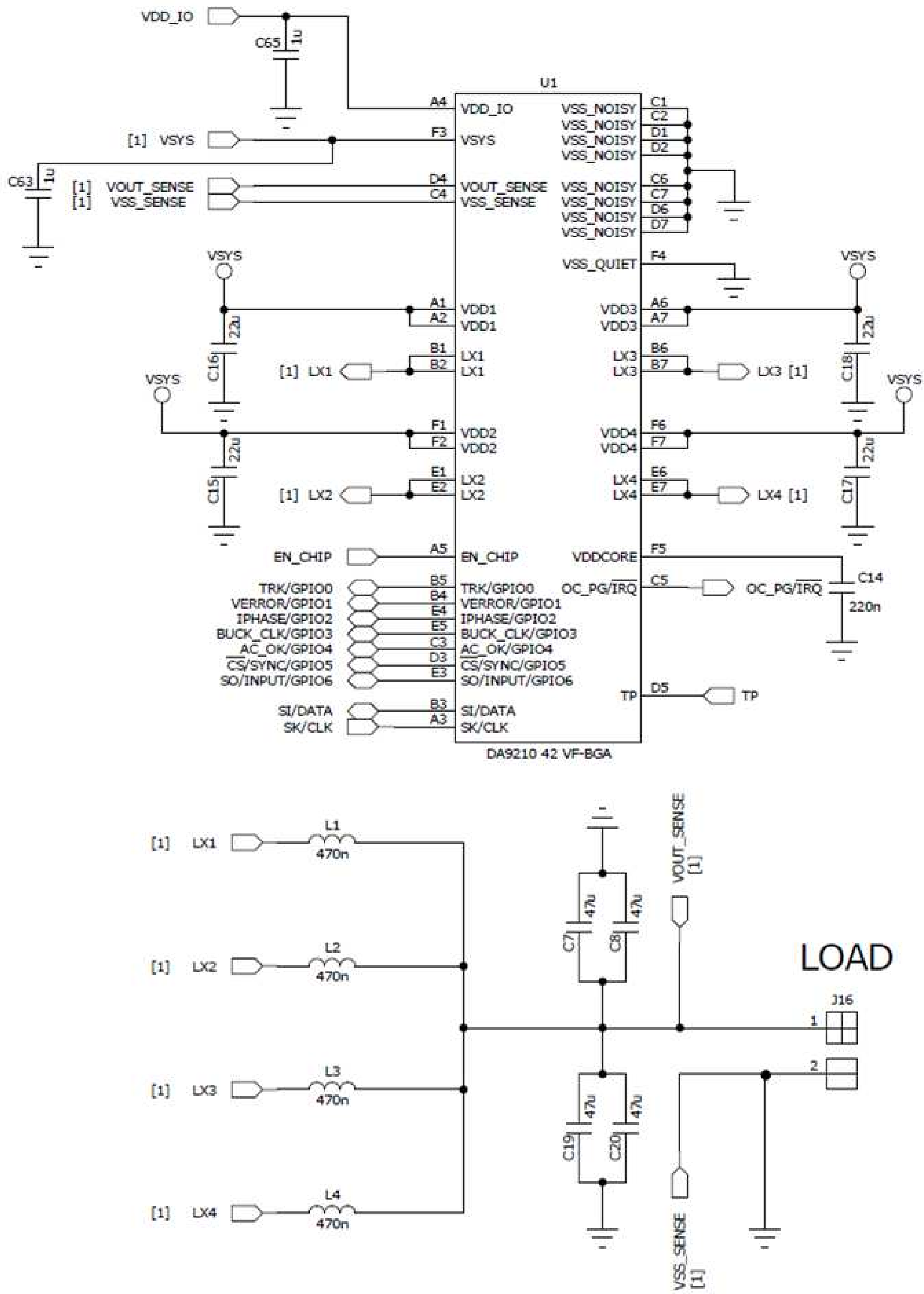

Figure 1: Schematic drawing

5. Layout recommendations

The automotive version of DA9210 is packaged in a 42-pin VF-BGA with a 0.8 mm pitch. The footprint is designed such that the PCB layout can be done using standard drilled PTH VIAs.

The PCB layout can be done with a 4-layer PCB stack-up however, when the device is part of a more complex system, the number of routing layers and other PCB parameters are determined by the ecosystem as a whole.

This chapter is divided into several sections, ranked by priority from the most important to less critical layout tasks:

- Package information, section 5.1
- Multiphase Buck convertor, section 5.2
- Reference voltage, section 5.3
- Communication interfaces, section 5.4
- GPIOs and control signals, section 5.5

Each of the blocks has separate design rules. The ball map in section 5.1 is given as additional information to help in understanding the PCB diagrams in the remainder of the document.

5.1 DA9210 automotive package information

5.1.1 DA9210 ball map

Figure 2: DA9210 42VF-BGA ball map

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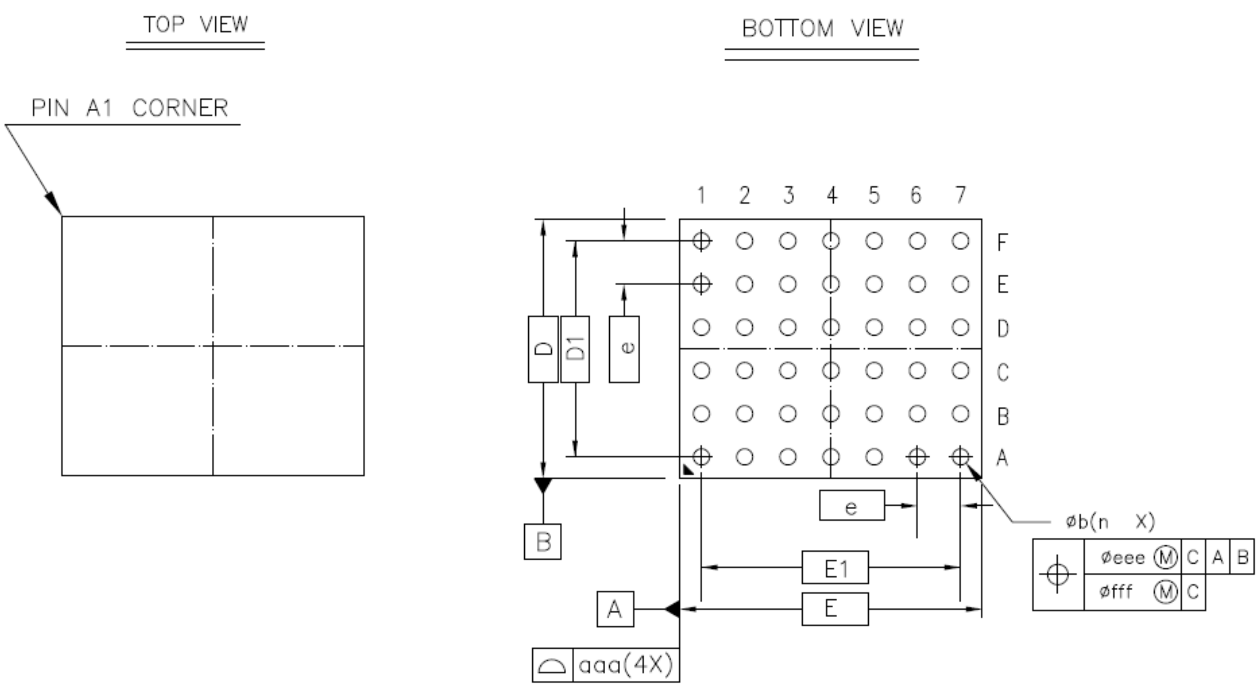
Table 1: DA9210 42VF-BGA pin list

Pin 42 VF-BGA	Signal name	Alternate function	Type	Description
B1, B2	LX1		AO	Switching node for phase 1
E1, E2	LX2		AO	Switching node for phase 2
B6, B7	LX3		AO	Switching node for phase 3
E6, E7	LX4		AO	Switching node for phase 4
A1, A2	VDD1		PS	Supply voltage for phase 1 To be connected to VSYS
F1, F2	VDD2		PS	Supply voltage for phase 2 To be connected to VSYS
A6, A7	VDD3		PS	Supply voltage for phase 3 To be connected to VSYS
F6, F7	VDD4		PS	Supply voltage for phase 4 To be connected to VSYS
A5	EN_CHIP		DI	IC Enable Signal
C5	OC_PG	nIRQ	DO	Output for Over Current Alarm and Power Good signal, IRQ line towards the host
A4	VDD_IO		PS	I/O Voltage Rail
D4	VOUT_SENSE		AI	Output and Sense node for the Buck
C4	VSS_SENSE		AI	Ground Sense node for the Buck
F5	VDDCORE		AO	Regulated supply for internal circuitry (decouple with 220 nF)
B5	GPIO0		AI/DIO	General purpose I/O
B4	Verror	GPIO1	AIO/DIO	Error Amplifier Voltage Signal for dual parallel mode, general purpose I/O
E4	Iphase	GPIO2	AIO/DIO	Current Distribution Signal for dual parallel mode, general purpose I/O
E5	BUCK_CLK	GPIO3	DIO	Buck Clock Input/Output (depending on slave/master function in dual parallel mode), general purpose I/O
C3	AC_OK	GPIO4	DIO	Input from safe charger out to OC_PG signaling, general purpose I/O, input of external 6 MHz clock
D3	nCS/SYNC	GPIO5	DIO	4-WIRE chip select, DVC Interface input clock , general purpose I/O
E3	SO/INPUT	GPIO6	DIO	4-WIRE Data Output, DVC Interface input data, general purpose I/O
B3	SI	DATA	DIO	4-WIRE Data Input, 2-WIRE Data
A3	SK	CLK	DI	4-WIRE/2-WIRE Clock
D5	TP		DIO	Test pin, connect to VSS
F3	VSYS		PS	Supply for IC and input for voltage supervision
F4	VSS_QUIET		VSS	
C1, C2, D1, D2, C6, C7, D6, D7	VSS_NOISY		VSS	

5.1.2 Package outline drawing



		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package :				MFC VFBGA	
Body Size:	X	E		5.600	
	Y	D		4.800	
Ball Pitch :		e		0.800	
Total Thickness :		A	0.850	0.920	0.990
Mold Thickness :		M		0.540 Ref.	
Substrate Thickness :		S		0.170 Ref.	
Ball Diameter :				0.300	
Stand Off :		A1	0.160	–	0.260
Ball Width :		b	0.270	–	0.370
Package Edge Tolerance :		aaa		0.070	
Mold Parallelism :		bbb		0.100	
Coplanarity:		ddd		0.080	
Ball Offset (Package) :		eee		0.120	
Ball Offset (Ball) :		fff		0.050	
Ball Count :		n		42	
Edge Ball Center to Center :	X	E1		4.800	
	Y	D1		4.000	

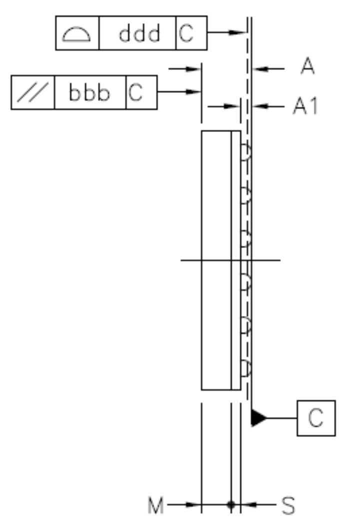


Figure 3: DA9210 42 VF-BGA package drawing

5.2 Multi-phase Buck converter

The DA9210 follows the standard Buck design procedure with output capacitors placed as close as possible to the load/processor and “remote voltage sensing”. For this reason, and because of the high currents which the device can deliver, a wide output plane for minimized parasitic impedance is highly desirable.

Differential feedback lines must be taken from the load point and routed back carefully to the DA9210 pins to precisely control the voltage at the load point. This is described in the next sections. As an example, a 4-layer PCB was designed using PTH via technique as shown in Figure 4.

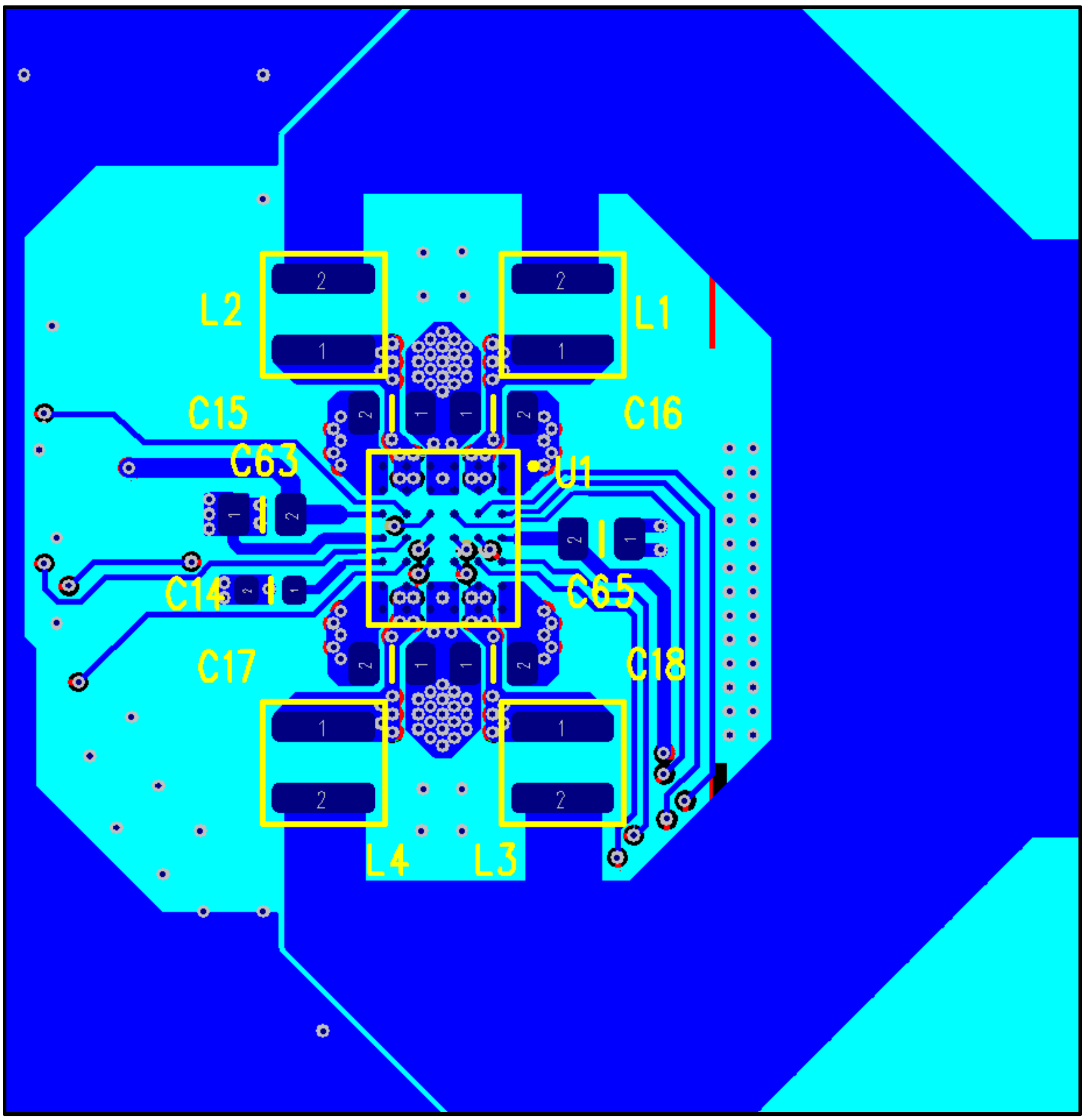


Figure 4: Example of components placement on 4-layer PCB

5.2.1 Device grounding

Due to the high current levels and high performance requirements in DA9210, grounding of the device and ground patterns are fundamental aspects of the PCB layout.

In the 42 VF-BGA, the ground terminals are placed at the periphery of the package and should be connected in the best and fastest possible way to the ground plane of the PCB. This is unlike the 48 WL-CSP package variant of DA9210, where the ground terminals are placed in the central area of the device.

It's also important that in the 42 VF-BGA, the ground signals of different phases do not include parasitic resistances and asymmetric paths.

This is achieved by placing the highest possible number of drilled PTH VIAs, as shown in Figure 5 (red circles). In this example, layer 2 of the PCB is used as ground plane. This is directly underneath the device and is probably the best choice in terms of device stability and noise reduction.

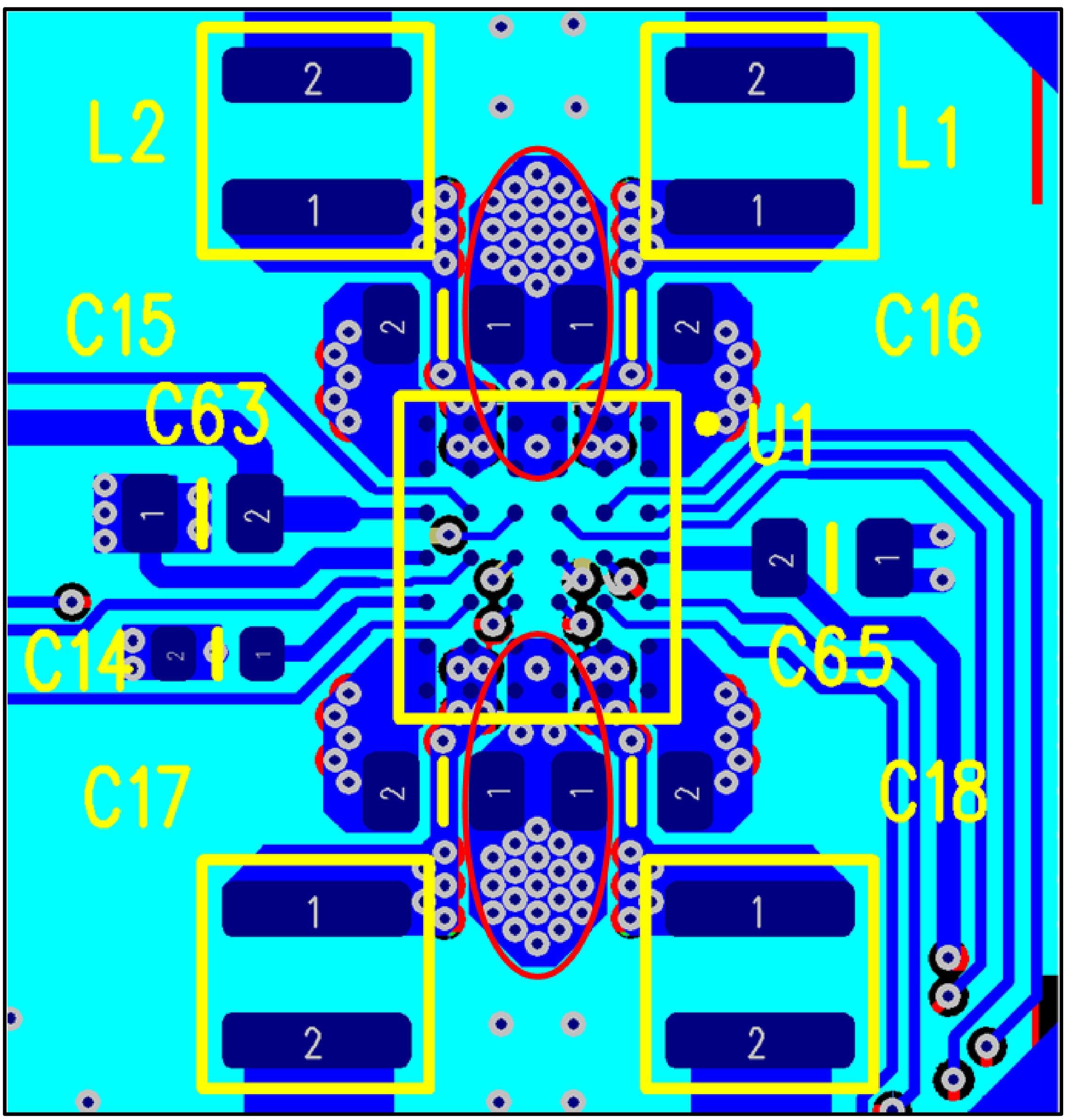


Figure 5: Device ground connection

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The PTH VIAs of signals other than ground must be placed carefully around the device to keep the ground copper gaps between the device ground VIAs and the internal ground planes large enough for a good, stable ground connection.

Figure 6 shows how this can be achieved.

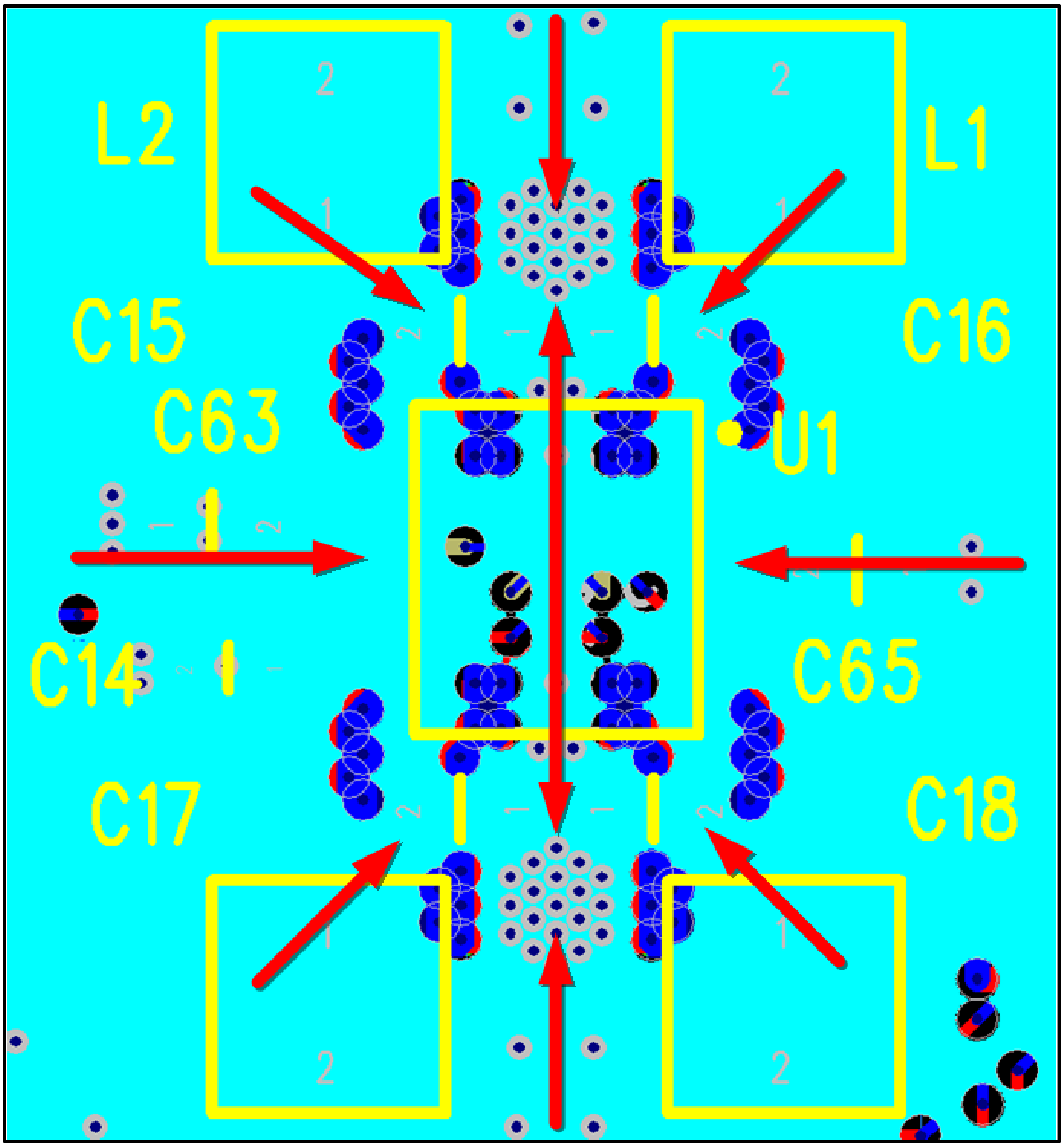

Figure 6: Device ground connection

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The ground pins of DA9210 are identified as VSS_NOISY and VSS_QUIET, where the “NOISY” pins are intended for use by the pass devices of different phases and the “QUIET” pin is connected to sensitive analogue circuits.

VSS_QUIET should be connected to a quiet area of ground (GND terminal of C63) to achieve the best device performance and grant stability. Figure 7 shows how this is can be done in our example.

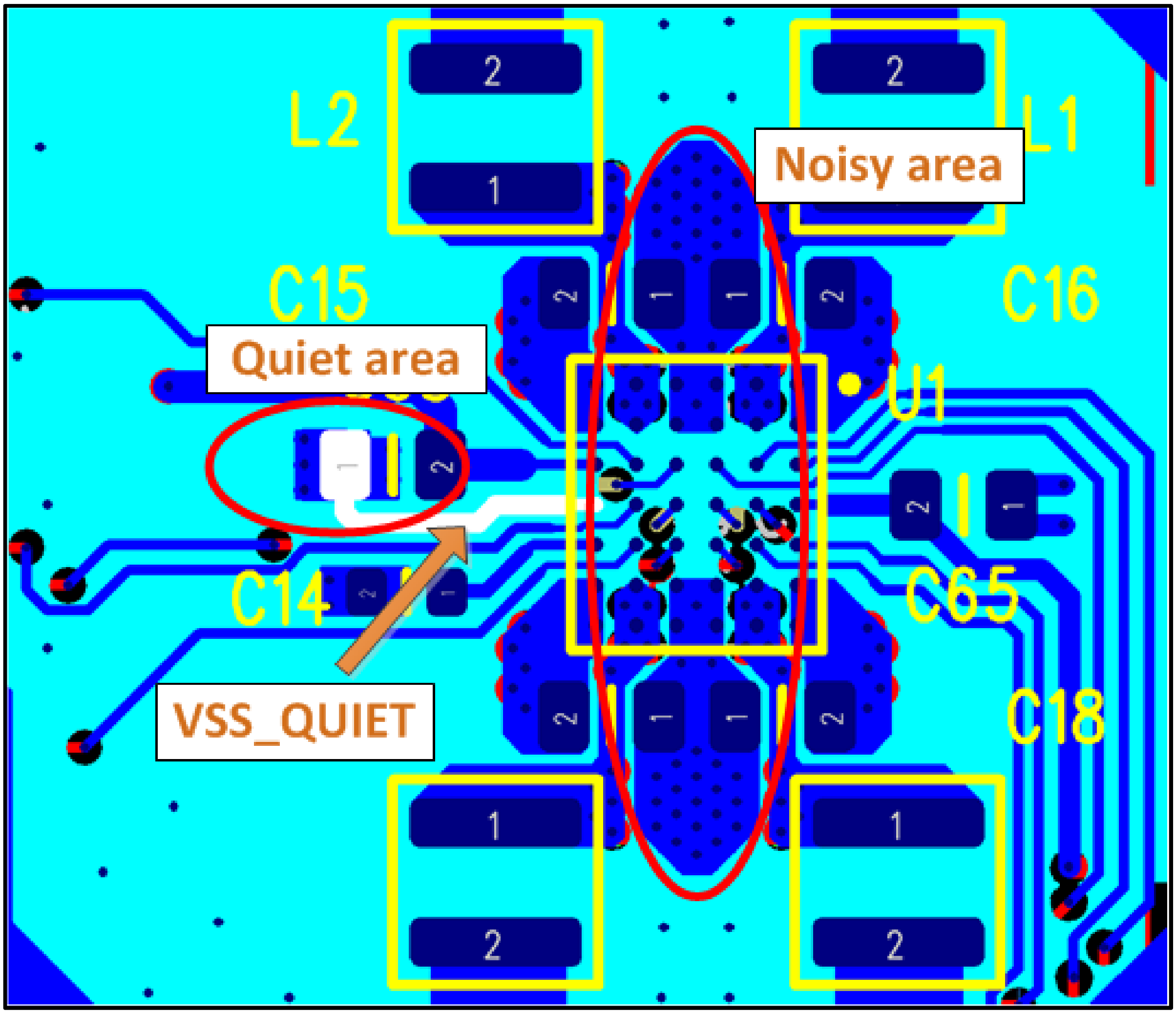

Figure 7: VSS_QUIET connection

5.2.2 Buck power supply input pins

As for the ground connection of the device, special attention is also required for the supply input pins.

At least four input capacitors are needed, each connected to VDD of the related phase input. Recommended capacitor values are 10 or 22 µF, 6.3 V, 0603 footprint, X5R (C15, C16, C17 and C18 in Figure 8).

The input capacitors should be connected as close as possible to DA9210 and create an input filter directly on the top layer, as shown in Figure 8. The ground of the input capacitor can be easily shared with the VSS_NOISY top layer area.

Note that as a good connection is required between the capacitor and the VDD plane, in our example a number of drilled PTH VIAs are placed close to the capacitor landing pad.

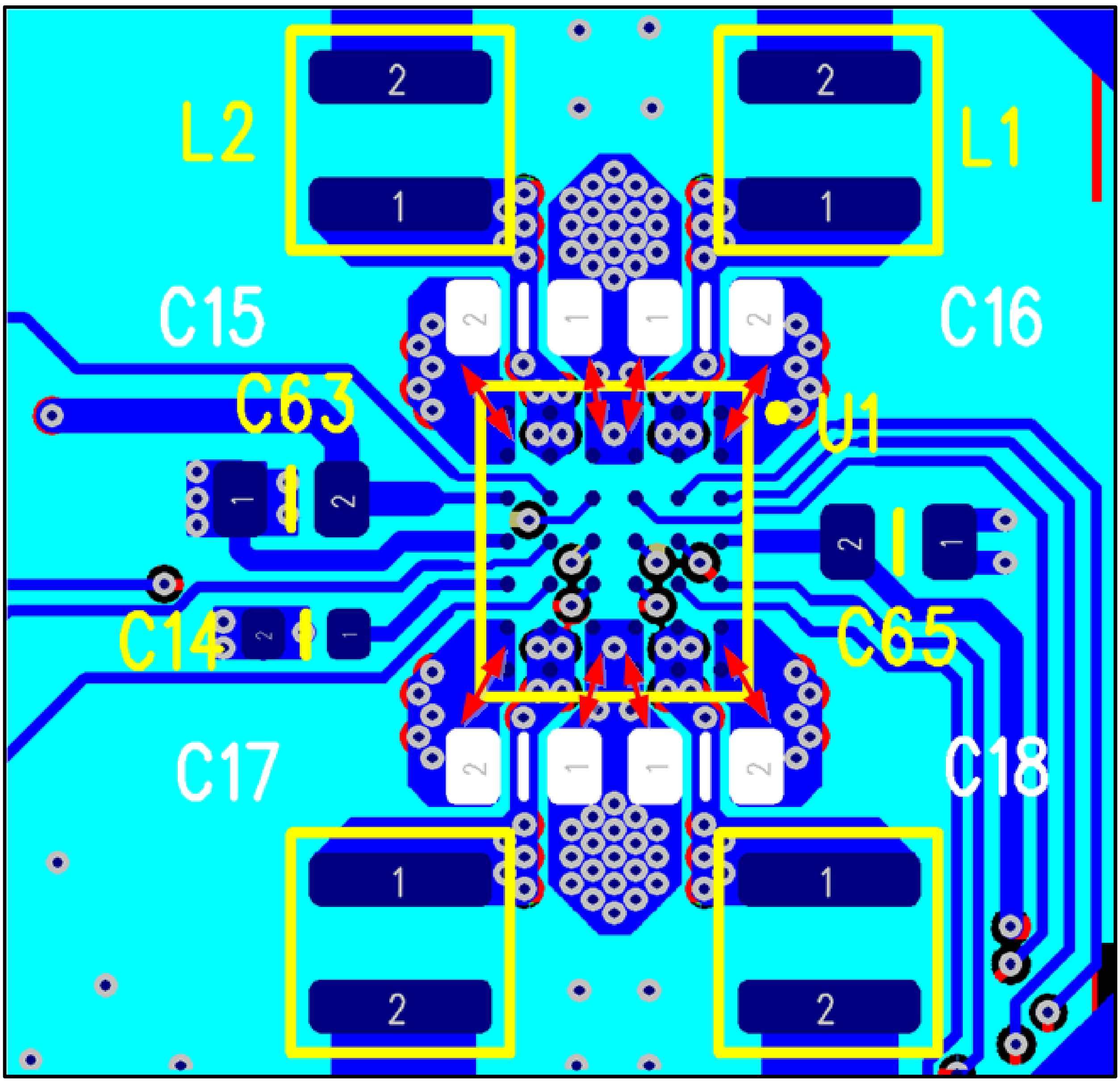

Figure 8: Input capacitors, placement and routing

DA9210 has an additional input pin called VSYS, which is a quiet supply pin for the sensitive analogue circuits, and has a separate capacitor (C63 in Figure 9) with a recommended value of 1 µF, 6.3 V, 0402 footprint, X5R or X7R.

This is basically the same net (power supply) as for the 4-phase Buck inputs, but a separate trace is routed from C63 to the VSYS pin and no merging with the Buck input lines or planes is allowed.

It is also recommended that the decoupling capacitor C65 (1 µF, 6.3 V, 0402 footprint, X5R or X7R) is placed on the VDD_IO line to suppress noise on this input.

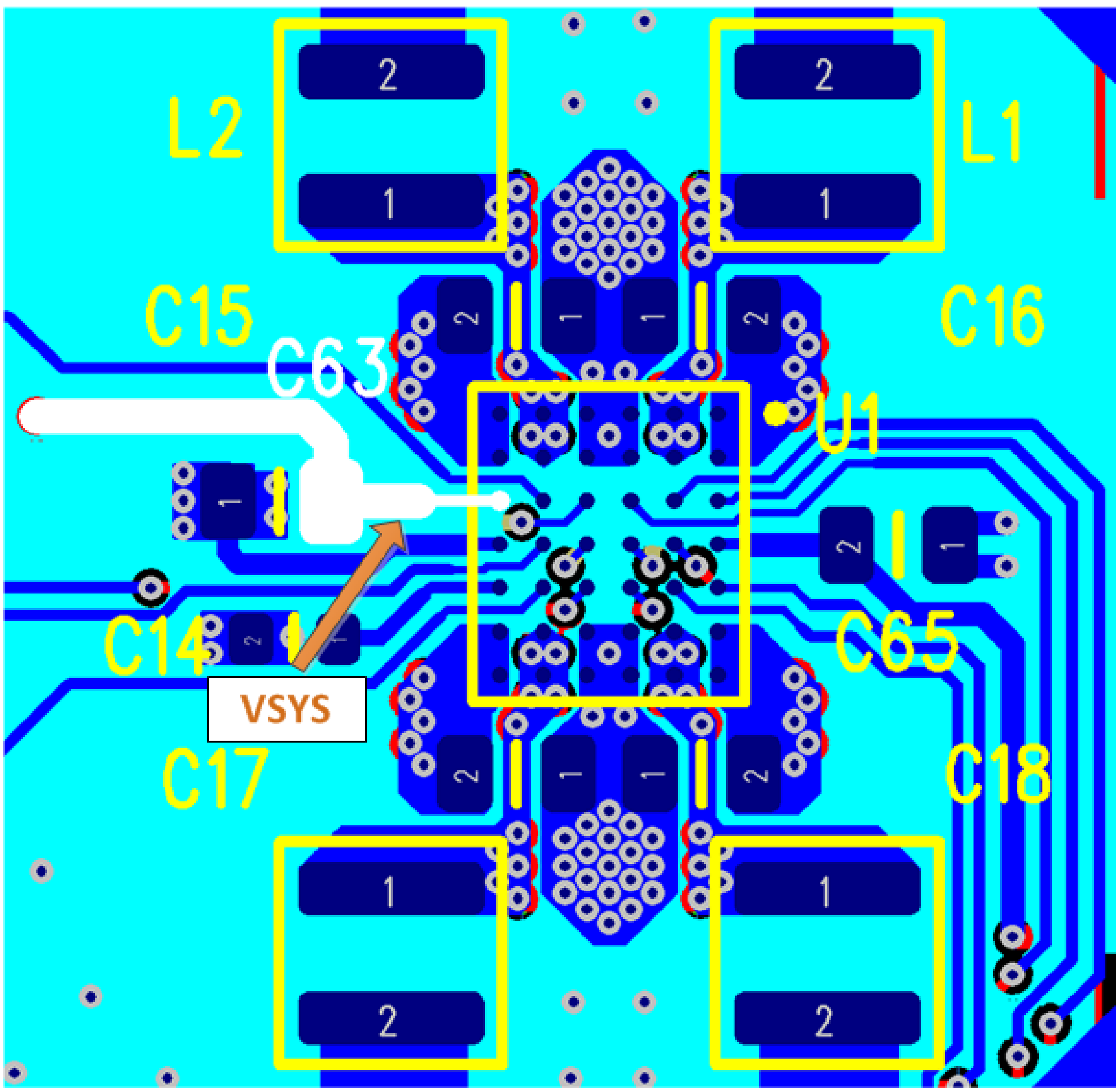

Figure 9: Power supply capacitors

5.2.3 Buck output

DA9210's output inductors should be placed as shown in Figure 10. Note that regarding EMI issues in system design, the traces or planes between the output LX pins and inductor terminals should be as short as possible to reduce the emission to the minimum.

Particular care must be taken when dimensioning the line width as the parasitic resistance must be reduced as much as possible - a maximum peak output current of more than 4 A can be experienced on the trace at maximum load. With the increase of parasitic trace resistances, the overall converter efficiency decreases accordingly.

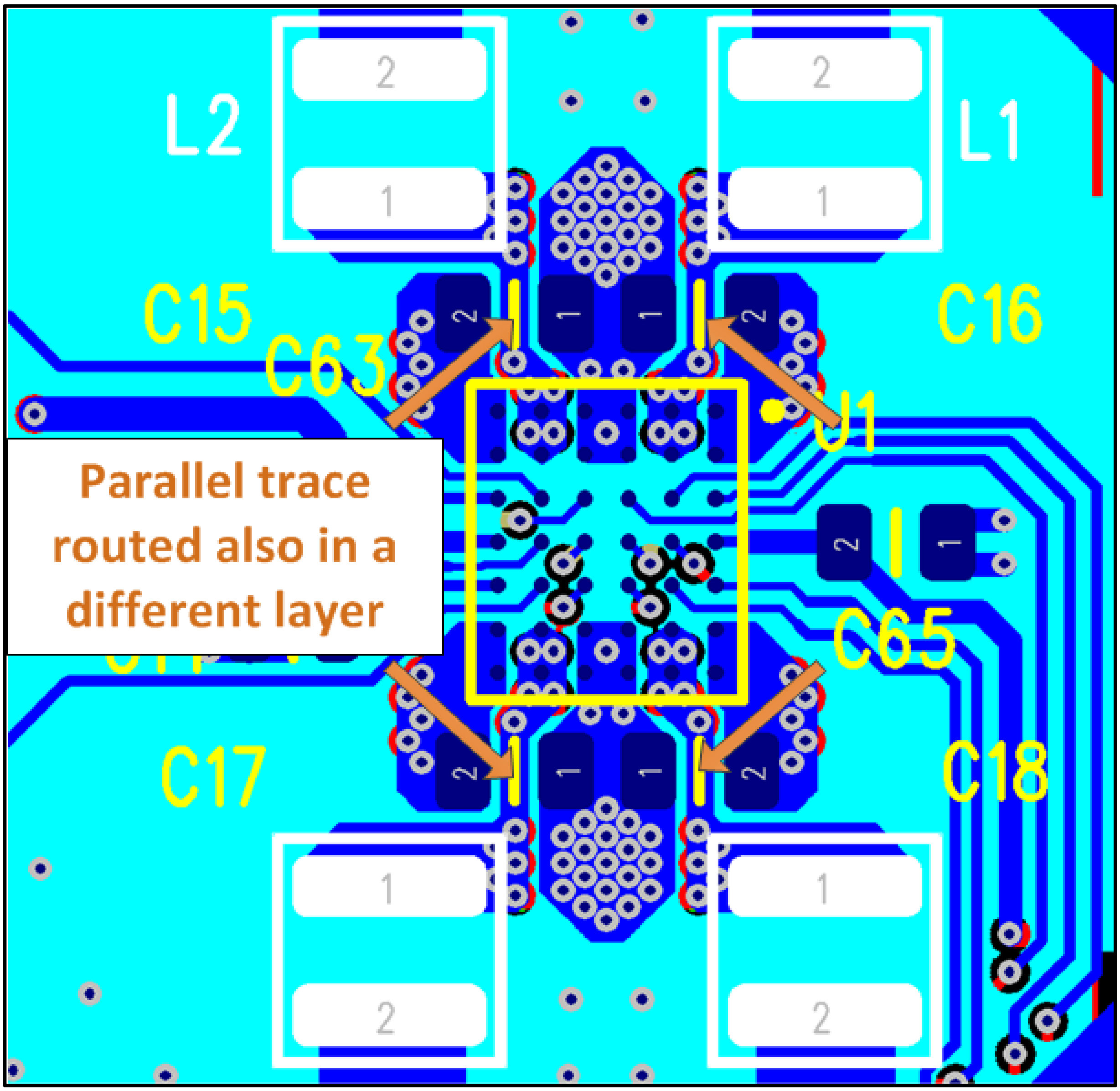

Figure 10: Inductors, placement and routing

Shielded inductors of 0.47 µH and at least 3.5 or 4 A of saturation current are recommended. If the system design allows it, the best performance is achieved by transferring the output current directly on the top layer, without using any VIAs. However this is not possible when routing traces from chip LX nodes to output inductors because of the position of the input capacitors to reduce input impedance. A parallel trace on a different layer can be considered (as in the example in Figure 11) to minimize the resistance of the output track.

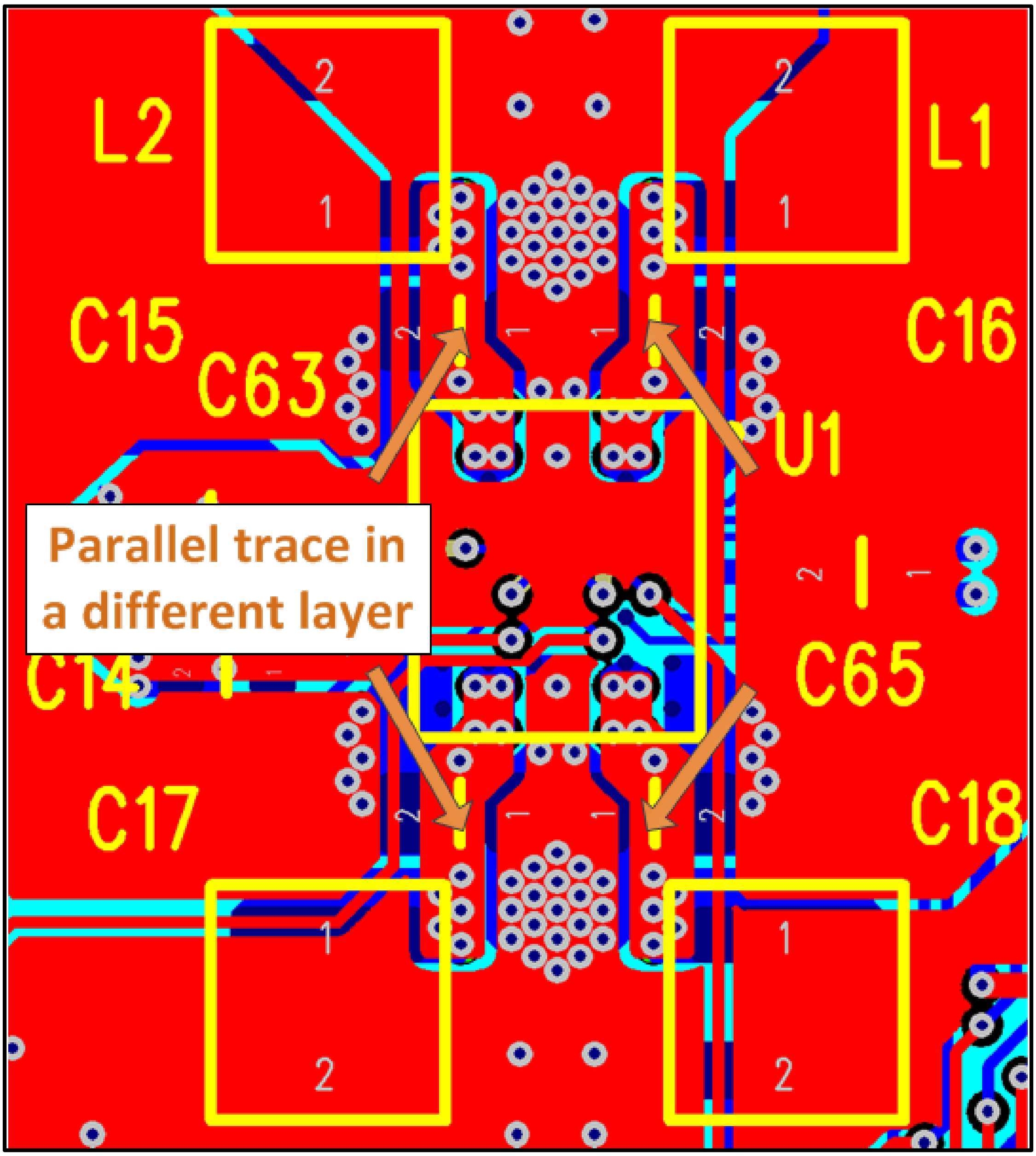

Figure 11 Parallel output trace

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Care must be taken regarding the width of the traces or output plane, since the merged output peak current can be up to 12 A. The output plane should form another capacitor with the ground plane on layer 2, an example of how the overall system should look is shown in Figure 12.

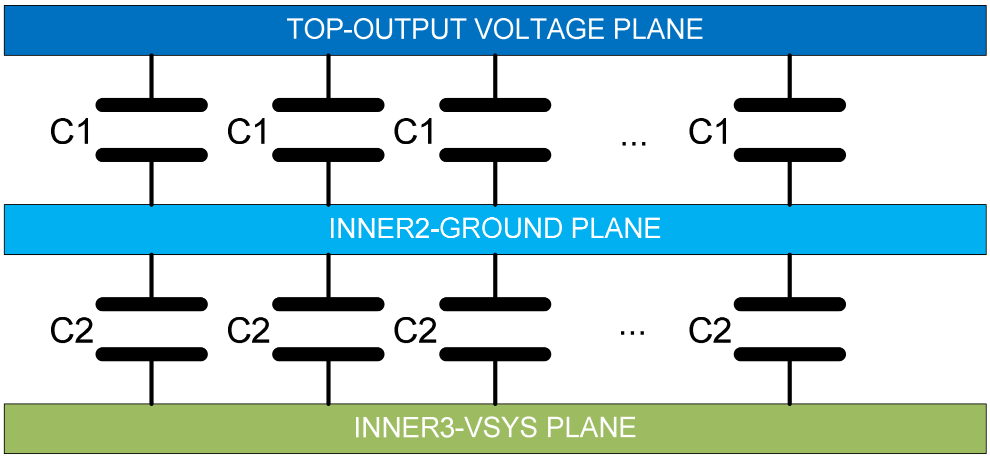

Figure 12 Plane structure filtering

Output capacitors should be placed close to the load. The DA9210 is designed in such a way that it compensates the influence of the long distance between the inductors and output capacitors.

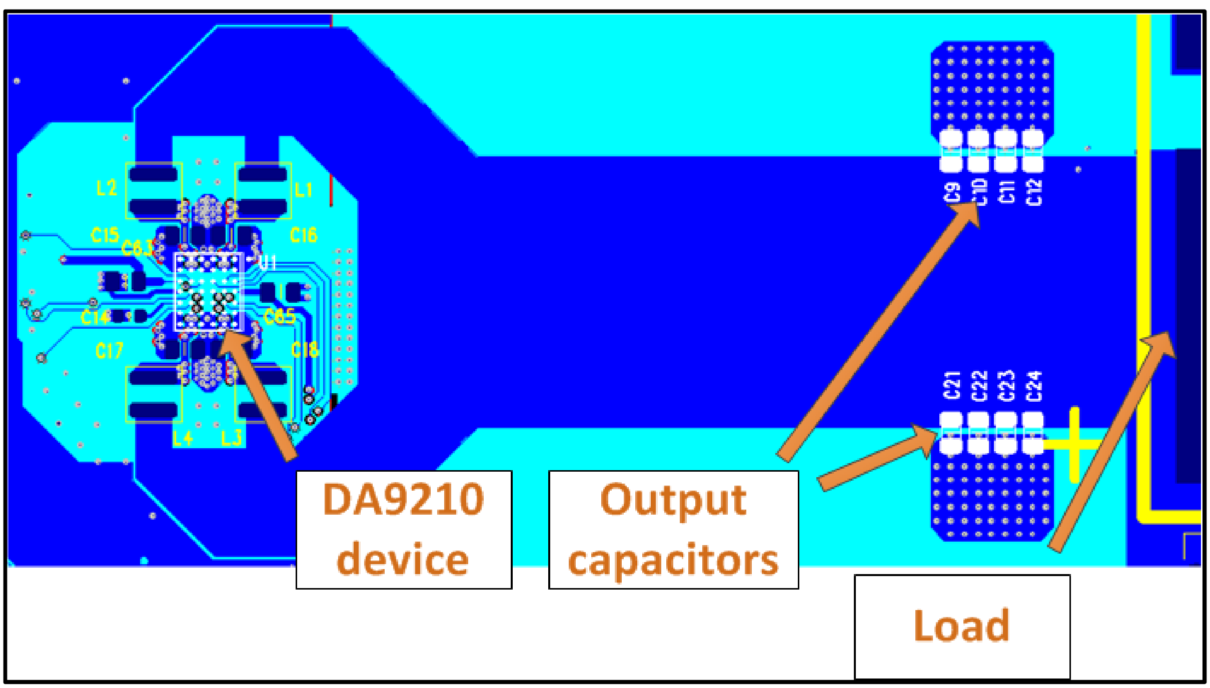

Figure 13 Output capacitors placement

For use as output capacitors, 4 x 47 µF, 4 V, 0603 or 4 x 47 µF, 4 V, 0805 footprint, X5R, or 8 x 22 µF, 6.3 V, 0603 footprint, X5R are recommended. System designers should decide which approach to use based on the total cost and the available space on the PCB.

5.2.4 Feedback lines

Special care has to be taken when placing the feedback lines. They must be routed far from any noise source (inductors, communication interfaces, and so on) and in a symmetric way.

The negative feedback line is at ground potential and care should be taken not to connect any part of the trace to the ground plane. The feedback lines must be routed from the load point in order to achieve the best voltage accuracy and stability at the load point. On a 4-layer PCB the recommended layer is layer 3 or layer 4 (bottom), but in general at least one insulation plane (ground or power layer) must be present between the top components and the feedback signals. Good feedback signal shielding is very important for Buck stability.

The number of used VIAs on the VOUT_SENSE and VSS_SENSE path should be minimised to avoid any potential noise coupling into feedback lines.

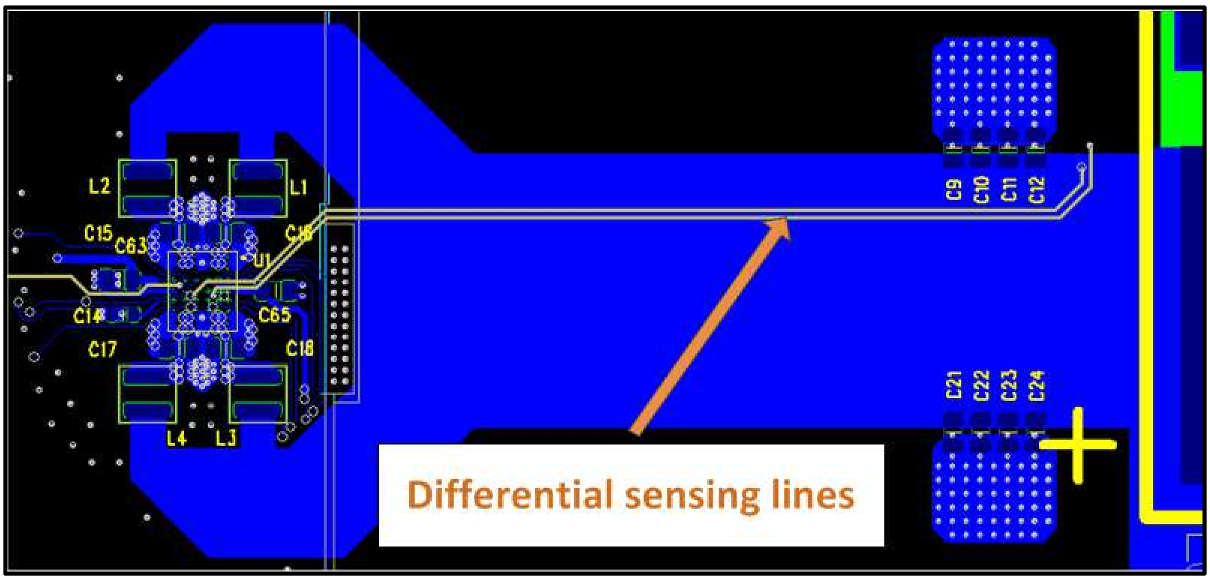

Figure 14 Feedback lines routing

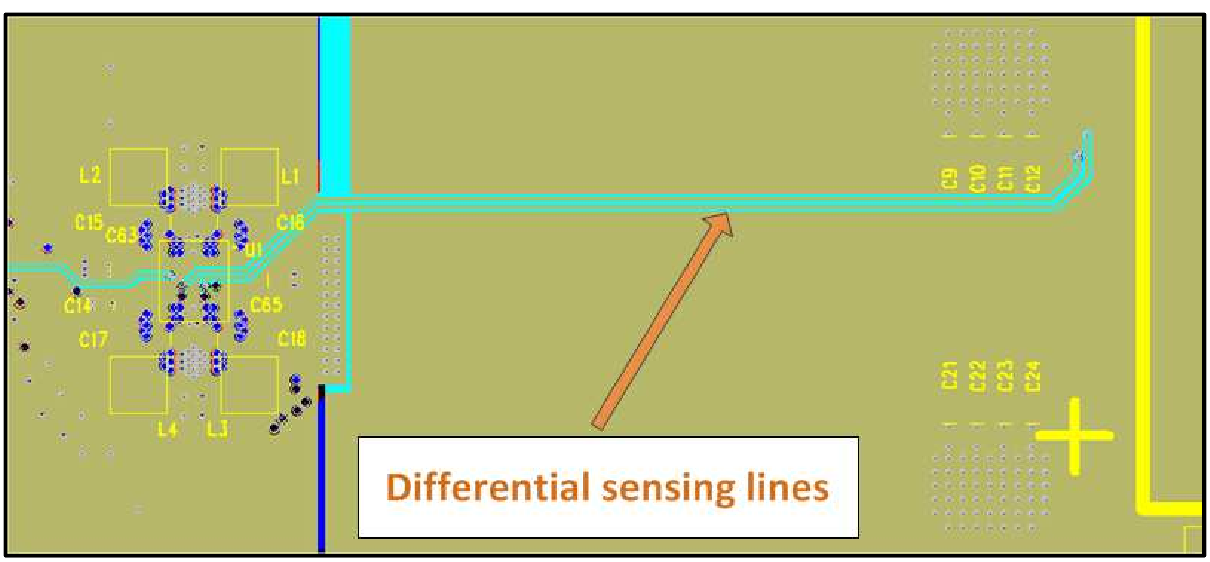

Figure 15 Feedback lines shielding

If it is not possible to avoid noise injection to feedback lines due to a layout limitation (for example, a long feedback pattern or noise from other device in a system), it is recommended to add a decoupling capacitor between the VOUT_SENSE and VSS_SENSE feedback lines close to the device. For example, capacitor 100 nF/402 can be used for filtering noise, but final selection is dependent on particular application and system.

5.3 Reference voltage source

A 2.5 V precise reference voltage source (VDDCORE) is integrated in the DA9210 device. The only external component needed for proper operation is a 220 nF 0402 capacitor placed close to the device.

Reference traces must be free of noise and any longer parallel routing with noisy lines must be avoided.

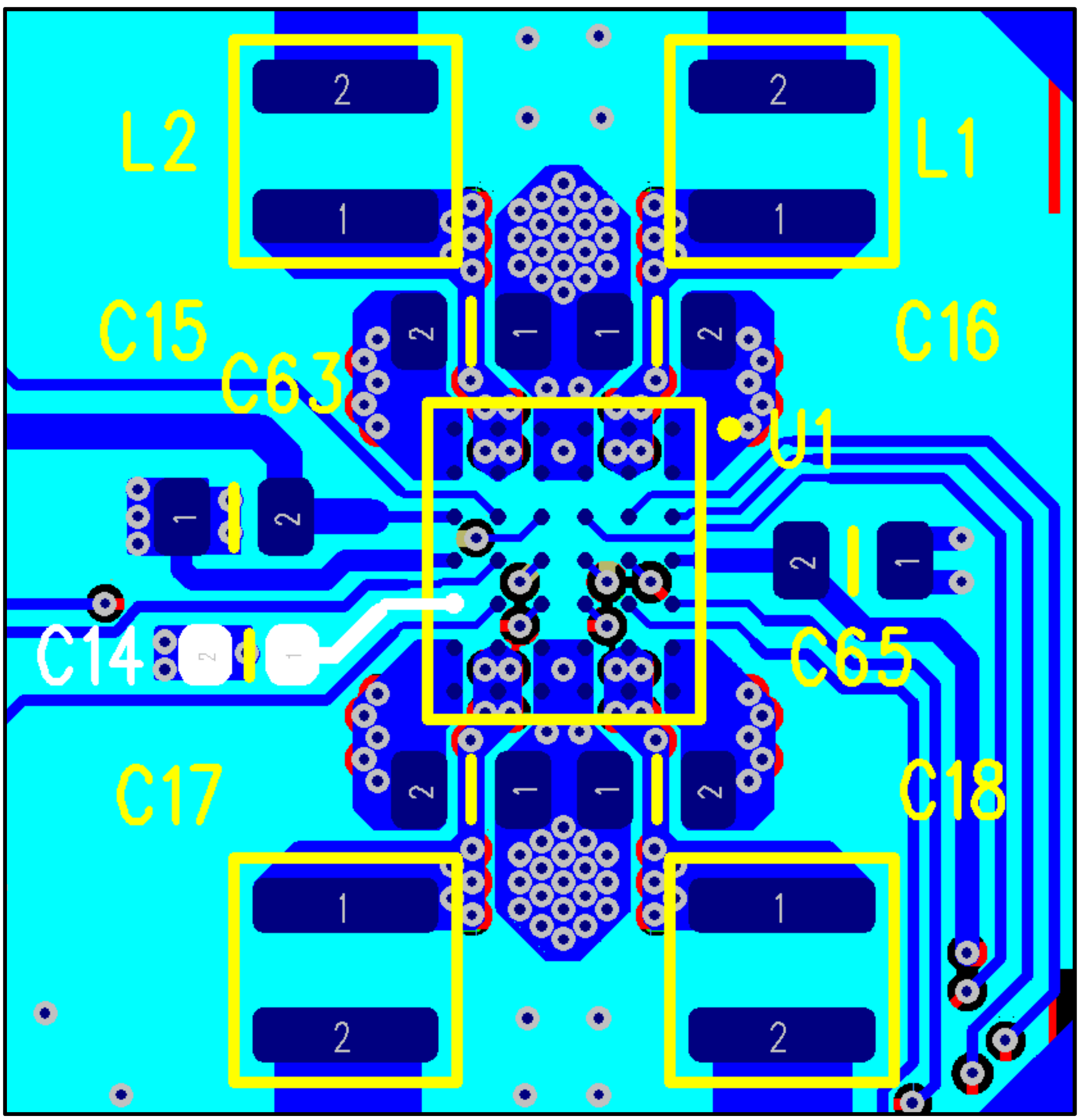

Figure 16 Reference component placement and routing

In general, designers should avoid VIAs in reference routing, since more noise can couple into the reference signal VDDCORE. When the reference capacitor is placed close to inductors (L1 to L4), we recommend that the inductors are shielded to avoid inductive coupling.

5.4 Communication interfaces

There are no firm rules regarding the interface routing strategy. All related signals are digital and immune to various kinds of noise. Care must be taken regarding the noise produced by the interface signals; avoid coupling to sensitive analogue references and feedbacks. The layer is not critical, but on a 4-layer PCB it is recommended to use layer 4 or layer 1 if possible.

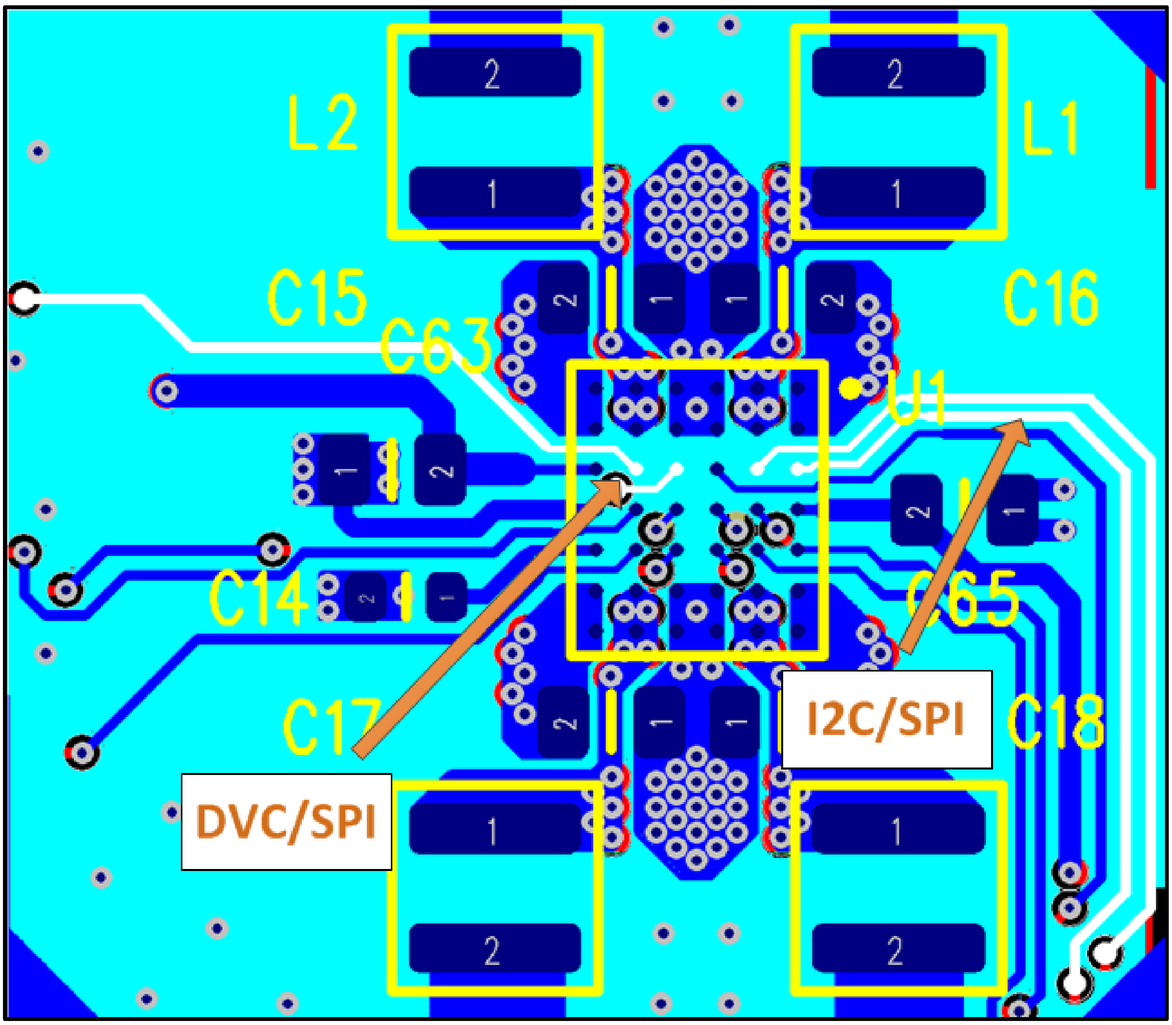

Figure 17 Interfaces lines

5.5 GPIOs and control signals

Generally, GPIOs (GPIO0 to GPIO6), TP (test pin), EN_CHIP pin and OC_PG/nIRQ pin have the lowest routing priority. Any layer can be used for routing these signals.

In most designs and applications, pin TP should be tied to ground potential. If the device will be programmed "on-board", the routing of pin TP can be performed as shown in Figure 18.

The maximum voltage that can be applied to this pin is 7.8 V.

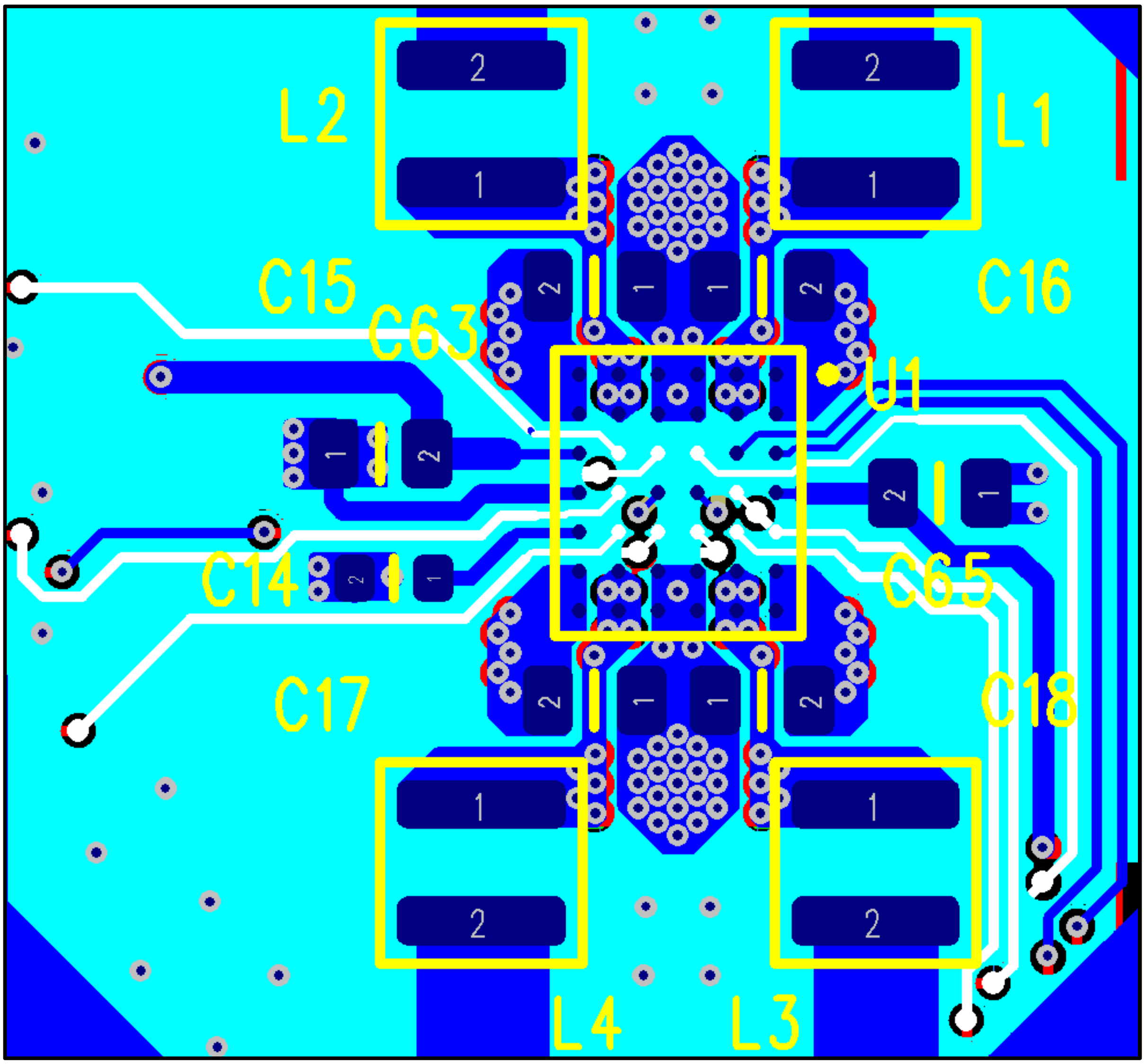

Figure 18 GPIO and control signals routing example

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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