RX671 Group, RX62N/RX621 Group

Differences Between the RX671 Group and the RX62N Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX671 Group and RX62N Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 145-pin package version of the RX671 Group and the 176-pin package version of the RX62N Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX671 Group and RX62N Group

Contents

1. Comparison of Built-In Functions of RX671 Group and RX62N Group

A comparison of the built-in functions of the RX671 Group and RX62N Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX671 Group and RX62N Group.

Table 1.1 Comparison of Built-In Functions of RX671 Group and RX62N Group

Function	RX62N	RX671
CPU	●	●
Operating mode	●/▲	●/▲
Address space	▲	▲
Resets	●	●
Option-setting memory (OFSM)	×	○
Voltage detection circuit (LVD): RX62N, (LVDA): RX671	●	●
Clock generation circuit	●	●
Clock frequency accuracy measurement circuit (CAC)	×	○
Low power consumption function	●	●
Battery backup function (VBATTB)	×	○
Register write protection function	×	○
Exception handling	●/▲	●/▲
Interrupt controller (ICUa): RX62N, (ICUE): RX671	●	●
Buses	●/▲	●/▲
Memory-protection unit (MPU)	▲	▲
DMA controller (DMACA): RX62N, (DMACAb): RX671	●	●
EXDMA controller (EXDMAC): RX62N, (EXDMACa): RX671	●	●
Data transfer controller (DTCa): RX62N, (DTCb): RX671	●	●
Event link controller (ELC)	×	○
I/O ports	●/■	●/■
Multi-function pin controller (MPC)	×	○
Multi-function timer pulse unit 2 (MTU2): RX62N Multi-function timer pulse unit 3 (MTU3a): RX671	●	●
Port output enable 2 (POE2): RX62N Port output enable 3 (POE3a): RX671	●	●
16-bit timer pulse unit (TPUa)	×	○
Programmable pulse generator (PPG)	●	●
8-bit timer (TMR): RX62N, (TMRb): RX671	●	●
Compare match timer (CMT)	●	●
Compare match timer W (CMTW)	×	○
Realtime clock (RTC): RX62N, (RTCd): RX671	●	●
Watchdog timer (WDT): RX62N, (WDTA): RX671	●/■	●/■
Independent watchdog timer (IWDT): RX62N, (IWDTa): RX671	●	●
Ethernet controller (ETHERC)	○	×
DMA controller for the ethernet controller (EDMAC)	○	×
USB 2.0 Host/Function module (USB): RX62N USB 2.0 FS Host/Function module (USBb): RX671	●	●
Serial communications interface (SCIa): RX62N, (SCIk, SCIm, SCIh): RX671	●	●
Serial communications interface (RSCI)	×	○
I²C bus interface (RIIC): RX62N, (RIICa): RX671	●	●
High-speed I²C bus interface (RIICHS)	×	○
CAN module (CAN)	●	●

Function	RX62N	RX671
Serial peripheral interface (RSPI): RX62N, (RSPId): RX671	●	
Serial peripheral interface (RSPIA)	×	○
Quad SPI memory interface (QSPIX)	×	○
CRC calculator (CRC): RX62N, (CRCA): RX671	●	
SD host interface (SDHI)	×	○
Serial sound interface (SSIE)	×	○
Remote control signal receiver (REMCa)	×	○
Capacitive touch sensing unit (CTSUa)	×	○
Boundary scan	▲	
Trusted Secure IP (TSIP)	×	○
12-bit A/D converter (S12AD): RX62N, (S12ADFa): RX671	●	
10-bit A/D converter (ADb)	○	×
D/A converter	○	×
Temperature sensor	×	○
Data operation circuit (DOCA)	×	○
RAM	●	
Standby RAM	×	○
Flash memory	●/▲	
Packages	●/▲/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX62N	RX671
CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (system clock cycle) • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 77 • Floating-point instructions: 11 • DSP instructions: 23 • Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
FPU	• Single-precision floating point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Item	RX62N	RX671
Double-precision floating point coprocessor	—	• Double-precision floating-point register set — Double-precision floating-point data registers: 64-bit × 16 — Double-precision floating-point control registers: 32-bit × 4 • Double-precision floating-point processing instructions: 21 • Function for notifying the interrupt controller of double-precision floating-point exceptions
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

Table 2.2 Comparison of CPU Registers

Register	Bit	RX62N	RX671
EXTB	—	—	Exception table register
ACC (RX62N) ACC0, ACC1 (RX671)	—	Accumulator	Accumulator 0, accumulator 1
DR0 to DR15	—	—	Double-precision floating-point data registers
DPSW	—	—	Double-precision floating-point status word
DCMR	—	—	Double-precision floating-point comparison result register
DECNT	—	—	Double-precision floating-point exception handling control register
DEPC	—	—	Double-precision floating-point exception program counter

2.2 Operating Modes

Table 2.3 is a comparative overview of the operating modes, and Table 2.4 is a comparison of operating mode registers.

Table 2.3 Comparative Overview of Operating Modes

Item	RX62N	RX671
Operating modes selected by mode-setting pins	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
	USB (user) boot mode	Boot mode (USB interface)
	—	Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode	Single-chip mode
	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode
	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode
Selection of endian	MDE pin	MDE register

Table 2.4 Comparison of Operating Mode Registers

Register	Bit	RX62N	RX671
MDMONR	MD0	MD0 status flag	—
	MD1	MD1 status flag	
	MDE	MDE status flag (b7)	MDE status flag (b0)
MDSR	—	Mode status register	
SYSCR1	—	System control register 1	System control register 1
		Initial values after a reset are different.	
	SBYRAME	—	Standby RAM enable bit

2.3 Address Space

Figure 2.1 is a comparative memory map of single-chip mode, Figure 2.2 is a comparative memory map of on-chip ROM enabled extended mode, and Figure 2.3 is a comparative memory map of on-chip ROM disabled extended mode.

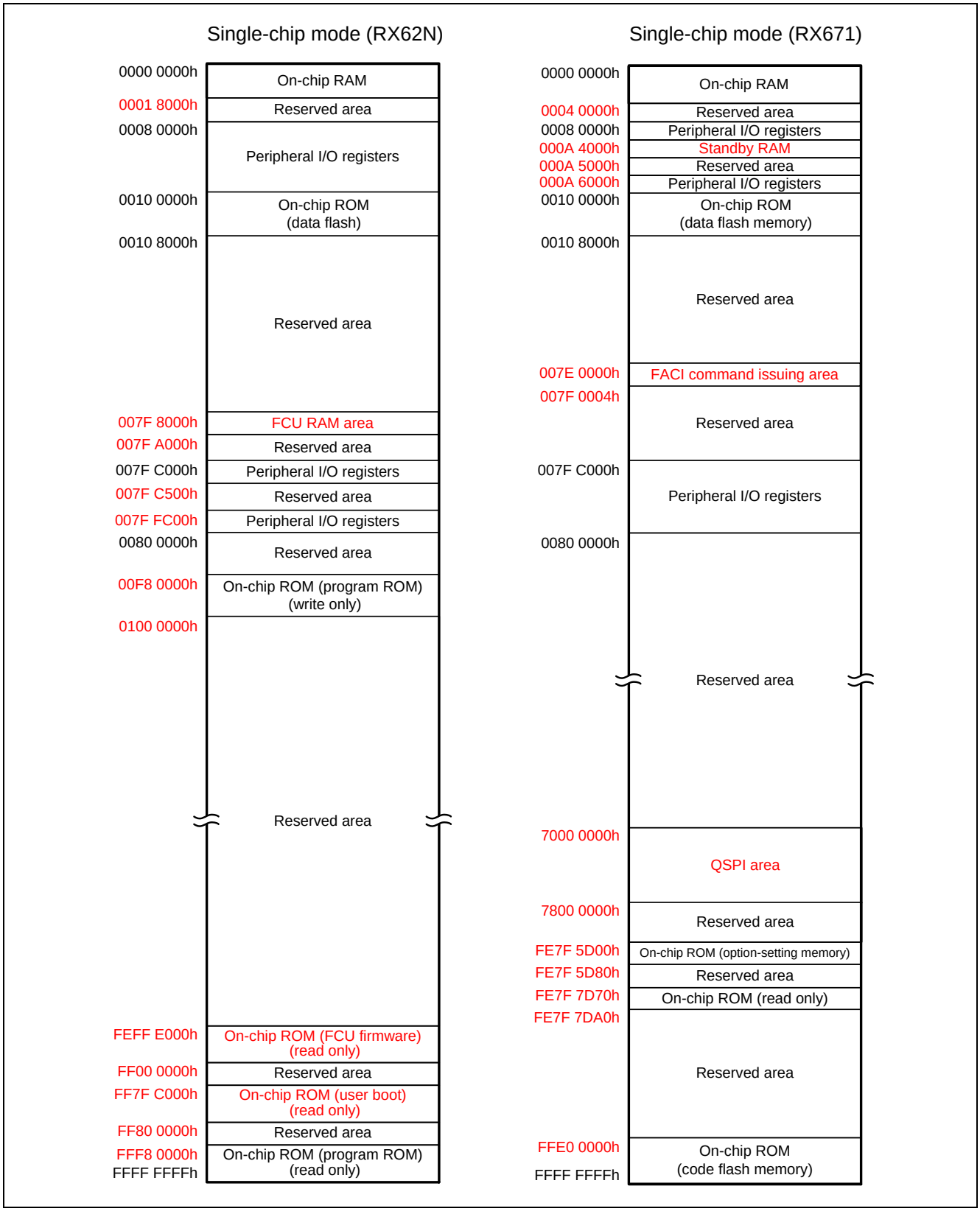

Figure 2.1 Comparative Memory Map of Single-Chip Mode

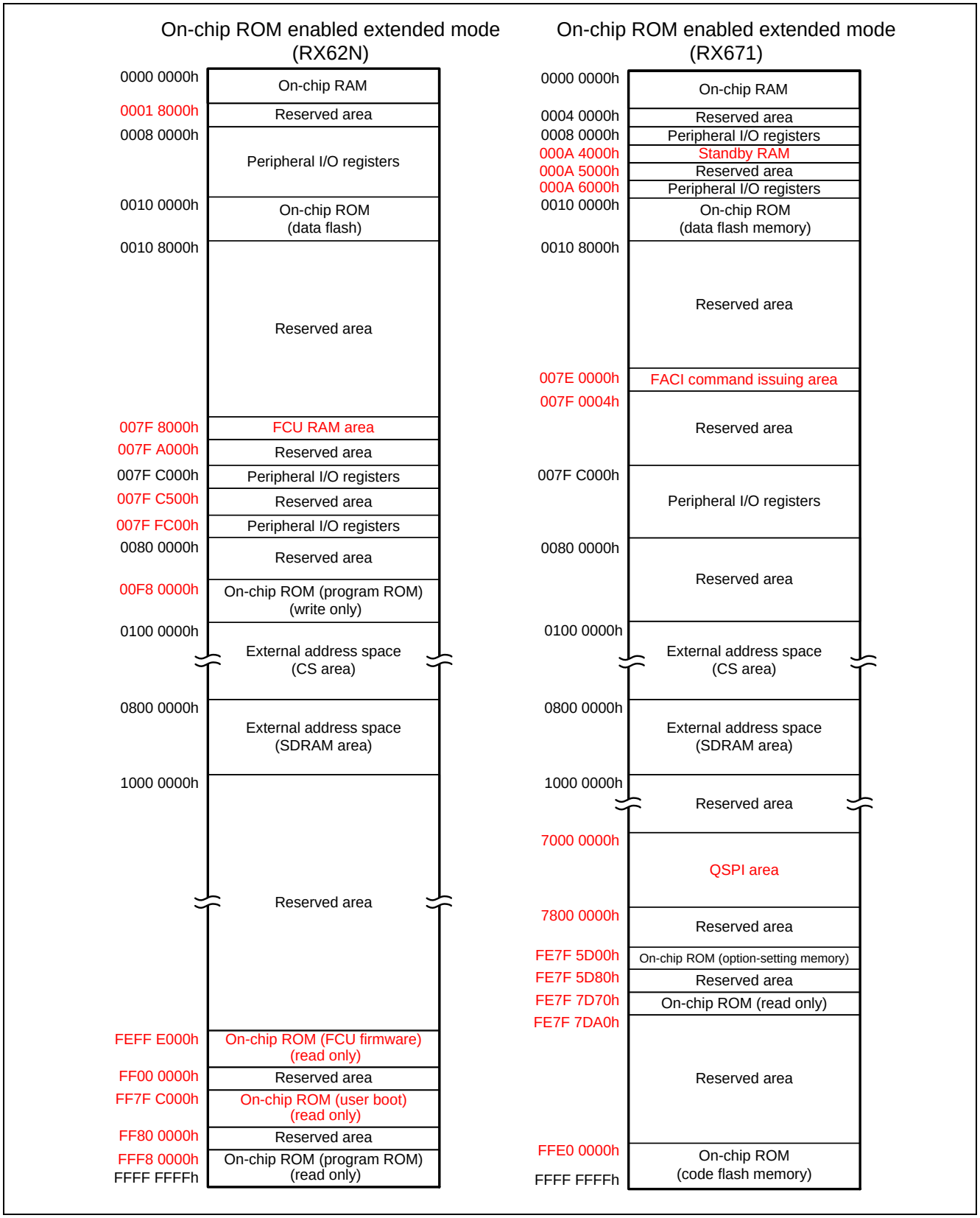

Figure 2.2 Comparative Memory Map of On-Chip ROM Enabled Extended Mode

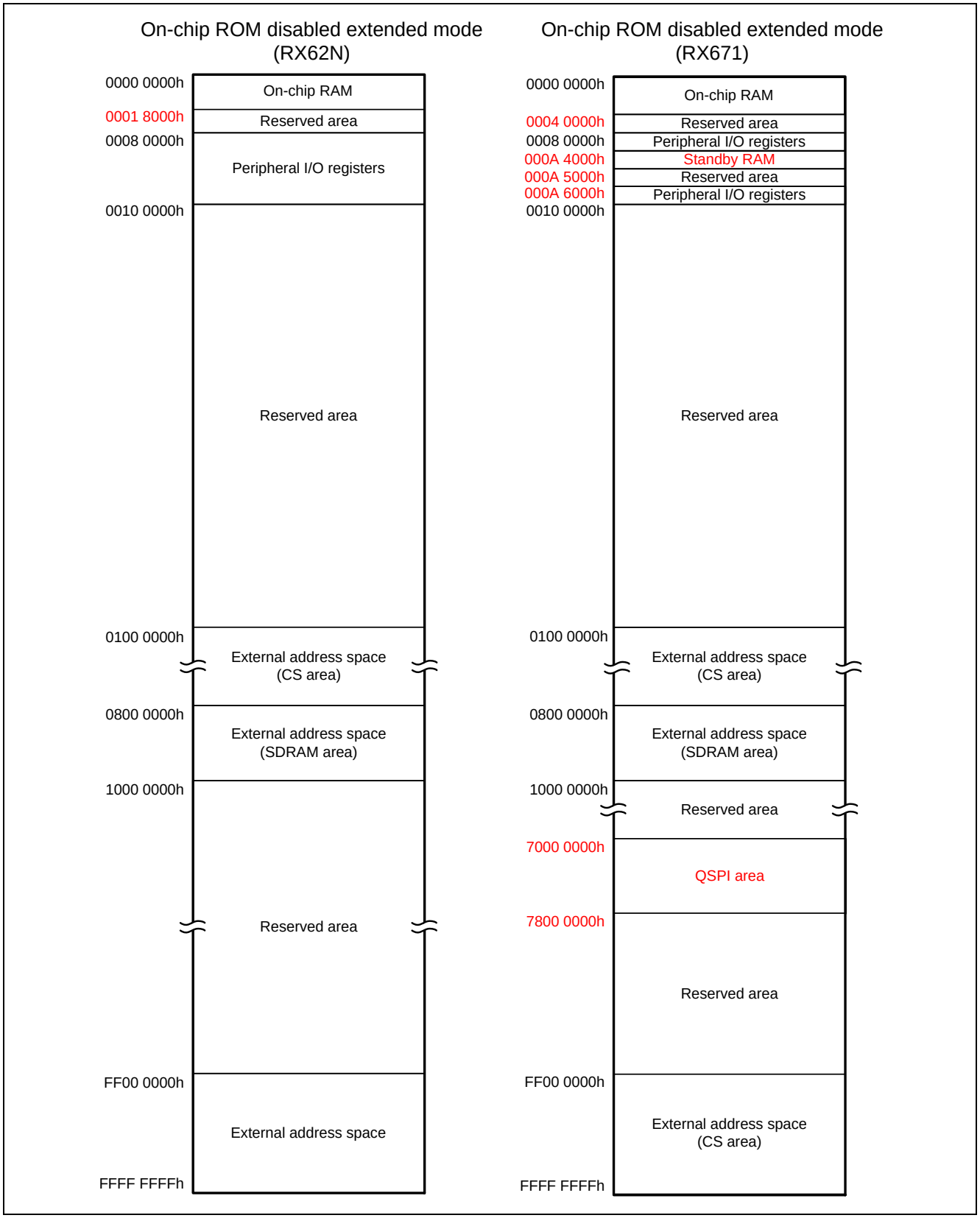

Figure 2.3 Comparative Memory Map of On-Chip ROM Disabled Extended Mode

2.4 Resets

Table 2.5 is a comparative overview of resets, and Table 2.6 is a comparison of reset-related registers.

Table 2.5 Comparative Overview of Resets

Item	RX62N	RX671
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	V_{CC} rises (voltage detection: V_{POR}).	V_{CC} rises (voltage detection: V_{POR}).
Voltage monitoring 0 reset	—	V_{CC} falls (voltage detection: Vdet0).
Voltage monitoring 1 reset	V_{CC} falls (voltage detection: Vdet1).	V_{CC} falls (voltage detection: Vdet1).
Voltage monitoring 2 reset	V_{CC} falls (voltage detection: Vdet2).	V_{CC} falls (voltage detection: Vdet2).
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	Deep software standby mode is canceled by an interrupt.
Independent watchdog timer reset	The independent watchdog timer underflows.	The independent watchdog timer underflows or a refresh error occurs.
Watchdog timer reset	The watchdog timer overflows.	The watchdog timer underflows or a refresh error occurs.
Software reset	—	Register setting

Table 2.6 Comparison of Reset-Related Registers

Register	Bit	RX62N	RX671
RSTSR (RX62N)*1 RSTSR0 (RX671)	LVD0RF	—	Voltage monitor 0 reset detect flag
	LVD1F	LVD1 detection flag (b1)	LVD1 detection flag (b2)
	LVD2F	LVD1 detection flag (b2)	LVD2 detection flag (b3)
RSTCSR*1	—	Reset control/status register	—
IWDTSR*1	—	IWDT status register	—
RSTSR1	—	—	Reset status register 1
RSTSR2	—	—	Reset status register 2
SWRR	—	—	Software reset register

Note: 1. In the User's Manual: Hardware for the RX62N Group, information on RSTSR appears in section 9, Low Power Consumption, information on RSTCSR in section 24, Watchdog Timer (WDT), and information on IWDTSR in section 25, Independent Watchdog Timer (IWDT).

2.5 Option-Setting Memory

Figure 2.4 is a comparison of option-setting memory areas, and Table 2.7 is a comparison of option-setting memory registers.

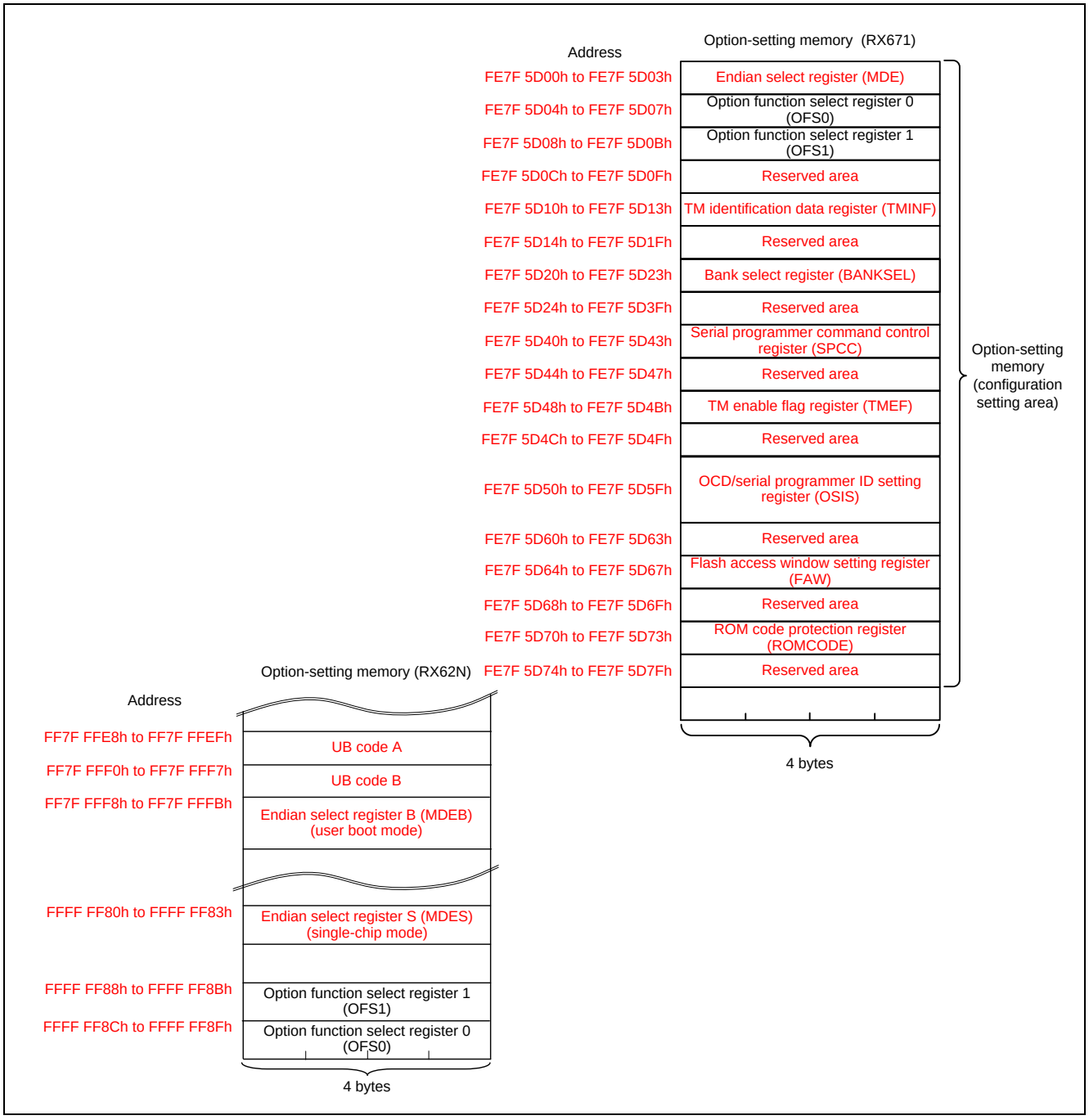

Figure 2.4 Comparison of Option-Setting Memory Areas

Table 2.7 Comparative Overview of Option-Setting Memory Registers

Register	Bit	RX62N	RX671 (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial program ID setting register
OFS0	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled. 1: Reset is enabled.	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request is enabled. 1: Reset is enabled.
	WDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled. 1: Reset is enabled.	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request is enabled. 1: Reset is enabled.
OFS1	VDSEL[1:0]	—	Voltage detection 0 level select bits
MDEB	—	Endian select register B	—
MDES	—	Endian select register S	—
MDE	—	—	Endian select register
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
BANKSEL	—	—	Bank select register
FAW	—	—	Flash access window setting register
ROMCODE	—	—	ROM code protection register

2.6 Voltage Detection Circuit

Table 2.8 is a comparative overview of the voltage detection circuits, and Table 2.9 is a comparison of voltage detection circuit registers.

Table 2.8 Comparative Overview of Voltage Detection Circuits

Item		RX62N (LVD)		RX671 (LVDA)		
		Voltage Monitoring 1	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage falls lower than Vdet1.	Voltage falls lower than Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
	Detection voltage	One level only	One level only	Selectable from three levels using OFS1.VDSEL [1:0] bits.	Selectable from three levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from three levels using LVDLVLR.LVD2LVL[3:0] bits.
	Monitor flag	—	—	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
		RSTSR.LVD1F flag: Detects rise or fall past Vdet1.	RSTSR.LVD2F flag: Detects rise or fall past Vdet2.		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet1 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet1.	Reset when Vdet2 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet2.	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC.
	Interrupt	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
		Non-maskable interrupt	Non-maskable interrupt		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
		Interrupt request generated when Vdet1 > VCC.	Interrupt request generated when Vdet2 > VCC.		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC and when VCC > Vdet2, or one or the other.
Digital filter	Enable/ disable switching	—	—	—	Available	Available
	Sampling time	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	—	—	Available: Vdet pass-through detection event output	Available: Vdet pass-through detection event output

Table 2.9 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX62N (LVD)	RX671 (LVDA)
LVDKEYR	—	Key code register for low-voltage detection control register	—
LVDCR	—	Low-voltage detection control register	—
LVD1CR1	—	—	Voltage monitor 1 circuit control register 1
LVD1SR	—	—	Voltage monitor 1 circuit status register
LVD2CR1	—	—	Voltage monitor 2 circuit control register 1
LVD2SR	—	—	Voltage monitor 2 circuit status register
LVCMPCR	—	—	Voltage monitor circuit control register
LVDLVLR	—	—	Voltage detection level select register
LVD1CR0	—	—	Voltage monitor 1 circuit control register 0
LVD2CR0	—	—	Voltage monitor 2 circuit control register 0

2.7 Clock Generation Circuit

Table 2.10 is a comparative overview of the clock generation circuits, and Table 2.11 is a comparison of clock generation circuit registers.

Table 2.10 Comparative Overview of Clock Generation Circuits

Item	RX62N	RX671
Uses	• Generates the system clock (ICLK) supplied to the CPU, DTC, DMACA, ETHERC, EDMAC, ROM, and RAM. • Generates the peripheral module clock (PCLK) to be supplied to the peripheral modules. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB-dedicated clock (UCLK) supplied to the USB. • Generates the RTC-dedicated clock (SUBCLK) supplied to the RTC. • Generates the on-chip oscillator clock (IWDTCLK) supplied to the IWDT.	• Generates the system clock (ICLK) supplied to the CPU, DMAC, DTC, QSPIX, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, RSPIA, SCIm, RSCI, MTU, and RIICHS. • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module (for analog conversion) clocks (PCLKC: unit 0, PCLKD: unit 1) to be supplied to the S12ADC. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the external bus clock (BCLK) supplied to the external bus. • Generates the SDRAM clock (SDCLK) supplied to the SDRAM. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the CAN clock (CANMCLK) supplied to the CAN. • Generates the RTC sub clock (RTCSCLK) supplied to the RTC. • Generates the RTC main clock (RTCMCLK) supplied to the RTC. • Generates the REMC sub clock (REMSCLK) supplied to the REMC. • Generates the VBATT clock (VBATCLK) supplied to the VBATT. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) supplied to the JTAG.

Item	RX62N	RX671
Operating frequencies	• ICLK: 8 MHz to 100 MHz • PCLK: 8 MHz to 50 MHz	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 60 MHz (max.) • PCLKD: 60 MHz (max.) • FCLK: — 4 MHz to 60 MHz (when programming or erasing the code flash memory or data flash memory) — 60 MHz (max.) (for reading from the data flash memory)
	• BCLK: 8 MHz to 100 MHz • BCLK pin output: 8 MHz to 50 MHz • SDCLK: 8 MHz to 50 MHz • SDCLK pin output: 8 MHz to 50 MHz • UCLK: 48 MHz (only when EXTAL = 12 MHz)	• BCLK: 120 MHz (max.) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max.)
		• CLKOUT pin output: 40 MHz (max.) • CACCLK: Same frequency as each oscillator • CANMCLK: 24 MHz (max.)
	• SUBCLK: 32.768 kHz	• RTCSCLK: 32.768 kHz • RTCMCLK: 1 kHz to 16 MHz • REMSCLK: 32.768 kHz • VBATCLK: 32.768 kHz
	• IWDTCLK: 125 kHz (typ.)	• IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max.)
	• Restrictions for setting clock frequencies: ICLK ≥ PCLK, ICLK ≥ BCLK	
Main clock oscillator	• Resonator frequency: 8 MHz to 14 MHz	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.)
	• Connectable resonator or additional circuit: Crystal resonator	• Connectable resonator or additional circuit: Ceramic resonator, crystal resonator
	• Connection pins: EXTAL, XTAL • Function that switches to internal oscillation, and function that puts the MTU pins in the high-impedance state, when oscillation stop of the main clock is detected	• Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT

Item	RX62N	RX671
PLL frequency synthesizer	• Input clock source: Main clock • Resonator frequency: 8 MHz to 14 MHz • Frequency multiplication ratio: 8 • PLL frequency synthesizer output clock: 64 MHz to 112 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable within range from 10 to 30 • PLL frequency synthesizer output clock frequency: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	—	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control • FLL function • Support for user trimming
Low-speed on-chip oscillator (LOCO)	—	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 120 kHz
External clock input (TCK) for JTAG	—	Input clock frequency: 10 MHz (max.)
Control of output on BCLK pin	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock. (When EXTAL × 1 is selected for BCLK, BCLK/2 cannot be selected.)	• BCLK clock output or high output is selectable • BCLK or BCLK/2 is selectable as the output clock
Control of output on SDCLK pin	SDCLK clock output or high output is selectable	SDCLK clock output or high output is selectable
Event link function (output)	—	Main clock oscillator oscillation stop detection
Event link function (input)	—	Switching of clock source to low-speed on-chip oscillator

Table 2.11 Comparison of Clock Generation Circuit Registers

Register	Bit	RX62N	RX671
SCKCR	—	System clock control register	System clock control register
		Initial values after a reset are different.	
SCKCR	PCKD[3:0]	—	Peripheral module clock D (PCLKD) select bits
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
	PCK[3:0] (RX62N) PCKB[3:0] (RX671)	Peripheral module clock select bits	Peripheral module clock B (PCLKB) select bits
	PCKA[3:0]	—	Peripheral module clock A (PCLKA) select bits
	BCK[3:0]	External bus clock and SDRAM clock select bits b19 b16 0 0 0 0: ×8 0 0 0 1: ×4 0 0 1 0: ×2 0 0 1 1: ×1 Settings other than the above are prohibited.	External bus clock (BCLK) select bits b19 b16 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than the above are prohibited.
	ICK[3:0]	System clock select bits b27 b24 0 0 0 0: ×8 0 0 0 1: ×4 0 0 1 0: ×2 0 0 1 1: ×1 Settings other than the above are prohibited.	System clock (ICLK) select bits b27 b24 0 0 0 0: ×1/1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than the above are prohibited.
	FCK[3:0]	—	FlashIF clock (FCLK) select bits
ROMWT	—	—	ROM wait cycle setting register
SCKCR2	—	—	System clock control register 2
SCKCR3	—	—	System clock control register 3
PLLCR	—	—	PLL control register
PLLCR2	—	—	PLL control register 2
MOSCCR	—	—	Main clock oscillator control register
LOCOCR	—	—	Low-speed on-chip oscillator control register
ILOCOCR	—	—	IWDT-dedicated on-chip oscillator control register
HOCOCR	—	—	High-speed on-chip oscillator control register
HOCOCR2	—	—	High-speed on-chip oscillator control register 2

Register	Bit	RX62N	RX671
OSCOVFSR	—	—	Oscillation stabilization flag register
OSTDCR	OSTDIE	—	Oscillation stop detection interrupt enable bit
	OSTDF	Oscillation stop detection flag	—
	KEY[7:0]	OSTDCR key code bits	—
SUBOSCCR (RX62N) SOSCCR (RX671)	SUBSTOP (RX62N) SOSTP (RX671)	Sub-clock oscillator control bit	Sub-clock oscillator stop bit
OSTDSR	—	—	Oscillation stop detection status register
MOSCWTCR	—	—	Main clock oscillator wait control register
SOSCWTCR	—	—	Sub-clock oscillator wait control register
MOFCR	—	—	Main clock oscillator forced oscillation control register
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register
CKOCR	—	—	CLKOUT output control register
SOSCCR2	—	—	Sub-clock oscillator control register 2
BKSCCR	—	—	Backup area sub-clock control register
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
HOCOTRRn	—	—	High-speed on-chip oscillator trimming register n (n = 0 to 2)

2.8 Low Power Consumption

Table 2.12 is a comparative overview of low power consumption, and Table 2.13 is a comparison of low power consumption registers.

Table 2.12 Comparative Overview of Low Power Consumption

Item	RX62N	RX671
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLK), and external bus clock (BCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	BCLK output or high-level output can be selected.	BCLK output or high-level output can be selected.
SDCLK output control function	SDCLK output or high-level output can be selected.	SDCLK output or high-level output can be selected.
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Operating power reduction function	—	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Operating power control modes: 3 — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 There is no difference in the power consumption when the same conditions (frequency and voltage) are specified in low-speed operating mode 1 and low-speed operating mode 2.

Table 2.13 Comparison of Low Power Consumption Function Registers

Register	Bit	RX62N	RX671
SBYCR	—	Standby control register	Standby control register
		Initial values after a reset are different.	
	STS[4:0]	Standby timer select bits	—
MSTPCRA	—	Module stop control register A	Module stop control register A
		Initial values after a reset are different.	
	MSTPA0	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	Compare match timer W (unit 0) module stop bit
	MSTPA8	Multifunction timer pulse unit (unit 1) module stop bit	—
	MSTPA9	Multifunction timer pulse unit (unit 0) module stop bit Target module: MTU unit 0	Multifunction timer pulse unit 3 module stop bit Target module: MTU
	MSTPA13	—	16-bit timer pulse unit 0 (unit 0) module stop bit
	MSTPA16	—	12-bit A/D converter (unit 1) module stop bit
	MSTPA19	D/A converter module stop bit	—
	MSTPA22	10-bit A/D converter (unit 1) module stop bit	—
	MSTPA23	10-bit A/D converter (unit 0) module stop bit	—
	MSTPA24	—	Module stop A24 stop bit
	MSTPA27	—	Module stop A27 stop bit
MSTPCRB	MSTPB1	—	CAN module 1 module stop bit
	MSTPB2	CAN module 2 module stop bit	—
	MSTPB4	—	Serial communication interface SCIh module stop bit
	MSTPB6	—	Data operation circuit module stop bit
	MSTPB8	—	Temperature sensor module stop bit
	MSTPB9	—	Event link controller module stop bit
	MSTPB15	Ethernet controller DMAC module stop bit	—
	MSTPB24	—	Serial communication interface 7 module-stop setting bit
	MSTPB27	—	Serial communication interface 4 module-stop setting bit
MSTPCRC	MSTPC1	RAM1 module stop bit	—
	MSTPC7	—	Standby RAM module stop bit
	MSTPC17	—	I^2C bus interface 2 module stop bit
	MSTPC19	—	CAC module stop bit
	MSTPC22	—	Serial peripheral interface 2 module-stop setting bit
	MSTPC24	—	Serial communication interface 11 module-stop setting bit

Register	Bit	RX62N	RX671
MSTPCRC	MSTPC25	—	Serial communication interface 10 module-stop setting bit
	MSTPC26	—	Serial communication interface 9 module-stop setting bit
	MSTPC27	—	Serial communication interface 8 module-stop setting bit
MSTPCRD	—	—	Module stop control register D
OPCCR	—	—	Operating power control register
RSTCKCR	—	—	Sleep mode return clock source switching register
DPSBYCR	—	Deep standby control register	Deep standby control register
		Initial values after a reset are different.	
	RAMCUT0	On-chip RAM off 0 bit	—
	RAMCUT1	On-chip RAM off 1 bit	—
	RAMCUT2	On-chip RAM off 2 bit	—
	DEEPCUT[1:0]	—	Deep cut bits
DPSWCR	—	Deep standby wait control register	—
DPSIER	—	Deep standby interrupt enable register	—
DPSIER0	—	—	Deep standby interrupt enable register 0
DPSIER1	—	—	Deep standby interrupt enable register 1
DPSIER2	—	—	Deep standby interrupt enable register 2
DPSIER3	—	—	Deep standby interrupt enable register 3
DPSIFR	—	Deep standby interrupt flag register	—
DPSIFR0	—	—	Deep standby interrupt flag register 0
DPSIFR1	—	—	Deep standby interrupt flag register 1
DPSIFR2	—	—	Deep standby interrupt flag register 2
DPSIFR3	—	—	Deep standby interrupt flag register 3
DPSIEGR	—	Deep standby interrupt edge register	—
DPSIEGR0	—	—	Deep standby interrupt edge register 0
DPSIEGR1	—	—	Deep standby interrupt edge register 1
DPSIEGR2	—	—	Deep standby interrupt edge register 2
DPSIEGR3	—	—	Deep standby interrupt edge register 3
RSTSR	—	Reset status register	—
DPSBKRy	—	Deep standby backup register (y = 0 to 31)	—

2.9 Exception Handling

Table 2.14 is a comparative overview of exception handling, Table 2.15 is a comparative listing of vector tables, and Table 2.16 is a comparative listing of return from exception handling routine instructions.

Table 2.14 Comparative Overview of Exception Handling

Item	RX62N	RX671
Exception events	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Address exception • Single-precision floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.15 Comparative Listing of Vector Tables

Item		RX62N	RX671
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception (RX62N)/ single-precision floating-point exception (RX671)		Fixed vector table	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.16 Comparative Listing of Return from Exception Handling Routine Instructions

Item		RX62N	RX671
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Address exception		—	RTE
Floating-point exception (RX62N)/ single-precision floating-point exception (RX671)		RTE	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Prohibited	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.10 Interrupt Controller

Table 2.17 is a comparative overview of the interrupt controllers, and Table 2.18 is a comparison of interrupt controller registers.

Table 2.17 Comparative Overview of Interrupt Controllers

Item		RX62N (ICUa)	RX671 (ICUE)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each connected peripheral module source.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX62N (ICUa)	RX671 (ICUE)
Interrupts	External pin interrupts	• Interrupts from pins IRQ0 to IRQ15 • Number of sources: 16 • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges	• Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Ability to set as source detection of low level, falling edge, rising edge, or rising and falling edges • A digital filter can be used to remove noise.
	Software interrupts	• An interrupt can be generated by writing to a register. • Number of sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority	Setting of priority level by writing to a register	Setting of priority level in interrupt source priority register (IPR)
	Fast interrupt function	It is possible to speed up interrupt processing by the CPU. This setting can be used for one interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC/DMAC control	Interrupt sources can be used to start the DTC and DMAC.	Interrupt sources can be used to start the DTC and DMAC.
	EXDMAC control	—	• An interrupt selected by software configurable interrupt B source select register 144 or software configurable interrupt A source select register 208 can be used to start EXDMAC0. • An interrupt selected by software configurable interrupt B source select register 145 or software configurable interrupt A source select register 209 can be used to start EXDMAC1.
Non-maskable interrupts	NMI pin interrupt	Interrupt from the NMI pin • Interrupt detection: Falling edge or rising edge	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • Digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt at detection of oscillation stop	Interrupt at detection of main clock oscillation stop
	WDT underflow/ refresh error interrupt	—	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	—	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.

Item		RX62N (ICUa)	RX671 (ICUE)
Non-maskable interrupts	Voltage monitoring interrupt	Interrupt at power voltage fall detection	• Interrupt from voltage detection circuit 1 (LVD1) • Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in the RAM.
	Double-precision floating-point exceptions	—	Exceptions from double-precision floating-point coprocessor
Return from low power consumption state	Sleep mode	Exit sleep mode by a non-maskable interrupt or any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Return is initiated by a non-maskable interrupt, interrupt from IRQ15 to IRQ0, WDT interrupt, TMR interrupt, USB interrupt (USBR), or RTC alarm interrupt.	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB0 resume, RTC alarm, RTC period, IWDT, VBATT tamper detection, REMC interrupt, or software configurable interrupt 146 to 157).
	Software standby mode	Return is initiated by a non-maskable interrupt, interrupt from IRQ15 to IRQ0, USB interrupt (USBR), or RTC alarm interrupt.	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, IWDT).
	Deep software standby mode	—	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period).

Table 2.18 Comparison of Interrupt Controller Registers

Register	Bit	RX62N (ICUa)	RX671 (ICUE)
IRn*1	—	Interrupt request register n (n = 016 to 253)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 00h to 8Fh)	Interrupt source priority register n (n = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn*1	—	DTC activation enable register n (n = 027 to 252)	DTC transfer request enable register n (n = 026 to 255)
DMRSRm	—	DMAC activation request select register m (m = 0 to 3)	DMAC trigger select register m (m = 0 to 7)
IRQFLTE0	—	—	IRQ pin digital filter enable register 0
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC0	—	—	IRQ pin digital filter setting register 0
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	LVDST	Voltage monitoring interrupt status flag	—
	OSTST	Oscillation stop detection interrupt status flag (b2)	Oscillation stop detection interrupt status flag (b1)
	WDTST	—	WDT underflow/refresh error status flag
	IWDTST	—	IWDT underflow/refresh error status flag
	LVD1ST	—	Voltage monitor 1 interrupt status flag
	LVD2ST	—	Voltage monitor 2 interrupt status flag
	EXNMIST	—	Extended non-maskable interrupt status flag
NMIER	LVDEN	Voltage monitoring interrupt enable bit	—
	OSTEN	Oscillation stop detection interrupt enable bit (b2)	Oscillation stop detection interrupt enable bit (b1)
	WDTEN	—	WDT underflow/refresh error enable bit
	IWDTEN	—	IWDT underflow/refresh error enable bit
	LVD1EN	—	Voltage monitor 1 interrupt enable bit
	LVD2EN	—	Voltage monitor 2 interrupt enable bit
	EXNMIEN	—	Extended non-maskable interrupt enable bit
NMICLR	OSTCLR	OST clear bit (b2)	OST clear bit (b1)
	WDTCLR	—	WDT clear bit
	IWDTCLR	—	IWDT clear bit
	LVD1CLR	—	LVD1 clear bit
	LVD2CLR	—	LVD2 clear bit
EXNMISR	—	—	Extended non-maskable interrupt status register
EXNMIER	—	—	Extended non-maskable interrupt enable register
EXNMICLR	—	—	Extended non-maskable interrupt status clear register

Register	Bit	RX62N (ICUa)	RX671 (ICUE)
NMIFLTE	—	—	NMI pin digital filter enable register
NMIFLTC			NMI pin digital filter setting register
GRPIE0	—	—	Group IE0 interrupt request register
GRPBE0	—	—	Group BE0 interrupt request register
GRPBL0 GRPBL1	—	—	Group BL0/BL1 interrupt request register
GRPAL0 GRPAL1	—	—	Group AL0/AL1 interrupt request register
GENIE0	—	—	Group IE0 interrupt request enable register
GENBE0	—	—	Group BE0 interrupt enable register
GENBL0 GENBL1	—	—	Group BL0/BL1 interrupt enable register
GENAL0 GENAL1	—	—	Group AL0/AL1 interrupt enable register
GCRIE0	—	—	Group IE0 interrupt clear register
GCRBE0	—	—	Group BE0 interrupt clear register
PIBRk	—	—	Software configurable interrupt B request register k (k = 0h to Ch)
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh)
SLIBXRn	—	—	Software configurable interrupt B source select register Xn (n = 128 to 143)
SLIBRn	—	—	Software configurable interrupt B source select register n (n = 144 to 207)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SELEXDR	—	—	EXDMAC activation interrupt select register
SLIPRCR	—	—	Software configurable interrupt source select register Write protection register

Note: 1. On the RX62N Group n = 254, 255 correspond to a reserved area.

2.11 Buses

Table 2.19 is a comparative overview of the buses, Table 2.20 is a comparative overview of the external buses, and Table 2.21 is a comparison of bus registers.

Table 2.19 Comparative Overview of Buses

Item		RX62N	RX671
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to on-chip RAM	Connected to RAM
	Memory bus 2	Connected to on-chip ROM	Connected to code flash memory
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMACA, DTC, and EDMAC • Connected to on-chip memory (on-chip RAM, on-chip ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DMACA, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with the BCLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLK)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USB) • Operates in synchronization with the peripheral module clock (PCLK)	• Connected to peripheral modules (USB, DOC, CTSU, REMC, and standby RAM) • Operates in synchronization with the peripheral module clock (PCLKB)

Item		RX62N	RX671
Internal peripheral buses	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC and ETHERC) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (MTU, SCIm, and RSPI) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 5	• Connected to peripheral modules • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (RSCI, RSPIA, and RIICHS) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to on-chip ROM (in P/E) and data flash. • Operates in synchronization with the peripheral module clock (PCLK)	• Connected to code flash (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)
	SDRAM area	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)
Internal expansion bus	QSPI area	—	• Connected to external SPI devices • Operates in synchronization with the system clock (ICLK)

Table 2.20 Comparative Overview of External Buses

Item	RX62N	RX671
External address space	• The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • An 8, 16, or 32-bit bus space is selectable for each area. • The endian mode can be selected independently for each area.	• The external address space is divided into eight CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management. • Chip select signals can be output for each area. • The bus width can be selected independently for each area. — Separate bus: An 8 or 16-bit bus space is selectable. — Address/data multiplexed bus: An 8 or 16-bit bus space is selectable. • The endian mode can be selected independently for each area.
CS area controller	• Recovery cycles can be inserted. — Up to 15 cycles for read recovery — Up to 15 cycles for write recovery • Cycle wait function: Waits for up to 31 cycles (up to 7 cycles for page access). • Wait control — Ability to specify timing of assertion and negation of chip-select signals (CS0# to CS7#) — Ability to specify timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1# to WR3#) — Ability to specify data output start and end timing • Write access mode: Single write strobe mode or byte strobe mode	• Recovery cycles can be inserted. — Up to 15 cycles for read recovery — Up to 15 cycles for write recovery • Cycle wait function: Waits for up to 31 cycles (up to 7 cycles for page access). • Wait control — Ability to specify timing of assertion and negation of chip-select signals (CS0# to CS7#) — Ability to specify timing of assertion of the read signal (RD#) and write signals (WR0#/WR#, and WR1#) — Ability to specify data output start and end timing • Write access mode: Single write strobe mode or byte strobe mode • Separate bus or address/data multiplexed bus can be specified for each area.
SDRAM area controller	• Multiplexed output of row address/ column address (8, 9, 10, or 11 bits) • Selectable between self-refresh and auto-refresh • CAS latency can be specified from one to three cycles.	• Multiplexed output of row address/ column address (8, 9, 10, or 11 bits) • Selectable between self-refresh and auto-refresh • CAS latency can be specified from one to three cycles.
Write buffer function	Write access by the bus master ends when the write data from the bus master has been written to the write buffer.	Write access by the bus master ends when the write data from the bus master has been written to the write buffer.
Frequencies	• The CS area controller (CSC) operates in synchronization with BCLK. • The SDRAM area controller (SDRAMC) operates in synchronization with SDCLK.	• The CS area controller (CSC) operates in synchronization with BCLK. • The SDRAM area controller (SDRAMC) operates in synchronization with SDCLK.

Table 2.21 Comparison of Bus Registers

Register	Bit	RX62N	RX671
CSnCR (n = 0 to 7)	BSIZE[1:0]	External bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: 32-bit bus space selected 1 0: 8-bit bus space selected 1 1: Setting prohibited.	External bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: Setting prohibited. 1 0: 8-bit bus space selected 1 1: Setting prohibited.
	MPXEN	—	Address/data multiplexed I/O interface select bit
CSRECEN	—	—	CS recovery cycle insertion enable register
CSnWCR1 (n = 0 to 7)	CSWWAIT[4:0]	—	Normal write cycle wait select bits
CSnWCR2 (n = 0 to 7)	AWAIT[1:0]	—	Address cycle wait select bits
SDCCR	BSIZE[1:0]	SDRAM bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: 32-bit bus space selected 1 0: 8-bit bus space selected 1 1: Setting prohibited.	SDRAM bus width select bits b5 b4 0 0: 16-bit bus space selected 0 1: Setting prohibited. 1 0: 8-bit bus space selected 1 1: Setting prohibited.
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Setting prohibited. 0 1 0: Setting prohibited. 0 1 1: DTC/DMACA 1 0 0: Setting prohibited. 1 0 1: Setting prohibited. 1 1 0: EDMAC 1 1 1: EXDMAC	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: EXDMAC
BUSPRI	BPXB[1:0]	—	Bus priority control bits

2.12 Memory Protection Unit

Table 2.22 is a comparison of memory protection unit registers.

Table 2.22 Comparison of Memory Protection Unit Registers

Register	Bit	RX62N (MPU)	RX671 (MPU)
MPESTS	IA (RX62N) IMPER (RX671)	Instruction memory protection error generated bit	Instruction memory protection error generated bit
	DA (RX62N) DMPER (RX671)	Data memory protection error generated bit	Data memory protection error generated bit

2.13 DMA Controller

Table 2.23 is a comparative overview of the DMA controllers, and Table 2.24 is a comparison of DMA controller registers.

Table 2.23 Comparative Overview of DMA Controllers

Item		RX62N (DMACA)	RX671 (DMACAb)
Number of channels		4 (DMACm (m = 0 to 3))	8 (DMACm (m = 0 to 7))
Transfer space		512 MB (00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	4 GB (00000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		1,023 K data units (maximum number of transfers in block transfer mode: 1,023 data units × 1,024 blocks)	64 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)
DMA request sources		Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins	Activation source selectable for each channel • Software trigger • Interrupt requests from peripheral modules or trigger input to external interrupt input pins
Channel priority		Channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest)	Channel 0 > channel 1 > channel 2 > channel 3 ... > channel 7 (channel 0: highest)
Transfer data	Single data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data units: 1 to 1,023 data units	Number of data units: 1 to 1,024 data units
Transfer modes	Normal transfer mode	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.
	Repeat transfer mode	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units
	Block transfer mode	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,023 data units	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination

Item		RX62N (DMACA)	RX671 (DMACAb)
Interrupt requests	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	• Generated when the specified number of transfers is completed in normal transfer mode • Generated when the specified repeat count of transfers is completed in repeat transfer mode • Generated when the specified block count of transfers is completed in block transfer mode
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Event link activation		—	Event link request generated after one data transfer (or after one block transfer in case of block transfer operation).
Low power consumption function		Module stop state can be set.	Module stop state can be set.

Table 2.24 Comparison of DMA Controller Registers

Register	Bit	RX62N (DMACA)	RX671 (DMACAb)
DMSAR	—	DMA source address register Specifies the start address of the transfer source. 00000000h to 0FFFFFFFh (256 MB) F0000000h to FFFFFFFFh (256 MB)	DMA source address register Specifies the start address of the transfer source. 00000000h to FFFFFFFFh (4 GB)
DMDAR	—	DMA destination address register Specifies the start address of the transfer destination. 00000000h to 0FFFFFFFh (256 MB) F0000000h to FFFFFFFFh (256 MB)	DMA destination address register Specifies the start address of the transfer destination. 00000000h to FFFFFFFFh (4 GB)
DMCRA	DMCRAL DMCRAH	DMA transfer count register • Block transfer mode (DMTMD.MD[1:0] = 10b) The DMCRAH register specifies the block size and the DMCRAL register functions as a 10-bit block size counter. The block size is one when the setting is 001h and 1,023 when it is 3FFh. In block transfer mode, a value in the range of 001h to 3FFh can be set in the DMCRAH and DMCRAL registers. Setting a value of 000h is prohibited.	DMA transfer count register • Block transfer mode (DMACm.DMTMD.MD[1:0] = 10b) The DMCRAH register specifies the block size and the DMCRAL register functions as a 10-bit block size counter. The block size is one when the setting is 001h, 1,023 when it is 3FFh, and 1,024 when it is 000h. In block transfer mode, a value in the range of 000h to 3FFh can be set in the DMCRAH and DMCRAL registers.
DMCRB	—	DMA block transfer count register (b9 to b0) 001h to 3FFh (1 to 1,023 operations) 000h (1,024 operations)	DMA block transfer count register (b15 to b0) 0001h to FFFFh (1 to 65,535 operations) 0000h (65,536 operations)
DMIST	—	—	DMAC74 interrupt status monitor register

2.14 EXDMA Controller

Table 2.25 is a comparative overview of the EXDMA controllers, and Table 2.26 is a comparison of EXDMA controller registers.

Table 2.25 Comparative Overview of EXDMA Controllers

Item		RX62N (EXDMAC)	RX671 (EXDMACa)
Number of channels		2 (EXDMAC0 and EXDMAC1)	2 (EXDMAC0 and EXDMAC1)
Transfer space		512 MB (external areas from 0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh, excluding reserved areas)	512 MB (external areas from 0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh, excluding reserved areas)
Maximum transfer volume		1 M data units (maximum number of transfers in block transfer mode: 1,023 data units × 1,024 blocks)	1 M data units (maximum number of transfers in block transfer mode: 1,024 data units × 1,024 blocks)
DMA request sources		Activation source selectable from the following three sources for each channel: • Software trigger • External DMA transfer request pin • DMA transfer request from peripheral module (compare match of MTU1)	Activation source selectable from the following three sources for each channel: • Software trigger • External DMA transfer request input • DMA transfer request from peripheral module (TPU1.TRGA or MTU1.TRGA) (Channel 0: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR144 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR208; Channel 1: a software configurable interrupt B request from TPU1.TRGA selected in ICU.SLIBR145 or a software configurable interrupt A request from MTU1.TRGA selected in ICU.SLIAR209)
Channel priority		Channel 0 > channel 1 (channel 0: highest)	Channel 0 > channel 1 (channel 0: highest)
Transfer data	Single data unit	Bit length: 8, 16, 32 bits	Bit length: 8, 16, 32 bits
	Block size	Number of data units: 1 to 1,023 data units	Number of data units: 1 to 1,024 data units
	Cluster size	Number of data units: 1 to 7 data units	Number of data units: 1 to 8 data units

Item		RX62N (EXDMAC)	RX671 (EXDMACa)
Transfer modes	Normal transfer mode	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.	• Transfer of one data unit per DMA transfer request • Setting in which total number of data transfers is not specified (free running mode) is available.
	Repeat transfer mode	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,023 data units	• Transfer of one data unit per DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 data units
	Block transfer mode	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,023 data units	• Transfer of one data block per DMA transfer request • Maximum settable block size: 1,024 data units
	Cluster transfer	• Transfer of one data cluster per DMA transfer request • Maximum settable cluster size: 7 data units (28 bytes)	• Transfer of one data cluster per DMA transfer request • Maximum settable cluster size: 8 data units (32 bytes)
Address modes	Single address mode	• Transfers data by accessing the transfer source or destination peripheral device with the EDACKn signal and specifying the address of the other peripheral device. • Available in normal transfer mode, repeat transfer mode, and block transfer mode.	• Transfers data by accessing the transfer source or destination peripheral device with the EDACKn (n = 0 or 1) signal and specifying the address of the other peripheral device. • Available in normal transfer mode, repeat transfer mode, and block transfer mode.
	Dual address mode	• Transfers data by specifying the addresses of the transfer source and destination. • Available in normal transfer mode, repeat transfer mode, block transfer mode, and cluster transfer mode.	• Transfers data by specifying the addresses of the transfer source and destination. • Available in normal transfer mode, repeat transfer mode, block transfer mode, and cluster transfer mode.
Selective functions	Extended repeat area function	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 MB separately settable as extended repeat area for transfer source or destination

Item		RX62N (EXDMAC)	RX671 (EXDMACa)
Interrupt requests	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.	• Generated when the specified number of transfers is completed in normal transfer mode • Generated when the specified repeat count of transfers is completed in repeat transfer mode • Generated when the specified block count of transfers is completed in block transfer mode • Generated on completion of the specified cluster count of transfers in cluster transfer mode
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Low power consumption function		Module stop state can be set.	Module stop state can be set.

Table 2.26 Comparison of EXDMA Controller Registers

Register	Bit	RX62N (EXDMAa)	RX671 (EXDMAa)
EDMCRA	EDMCRAL EDMCRAH	EXDMA transfer count register • Repeat transfer mode (EXDMACn.EDMTMD.MD[1:0] = 01b) The EDMCRAH register specifies the repeat size and the EDMCRAL register functions as a 10-bit transfer counter. The number of transfers is one when the setting is 001h and 1,023 when it is 3FFh. In repeat transfer mode, a value in the range of 001h to 3FFh can be set in the EDMCRAH and EDMCRAL registers. Setting a value of 000h is prohibited. • Block transfer mode (EXDMACn.EDMTMD.MD[1:0] = 10b) The EDMCRAH register specifies the block size and the EDMCRAL register functions as a 10-bit block size counter. The block size is one when the setting is 001h and 1,023 when it is 3FFh. In block transfer mode, a value in the range of 001h to 3FFh can be set in the EDMCRAH and EDMCRAL registers. Setting a value of 000h is prohibited.	EXDMA transfer count register • Repeat transfer mode (EXDMACn.EDMTMD.MD[1:0] bits = 01b) The EDMCRAH register specifies the repeat size and the EDMCRAL register functions as a 10-bit transfer counter. The number of transfers is one when the setting is 001h, 1,023 when it is 3FFh, and 1,024 when it is 000h. In repeat transfer mode, a value in the range of 000h to 3FFh (transfer count: 1 to 1,024) can be set in the EDMCRAH and EDMCRAL registers. • Block transfer mode (EXDMACn.EDMTMD.MD[1:0] = 10b) The EDMCRAH register specifies the block size and the EDMCRAL register functions as a 10-bit block size counter. The block size is one when the setting is 001h and 1,023 when it is 3FFh, and 1,024 when it is 000h. In block transfer mode, a value in the range of 001h to 3FFh (1 to 1,024 transfers) can be set in the EDMCRAH and EDMCRAL registers.

Register	Bit	RX62N (EXDMAa)	RX671 (EXDMAa)
EDMCRA	EDMCRAL EDMCRAH	• Cluster transfer mode (EXDMACn.EDMTMD.MD[1:0] = 11b) The EDMCRAH register specifies the cluster size and the EDMCRAL register functions as a 3-bit cluster size counter. The cluster size is one when the setting is 001h and seven when it is 007h. In cluster transfer mode, a value in the range of 001h to 007h can be set in the EDMCRAH and EDMCRAL registers. Setting a value of 000h is prohibited.	• Cluster transfer mode (EXDMACn.EDMTMD.MD[1:0] = 11b) The EDMCRAH register specifies the cluster size and EDMCRAL register functions as a 3-bit cluster size counter. The cluster size is one when the setting is 001h, seven when it is 007h, and eight when it is 000h. In cluster transfer mode, a value in the range of 000h to 007h (1 to 8 transfers) can be set in the EDMCRAH and EDMCRAL registers.
EDMTMD	DCTG[1:0]	Transfer request source select bits b1 b0 0 0: Software 0 1: Setting prohibited. 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer requests from peripheral modules (compare match of MTU1)	Transfer request source select bits b1 b0 0 0: Software 0 1: Setting prohibited. 1 0: External DMA transfer request pin (EDREQn) 1 1: DMA transfer requests from peripheral modules (TPU1.TRGA or MTU1.TRGA)
EDMOMD	DACKSEL	—	EDACKn pin toggle selection bit
CLSBRy	—	Cluster buffer register y (y = 0 to 6)	Cluster buffer register y (y = 0 to 7)

2.15 Data Transfer Controller

Table 2.27 is a comparative overview of data transfer controllers, and Table 2.28 is a comparison of data transfer controller registers.

Table 2.27 Comparative Overview of Data Transfer Controllers

Item	RX62N (DTCa)	RX671 (DTCb)
Transfer channels	Data can be transferred on a channel corresponding to the interrupt source (transferred by DTC activation request from the ICU)	The number of channels is equal to the total number of interrupt sources that can activate the DTC.
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum repeat size is 256 data units. • Block transfer mode — A single activation leads to the transfer of a single block. — The maximum block size is 255 data units.	• Normal transfer mode A single transfer request leads to a single data transfer. • Repeat transfer mode — A single transfer request leads to a single data transfer. — The transfer address is returned to the transfer start address after the number of data transfers corresponding to “repeat size”. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, 1,024 bytes. • Block transfer mode — A single transfer request leads to the transfer of a single block. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer	• Multiple data transfers can be initiated by a single activation source (chain transfer). • The chain transfer operation mode is selectable between “performed when the counter reaches 0” and “performed every time.”	• Multiple types of data transfers can be initiated by a single transfer request. • Either “performed only when the transfer counter becomes 0” or “every time” can be selected.
Sequence transfer	—	A series of complicated transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one trigger source can be set at a time. • Up to 256 sequences for a single trigger source • The data that is initially transferred in response to a transfer request determines a sequence • The whole sequence can be executed on a single request, or be suspended in the middle of the sequence and resumed on the next transfer request (division of sequence).

Item	RX62N (DTCa)	RX671 (DTCb)
Transfer space	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• In short-address mode: 16 MB (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • In full-address mode: 4 GB (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Length of a single data unit: 8, 16, or 32 bits • Number of data units in a single block: 1 to 255 data units	• Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) • Single block size: 1 to 256 data
CPU interrupt requests	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.	• An interrupt request can be generated to the CPU on a request source for a data transfer. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after data transfer of specified volume.
Event link function	—	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Transfer information read skip can be executed.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	When “fixed” is selected for transfer source address or transfer destination address, write-back skip is executed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Allows disabling the write-back of transfer information.
Displacement addition	—	The displacement value can be added to the transfer source address (for each transfer information)
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state.

Table 2.28 Comparison of Data Transfer Controller Registers

Register	Bit	RX62N (DTCa)	RX671 (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
CRA	CRAL CRAH	DTC transfer count register A Block transfer mode (MRA.MD[1:0] bits = 10b) The CRAH register specifies the block size and the CRAL register functions as an 8-bit block size counter. The number of transfers is one when the setting is 01h and 255 when it is FFh. Setting a value of 00h is prohibited. The CRAL register is decremented (−1) at each data transfer; when it reaches 00h, the value of the CRAH register is transferred to the CRAL register.	DTC transfer count register A Block transfer mode (MRA.MD[1:0] bits = 10b) The CRAH register specifies the block size and the CRAL register functions as an 8-bit block size counter. The number of transfers is one when the setting is 01h, 255 when it is FFh, and 256 when it is 00h. The CRAL register is decremented (−1) at each data transfer; when it reaches 00h, the value of the CRAH register is reloaded in the CRAL register.
DTCVBR	—	DTC vector base register (b31 to b0) The upper 4 bits (b31 to b28) are ignored, and the address of this register is extended by the value specified in b27. The value of the lower 12 bits (b11 to b0) is always 0 and writing to these bits has no effect.	DTC vector base register (b31 to b0) Writes to the upper 4 bits are ignored, and the address of the register is extended by the value specified in b27. In addition, the lower 10 bits are reserved, and their value is fixed at 0. The write value of these bits should be 0. The ranges 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h can be set in 1 KB units.
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.16 I/O Ports

Table 2.29 is a comparative overview of I/O ports of 145-pin and 144-pin products, Table 2.30 is comparative overview of I/O ports of 100-pin products, Table 2.31 is comparison of I/O port functions, and Table 2.32 is a comparison of I/O port registers.

Table 2.29 Comparative Overview of I/O Ports on 145-Pin and 144-Pin Packages

Port Symbol	RX62N (145-Pin, 144-Pin)	RX671 (145-Pin, 144-Pin)
PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P34	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P52, P54 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77*1
PORT8	P80 to P83	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	—	PF5
PORTH	—	PH1, PH2
PORTJ	—	PJ3, PJ5

Note: 1. The 145-pin TFLGA (0.65 mm pitch) product does not have pins P71 and P72.

Table 2.30 Comparative Overview of I/O Ports on 100-Pin Packages

Port Symbol	RX62N (100-Pin)	RX671 (100-Pin)
PORT0	P05, P07	P05, P07
PORT1	P12 to P14, P16	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P34	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P52, P54, P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	—	PH1, PH2
PORTJ	—	PJ3

Table 2.31 Comparison of I/O Port Functions

Item	Port Symbol	RX62N	RX671
Input pull-up function	PORT0	—	P00 to P03, P05, P07
	PORT1	—	P12 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P34, P36, P37
	PORT4	—	P40 to P47
	PORT5	—	P50 to P56
	PORT6	—	P60 to P67
	PORT7	—	P70 to P77
	PORT8	—	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	—	PF5
	PORTG	PG0 to PG7	—
	PORTH	—	PH1, PH2
	PORTJ	—	PJ3, PJ5
Open-drain output function	PORT0	P00 to P03, P05, P07	P00 to P03, P05, P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34	P30 to P34, P36, P37
	PORT4	—	P40 to P47
	PORT5	—	P50 to P56
	PORT6	—	P60 to P67
	PORT7	—	P70 to P77
	PORT8	—	P80 to P83, P86, P87
	PORT9	—	P90 to P93
	PORTA	—	PA0 to PA7
	PORTB	—	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	—	PD0 to PD7
	PORTE	—	PE0 to PE7
	PORTF	—	PF5
	PORTH	—	PH1, PH2
	PORTJ	—	PJ3, PJ5
Drive capacity switching function	PORT0	—	P00 to P03, P05, P07
	PORT1	—	P12 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P34, P36, P37
	PORT4	—	P40 to P47
	PORT5	—	P50 to P56
	PORT6	—	P60 to P67
	PORT7	—	P70 to P77
	PORT8	—	P80 to P83, P86, P87
	PORT9	—	P90 to P93
	PORTA	—	PA0 to PA7
	PORTB	—	PB0 to PB7

Item	Port Symbol	RX62N	RX671
Drive capacity switching function	PORTC	—	PC0 to PC7
	PORTD	—	PD0 to PD7
	PORTE	—	PE0 to PE7
	PORTF	—	PF5
	PORTH	—	PH1, PH2
	PORTJ	—	PJ3, PJ5
5 V tolerant	PORT0	P00, P01, P02, P07	P07
	PORT1	P12, P13, P16, P17	P12 to P17
	PORT2	P20, P21	P20, P21
	PORT3	P33	P30 to P33
	PORT6	—	P67
	PORT7	—	P73
	PORTC	—	PC0 to PC3
	PORTJ	—	PJ3

Table 2.32 Comparison of I/O Port Registers

Register	Bit	RX62N	RX671
DDR (RX62N) PDR (RX671)	B0 to B7	Pn0 to Pn7 I/O select bits (n = 0 to 9, A to G)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J)
DR (RX62N) PODR (RX671)	B0 to B7	Pn0 to Pn7 output data store bits (n = 0 to 9, A to G)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J)
PORT (RX62N) PIDR (RX671)	B0 to B7	Pn0 to Pn7 bits (n = 0 to 9, A to G)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J)
ICR	—	Input buffer control register	—
PMR	—	—	Port mode register
ODR (RX62N) ODR0, ODR1 (RX671)	B0 to B7 (RX62N) B0, B2, B3, B4, B6 (RX671)	Pn0 to Pn7 output type select bits (n = 0 to 3, C)	Pm0 to Pm3 and PE1 output type select bits (m = 0 to 9, A to E, H, J) Pm4 to Pm7 output type select bits (m = 0 to 8, A to F, J)
PCR	B0 to B7	Pn0 input pull-up resistor control bits (n = 9, A to E, G)	Pm0 input pull-up resistor control bits (m = 0 to 9, A to F, H, J)
PF0CSE	—	Port function control register 0	—
PF1CSS	—	Port function control register 1	—
PF2CSS	—	Port function control register 2	—
PF3BUS	—	Port function control register 3	—
PF4BUS	—	Port function control register 4	—
PF5BUS	—	Port function control register 5	—
PF6BUS	—	Port function control register 6	—
PF7DMA	—	Port function control register 7	—
PF8IRQ	—	Port function control register 8	—
PF9IRQ	—	Port function control register 9	—
PFAADC	—	Port function control register A	—
PFBTMR	—	Port function control register B	—
PFCMTU	—	Port function control register C	—
PFDMTU	—	Port function control register D	—
PFENET	—	Port function control register E	—
PFFSCI	—	Port function control register F	—
PFGSPI	—	Port function control register G	—
PFHSPI	—	Port function control register H	—
PFJCAN	—	Port function control register J	—
PFKUSB	—	Port function control register K	—
PFLUSB	—	Port function control register L	—
PFMPOE	—	Port function control register M	—
PFNPOE	—	Port function control register N	—
DSCR	—	—	Drive capacity control register
DSCR2	—	—	Drive capacity control register 2

2.17 Multi-Function Timer Pulse Units 2 and 3

Table 2.33 is a comparative overview of multi-function timer pulse units 2 and 3, and Table 2.34 is a comparison of multi-function timer pulse unit 2 and 3 registers.

Table 2.33 Comparative Overview of Multi-Function Timer Pulse Units 2 and 3

Item	RX62N (MTU2)	RX671 (MTU3a)
Pulse input/output	Max. 16 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	Seven or eight clocks for each channel (four clocks for channel 5 and channel 11)	11 clocks for each channel (14 for MTU0, 12 for MTU2, 10 for MTU5, and four each for MTU1 and MTU2 (when LWA = 1))
Available operations	[Channels 0 to 4, and 6 to 10] • Waveform output at compare match • Input capture function • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU8] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous clearing by compare match or input capture (excluding MTU8) • Simultaneous register input/output by synchronous counter operation (excluding MTU8) • Up to 12-phase PWM output in combination with synchronous operation (excluding MTU8)
	[Channels 0, 3, 4, 6, 9, and 10] Ability to specify buffer operation	[MMTU0, MTU3, MTU4, MTU6, MTU7, MTU8] Ability to specify buffer operation
	[Channels 1, 2, 7, and 8] • Independent specification of phase counting mode • Cascade connection operation	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation
	[Channels 3, 4, 9, and 10] Ability to produce six-phase waveform output, including three phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode

Item	RX62N (MTU2)	RX671 (MTU3a)
Available operations	[Channels 0, 3, 4, 6, 9, and 10] Ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output	[MTU3, MTU4] Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
	[Channels 5 and 11] Dead time compensation counter	[MTU5] Can be used as a dead time compensation counter.
	—	[MTU0/MTU5, MTU1, MTU2, MTU8] Ability to use the MTU1 and MTU2 in combination and specify 32-bit phase counting mode linked to the MTU0 or MTU5 and MTU8
Interrupt skipping function	• Interrupts at counter peak or trough • A/D converter conversion start trigger skipping function	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode
Interrupt sources	28 sources	43 sources
Buffer operation	Automatic transfer of register data	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate programmable pulse generator (PPG) output triggers • Ability to generate A/D converter start trigger	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D conversion start request delay function, and ability to synchronize operation with PWM output
Low power consumption function	Each unit can be placed in a module stop state.	Ability to transition to module stop state

Table 2.34 Comparison of Multi-Function Timer Pulse Unit 2 and 3 Registers

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU7.TCR MTU8.TCR	CCLR[2:0]	Counter clear source select bits b7 b5 0 0 0: TCNT clearing disabled 0 0 1: TCNT cleared by TGRA compare match/input capture 0 1 0: TCNT cleared by TGRB compare match/input capture 0 1 1: TCNT cleared by counter clearing in another channel performing synchronous clearing/synchronous operation	Counter clear source select bits b7 b5 0 0 0: TCNT clearing disabled 0 0 1: TCNT cleared by TGRA compare match/input capture 0 1 0: TCNT cleared by TGRB compare match/input capture 0 1 1: TCNT cleared by counter clearing in another channel performing synchronous clearing/synchronous operation 1 0 0: TCNT clearing disabled 1 0 1: TCNT cleared by TGRC compare match/input capture 1 1 0: TCNT cleared by TGRD compare match/input capture 1 1 1: TCNT cleared by counter clearing in another channel performing synchronous clearing/synchronous operation
MTU6.TCR	TPSC[2:0]	Time prescaler select bits b2 b0 0 0 0: Internal clock: counts on PCLK/1 0 0 1: Internal clock: counts on PCLK/4 0 1 0: Internal clock: counts on PCLK/16 0 1 1: Internal clock: counts on PCLK/64 1 0 0: External clock: counts on MTCLKn pin input (n = A or E) 1 0 1: External clock: counts on MTCLKn pin input (n = B or F) 1 1 0: External clock: counts on MTCLKn pin input (n = C or G) 1 1 1: External clock: counts on MTCLKn pin input (n = D or H)	Counter clear source select bits b2 b0 0 0 0: Internal clock: counts on PCLKA/1 0 0 1: Internal clock: counts on PCLKA/4 0 1 0: Internal clock: counts on PCLKA/16 0 1 1: Internal clock: counts on PCLKA/64 1 0 0: Internal clock: counts on PCLKA/256 1 0 1: Internal clock: counts on PCLKA/1024 1 1 0: External clock: counts on MTCLKA pin input 1 1 1: External clock: counts on MTCLKB pin input

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU7.TCR	TPSC[2:0]	Time prescaler select bits b2 b0 0 0 0: Internal clock: counts on PCLK/1 0 0 1: Internal clock: counts on PCLK/4 0 1 0: Internal clock: counts on PCLK/16 0 1 1: Internal clock: counts on PCLK/64 1 0 0: External clock: counts on MTCLKn pin input (n = A or E) 1 0 1: External clock: counts on MTCLKn pin input (n = B or F) 1 1 0: Internal clock: counts on PCLK/256 1 1 1: Counts on TCNTn overflow/underflow (n = 8)	Counter clear source select bits b2 b0 0 0 0: Internal clock: counts on PCLKA/1 0 0 1: Internal clock: counts on PCLKA/4 0 1 0: Internal clock: counts on PCLKA/16 0 1 1: Internal clock: counts on PCLKA/64 1 0 0: Internal clock: counts on PCLKA/256 1 0 1: Internal clock: counts on PCLKA/1024 1 1 0: External clock: counts on MTCLKA pin input 1 1 1: External clock: counts on MTCLKB pin input
MTU8.TCR	TPSC[2:0]	Time prescaler select bits b2 b0 0 0 0: Internal clock: counts on PCLK/1 0 0 1: Internal clock: counts on PCLK/4 0 1 0: Internal clock: counts on PCLK/16 0 1 1: Internal clock: counts on PCLK/64 1 0 0: External clock: counts on MTCLKn pin input (n = A or E) 1 0 1: External clock: counts on MTCLKn pin input (n = B or F) 1 1 0: Internal clock: counts on PCLK/256 1 1 1: Counts on TCNTn overflow/underflow (n = 8)	Counter clear source select bits b2 b0 0 0 0: Internal clock: counts on PCLKA/1 0 0 1: Internal clock: counts on PCLKA/4 0 1 0: Internal clock: counts on PCLKA/16 0 1 1: Internal clock: counts on PCLKA/64 1 0 0: Internal clock: counts on PCLKA/256 1 0 1: Internal clock: counts on PCLKA/1024 1 1 0: External clock: counts on MTCLKA pin input 1 1 1: External clock: counts on MTCLKB pin input
TCR2	—	—	Timer control register 2

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
TMDR (RX62N) TMDR1 (RX671)	MD[3:0]	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited. 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Setting prohibited. 1 0 1 x: Setting prohibited. 1 1 0 0: Setting prohibited. 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough)	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited. 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Phase counting mode 5 1 0 1 x: Setting prohibited. 1 1 0 0: Setting prohibited. 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough)
TMDR2A TMDR2B	—	—	Timer mode register 2
TMDR3	—	—	Timer mode register 3

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU0.TIORH	IOA[3:0]	I/O control A bits b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 x x: Capture input source is MTU1/count clock. Input capture at MTU1.TCNT up-count/down-count.	I/O control A bits b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 0 0: Capture input source is MTU1/count clock MTU1.TCNT (LWA = 0) or input capture at MTU1.TCNTLW (LWA = 1) up-count/down-count. 1 1 1 x: Input capture at occurrence of MTU8.TGRC compare match.

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU6.TIORH	IOA[3:0] IOB[3:0]	I/O control A bits (b3 to b0) I/O control B bits (b7 to b4) b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 x x: Capture input source is MTU7/count clock. Input capture at MTU7.TCNT up-count/down-count.	I/O control A bits (b3 to b0) I/O control B bits (b7 to b4) b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 x 0 0: Input capture at rising edge. 1 x 0 1: Input capture at falling edge. 1 x 1 x: Input capture at both edges.

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU7.TIORH	IOA[3:0] IOB[3:0]	I/O control A bits (b3 to b0) I/O control B bits (b7 to b4) b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 x x: Input capture at occurrence of MTU6.TGRC compare match/input capture	I/O control A bits (b3 to b0) I/O control B bits (b7 to b4) b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 x 0 0: Input capture at rising edge. 1 x 0 1: Input capture at falling edge. 1 x 1 x: Input capture at both edges.

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU1.TIOR	IOB[3:0]	I/O control B bits b7 b4 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 x x: Input capture at occurrence of MTU0.TGRC compare match/input capture	I/O control B bits b7 b4 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 0 0: Input capture at occurrence of MTU0.TGRC compare match/input capture 1 1 1 x: Input capture at occurrence of MTU8.TGRC compare match.

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU8.TIORH	IOB[3:0]	I/O control B bits b7 b4 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 x 0 0: Input capture at rising edge. 1 x 0 1: Input capture at falling edge. 1 x 1 x: Input capture at both edges.	I/O control B bits b7 b4 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 x x: Capture input source is MTU1/count clock MTU1.TCNT (LWA = 0) or input capture at MTU1.TCNTLW (LWA = 1) up-count/down-count.

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU6.TIORL	IOC[3:0] IOD[3:0]	I/O control C bits (b3 to b0) I/O control D bits (b7 to b4) b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 0 0 0: Input capture at rising edge. 1 0 0 1: Input capture at falling edge. 1 0 1 x: Input capture at both edges. 1 1 x x: Capture input source is MTU7/count clock. Input capture at MTU7.TCNT up-count/down-count.	I/O control C bits (b3 to b0) I/O control D bits (b7 to b4) b3 b0 0 0 0 0: Output prohibited. 0 0 0 1: Initial output is low, low output at compare match. 0 0 1 0: Initial output is low, high output at compare match. 0 0 1 1: Initial output is low, toggle output at compare match. 0 1 0 0: Output prohibited. 0 1 0 1: Initial output is high, low output at compare match. 0 1 1 0: Initial output is high, high output at compare match. 0 1 1 1: Initial output is high, toggle output at compare match. 1 x 0 0: Input capture at rising edge. 1 x 0 1: Input capture at falling edge. 1 x 1 x: Input capture at both edges.

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
TIORU TIORV TIORW	IOC[4:0]	I/O control C bits b4 b0 0 0 0 0 0: Compare match 0 0 0 0 1: Setting prohibited. 0 0 0 1 x: Setting prohibited. 0 0 1 x x: Setting prohibited. 0 1 x x x: Setting prohibited. 1 0 0 0 0: Setting prohibited. 1 0 0 0 1: Input capture at rising edge. 1 0 0 1 0: Input capture at falling edge. 1 0 0 1 1: Input capture at both edges. 1 0 1 x x: Setting prohibited. 1 1 0 0 0: Setting prohibited. 1 1 0 0 1: Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 0 1 0: Measurement of low pulse width of external input signal. Capture at crest in complementary PWM mode. 1 1 0 1 1: Measurement of low pulse width of external input signal. Capture at crest and trough in complementary PWM mode. 1 1 1 0 0: Setting prohibited. 1 1 1 0 1: Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 1 1 0: Measurement of high pulse width of external input signal. Capture at crest in complementary PWM mode. 1 1 1 1 1: Measurement of high pulse width of external input signal. Capture at crest and trough in complementary PWM mode.	I/O control C bits b4 b0 0 0 0 0 0: No function 0 0 0 0 1: Setting prohibited. 0 0 0 1 x: Setting prohibited. 0 0 1 x x: Setting prohibited. 0 1 x x x: Setting prohibited. 1 0 0 0 0: Setting prohibited. 1 0 0 0 1: Input capture at rising edge. 1 0 0 1 0: Input capture at falling edge. 1 0 0 1 1: Input capture at both edges. 1 0 1 x x: Input capture at occurrence of MTU8.TGRC compare match. 1 1 0 0 0: Setting prohibited. 1 1 0 0 1: Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 0 1 0: Measurement of low pulse width of external input signal. Capture at crest in complementary PWM mode. 1 1 0 1 1: Measurement of low pulse width of external input signal. Capture at crest and trough in complementary PWM mode. 1 1 1 0 0: Setting prohibited. 1 1 1 0 1: Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode. 1 1 1 1 0: Measurement of high pulse width of external input signal. Capture at crest in complementary PWM mode. 1 1 1 1 1: Measurement of high pulse width of external input signal. Capture at crest and trough in complementary PWM mode.

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
MTU0.TIER2	TTGE2	—	A/D conversion start request enable 2 bit
MTU8.TCNT	—	Timer counter TCNT is a 16-bit register.	Timer counter TCNT is a 32-bit register.
MTU8.TGR	—	Timer general register TGR is a 16-bit register.	Timer general register TGR is a 32-bit register.
MTUA.TSTR (RX62N) TSTRA (RX671)	CST8	—	Counter start 8 bit
MTUB.TSTR (RX62N) TSTRB (RX671)	CST0 (RX62N) CST6 (RX671)	Counter start 0 bit (b0)	Counter start 6 bit (b6)
	CST1 (RX62N) CST7 (RX671)	Counter start 1 bit (b1)	Counter start 7 bit (b7)
	CST2	Counter start 2 bit	—
	CST3	Counter start 3 bit	—
	CST4	Counter start 4 bit	—
MTUA.TSYR (RX62N) TSYRA (RX671)	—	Timer synchronous register	Timer synchronous register
MTUB.TSYR (RX62N) TSYRB (RX671)	SYNC0 (RX62N) SYNC6 (RX671)	Timer synchronous operation 0 bit (b0)	Timer synchronous operation 6 bit (b6)
	SYNC1 (RX62N) SYNC7 (RX671)	Timer synchronous operation 1 bit (b1)	Timer synchronous operation 7 bit (b7)
	SYNC2	Timer synchronous operation 2 bit	—
	SYNC3	Timer synchronous operation 3 bit	—
	SYNC4	Timer synchronous operation 4 bit	—
TRWER (RX62N) TRWERA,TRWERB (RX671)	RWE	Timer read/write enable register The TRWER register enables or disables access to the registers and counters that have write-protection against accidental modification on channels 3, 4, 9, and 10.	Timer read/write enable register The TRWERA register enables or disables access to the registers and counters that have write-protection against accidental modification on the MTU3 and MTU4. The TRWERB register enables or disables access to the registers and counters that have write-protection against accidental modification on the MTU6 and MTU7.

Register	Bit	RX62N (MTU2)	RX671 (MTU3a)
TOER	—	Timer output master enable register	—
TOERA, TOERB	—	—	Timer output master enable register
TOCR1	—	Timer output control register 1	—
TOCR1A, TOCR1B	—	—	Timer output control register 1
TOCR2	—	Timer output control register 2	—
TOCR2A, TOCR2B	—	—	Timer output control register 2
TOLBR	—	Timer output level buffer register	—
TOLBRA, TOLBRB	—	—	Timer output level buffer register
TGCR (RX62N) TGCRA (RX671)	—	Timer gate control register	Timer gate control register A
TCNTS	—	Timer subcounter	—
TCNTSA, TCNTSB	—	—	Timer subcounter
TDDR	—	Timer dead time data register	—
TDDRA, TDDRB	—	—	Timer dead time data register
TCDR	—	Timer cycle data register	—
TCDRA, TCDRB	—	—	Timer cycle data register
TCBR	—	Timer cycle buffer register	—
TCBRA, TCBRB	—	—	Timer cycle buffer register
TITCR (RX62N) TITCR1A (RX671)	—	Timer interrupt skipping set register	Timer interrupt skipping set register 1
TITCR1B	—	—	Timer interrupt skipping set register 1
TITCR2A, TITCR2B	—	—	Timer interrupt skipping set register 2
TITCNT (RX62N) TITCNT1A (RX671)	—	Timer interrupt skipping counter	Timer interrupt skipping counter 1
TITCNT1B	—	—	Timer interrupt skipping counter 1
TITCNT2A, TITCNT2B	—	—	Timer interrupt skipping counter 2
TBTER	—	Timer buffer transfer set register	—
TBTERA, TBTERB	—	—	Timer buffer transfer set register
TDER	—	Timer dead time enable register	—
TDERA, TDERB	—	—	Timer dead time enable register
TWCR	—	Timer waveform control register	—
TWCRA, TWCRB	—	—	Timer waveform control register
TSYCR	—	—	Timer synchronous clear register
TCNTLW	—	—	Timer longword counter
TGRALW TGRBLW	—	—	Timer longword general register
TCSYSTR	—	—	Timer counter synchronous start register
NFCRn	—	—	Noise filter control register n (n = 0 to 4, 6, 7, 8, C)
NFCR5	—	—	Noise filter control register 5
TITMRA TITMRB	—	—	Timer interrupt skipping mode register

2.18 Port Output Enable 2 and 3

Table 2.35 is a comparative overview of port output enable 2 and 3, and Table 2.36 is a comparison of port output enable 2 and 3 registers.

Table 2.35 Comparative Overview of Port Output Enable 2 and 3

Item	RX62N (POE2)	RX671 (POE3a)
Pin status while output is disabled	High-impedance	High-impedance
High-impedance control target pins	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D) — MTU9 pin (MTIOC9B, MTIOC9D) — MTU10 pin (MTIOC10A, MTIOC10B, MTIOC10C, MTIOC10D)	• MTU output pins — MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pin (MTIOC3B, MTIOC3D) — MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pin (MTIOC6B, MTIOC6D) — MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D)
Conditions for generating high-impedance request	• Input pin changes When signal input occurs on pin POE0# to POE9#. • Short circuit of output pins: A match (short circuit) of signal levels lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B-A and MTIOC3D-A — MTIOC3B-B and MTIOC3D-B — MTIOC4A-A and MTIOC4C-A — MTIOC4A-B and MTIOC4C-B — MTIOC4B-A and MTIOC4D-A — MTIOC4B-B and MTIOC4D-B — MTIOC9B and MTIOC9D — MTIOC10A and MTIOC10C — MTIOC10B and MTIOC10D • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator	• Input pin changes When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, or POE11# • Short circuit of output pins: A match (short circuit) of signal levels lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D • Making of SPOER register setting • Detection of stopped oscillation on main clock oscillator

Item	RX62N (POE2)	RX671 (POE3a)
Functions	• Falling edge detection or PCLK/8 × 16, PCLK/16 × 16, or PCLK/128 × 16 low-level sampling can be specified for input pins POE0# to POE9#.	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0#, POE4#, POE8#, POE10#, and POE11# input pins.
	• MTU complementary PWM output pins and MTU0 or MTU6 can be placed in the high-impedance state by falling edge detection or low-level sampling on pins POE0# to POE9#.	• Output on all control target pins can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE0#, POE4#, POE8#, POE10#, and POE11# pins.
	• MTU complementary PWM output pins and MTU0 or MTU6 can be placed in the high-impedance state when oscillation stop of the clock generation circuit is detected.	• Output on all control target pins can be placed in the high-impedance state when oscillation by the clock generation circuit stops.
	• MTU pins can be placed in the high-impedance state when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more.	• It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, output on the pins can be placed in the high-impedance state.
	• MTU complementary PWM output pins and MTU0 or MTU6 can be placed in the high-impedance state by modifying the POE register settings.	• Output on all control target pins can be placed in the high-impedance state by modifying settings of POE registers.
	• Interrupts can be generated by input-level sampling or output-level comparison results.	• Interrupts can be generated in response to the results of input level sampling or output-level comparison.

Table 2.36 Comparison of Port Output Enable 2 and 3 Registers

Register	Bit	RX62N (POE2)	RX671 (POE3a)
ICSR1	POE1M[1:0]	POE1 mode select bits	—
	POE2M[1:0]	POE2 mode select bits	—
	POE3M[1:0]	POE3 mode select bits	—
	POE1F	POE1 flag	—
	POE2F	POE2 flag	—
	POE3F	POE3 flag	—
ICSR2	POE5M[1:0]	POE5 mode select bits	—
	POE6M[1:0]	POE6 mode select bits	—
	POE7M[1:0]	POE7 mode select bits	—
	POE5F	POE5 flag	—
	POE6F	POE6 flag	—
	POE7F	POE7 flag	—
ICSR4	POE9M[1:0] (RX62N) POE10M[1:0] (RX671)	POE9 mode select bits	POE10 mode select bits
	POE9E (RX62N) POE10E (RX671)	POE9 high-impedance enable bit	POE10 high-impedance enable bit
	POE9F (RX62N) POE10F (RX671)	POE9 flag	POE10 flag
ICSR5	—	—	Input level control/status register 5
ICSR6	—	—	Input level control/status register 6
SPOER	CH34HIZ (RX62N) MTUCH34HIZ (RX671)	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 pin high-impedance enable bit
	CH0HIZ (RX62N) MTUCH0HIZ (RX671)	MTU0 output high-impedance enable bit (b1)	MTU0 pin high-impedance enable bit (b2)
	CH910HIZ	MTU9 and MTU10 output high-impedance enable bit	—
	CH6HIZ (RX62N) MTUCH67HIZ (RX671)	MTU6 output high-impedance enable bit (b3)	MTU6 and MTU7 pin high-impedance enable bit (b1)
POECR1	PE0ZE (RX62N) MTU0AZE (RX671)	MTIOC0A high-impedance enable bit	MTIOC0A pin high-impedance enable bit
	PE1ZE (RX62N) MTU0BZE (RX671)	MTIOC0B high-impedance enable bit	MTIOC0B pin high-impedance enable bit
	PE2ZE (RX62N) MTU0CZE (RX671)	MTIOC0C high-impedance enable bit	MTIOC0C pin high-impedance enable bit
	PE3ZE (RX62N) MTU0DZE (RX671)	MTIOC0D high-impedance enable bit	MTIOC0D pin high-impedance enable bit
	PE4ZE	MTIOC6A high-impedance enable bit	—
	PE5ZE	MTIOC6B high-impedance enable bit	—
	PE6ZE	MTIOC6C high-impedance enable bit	—
	PE7ZE	MTIOC6D high-impedance enable bit	—

Register	Bit	RX62N (POE2)	RX671 (POE3a)
POECR2	P6CZE	MTU port 6 high-impedance enable bit	—
	P5CZE	MTU port 5 high-impedance enable bit	—
	P4CZE	MTU port 4 high-impedance enable bit	—
	P3CZEB	MTU port 3 high-impedance enable B bit	—
	P2CZEB	MTU port 2 high-impedance enable B bit	—
	P1CZEB	MTU port 1 high-impedance enable B bit	—
	P3CZEA	MTU port 3 high-impedance enable A bit	—
	P2CZEA	MTU port 2 high-impedance enable A bit	—
	P1CZEA	MTU port 1 high-impedance enable A bit	—
	MTU7BDZE	—	MTIOC7B/MTIOC7D pin high-impedance enable bit
	MTU7ACZE	—	MTIOC7A/MTIOC7C pin high-impedance enable bit
	MTU6BDZE	—	MTIOC6B/MTIOC6D pin high-impedance enable bit
	MTU4BDZE	—	MTIOC4B/MTIOC4D pin high-impedance enable bit
	MTU4ACZE	—	MTIOC4A/MTIOC4C pin high-impedance enable bit
	MTU3BDZE	—	MTIOC3B/MTIOC3D pin high-impedance enable bit
ALR1	—	—	Active level register 1
POECR4	—	—	Port output enable control register 4
POECR5	—	—	Port output enable control register 5
M0SELR1	—	—	MTU0 pin select register 1
M0SELR2	—	—	MTU0 pin select register 2
M3SELR	—	—	MTU3 pin select register
M4SELR1	—	—	MTU4 pin select register 1
M4SELR2	—	—	MTU4 pin select register 2

2.19 Programmable Pulse Generator

Table 2.37 is a comparison of programmable pulse generator registers.

Table 2.37 Comparison of the Programmable Pulse Generator Registers

Register	Bit	RX62N (PPG)	RX671 (PPG)
PPG1.PTRSLR	PTRSL	PPG trigger select bit 0: MTU0 to MTU3 selected as PPG1 trigger channels. 1: MTU6 to MTU9 selected as PPG1 trigger channels.	PPG trigger select register 0: MTU0 to MTU3 of the MTU selected as PPG1 trigger channels. 1: TPU0 to TPU3 of the TPU selected as PPG1 trigger channels.
NDRH2	—	—	Next data register H2
NDRL2	—	—	Next data register L2
PPG1.PCR	G0CMS [1:0]	Group 4 compare match select bits • PPG1.PTRSLR.PTRSL bit = 0 b1 b0 0 0: Compare match on MTU0 0 1: Compare match on MTU1 1 0: Compare match on MTU2 1 1: Compare match on MTU3 • PPG1.PTRSLR.PTRSL bit = 1 b1 b0 0 0: Compare match on MTU6 0 1: Compare match on MTU7 1 0: Compare match on MTU8 1 1: Compare match on MTU9	Group 4 compare match select bits • PPG1.PTRSLR.PTRSL bit = 0 b1 b0 0 0: Compare match on MTU0 0 1: Compare match on MTU1 1 0: Compare match on MTU2 1 1: Compare match on MTU3 • PPG1.PTRSLR.PTRSL bit = 1 b1 b0 0 0: Compare match on TPU0 0 1: Compare match on TPU1 1 0: Compare match on TPU2 1 1: Compare match on TPU3
	G1CMS [1:0]	Group 5 compare match select bits • PPG1.PTRSLR.PTRSL bit = 0 b3 b2 0 0: Compare match on MTU0 0 1: Compare match on MTU1 1 0: Compare match on MTU2 1 1: Compare match on MTU3 • PPG1.PTRSLR.PTRSL bit = 1 b3 b2 0 0: Compare match on MTU6 0 1: Compare match on MTU7 1 0: Compare match on MTU8 1 1: Compare match on MTU9	Group 5 compare match select bits • PPG1.PTRSLR.PTRSL bit = 0 b3 b2 0 0: Compare match on MTU0 0 1: Compare match on MTU1 1 0: Compare match on MTU2 1 1: Compare match on MTU3 • PPG1.PTRSLR.PTRSL bit = 1 b3 b2 0 0: Compare match on TPU0 0 1: Compare match on TPU1 1 0: Compare match on TPU2 1 1: Compare match on TPU3

Register	Bit	RX62N (PPG)	RX671 (PPG)
PPG1.PCR	G2CMS [1:0]	Group 6 compare match select bits • PPG1.PTRSLR.PTRSL bit = 0 b5 b4 0 0: Compare match on MTU0 0 1: Compare match on MTU1 1 0: Compare match on MTU2 1 1: Compare match on MTU3 • PPG1.PTRSLR.PTRSL bit = 1 b5 b4 0 0: Compare match on MTU6 0 1: Compare match on MTU7 1 0: Compare match on MTU8 1 1: Compare match on MTU9	Group 6 compare match select bits • PPG1.PTRSLR.PTRSL bit = 0 b5 b4 0 0: Compare match on MTU0 0 1: Compare match on MTU1 1 0: Compare match on MTU2 1 1: Compare match on MTU3 • PPG1.PTRSLR.PTRSL bit = 1 b5 b4 0 0: Compare match on TPU0 0 1: Compare match on TPU1 1 0: Compare match on TPU2 1 1: Compare match on TPU3
	G3CMS [1:0]	Group 7 compare match select bits • PPG1.PTRSLR.PTRSL bit = 0 b7 b6 0 0: Compare match on MTU0 0 1: Compare match on MTU1 1 0: Compare match on MTU2 1 1: Compare match on MTU3 • PPG1.PTRSLR.PTRSL bit = 1 b7 b6 0 0: Compare match on MTU6 0 1: Compare match on MTU7 1 0: Compare match on MTU8 1 1: Compare match on MTU9	Group 7 compare match select bits • PPG1.PTRSLR.PTRSL bit = 0 b7 b6 0 0: Compare match on MTU0 0 1: Compare match on MTU1 1 0: Compare match on MTU2 1 1: Compare match on MTU3 • PPG1.PTRSLR.PTRSL bit = 1 b7 b6 0 0: Compare match on TPU0 0 1: Compare match on TPU1 1 0: Compare match on TPU2 1 1: Compare match on TPU3
PPG1.PMR	G0NOV	Group 4 non-overlap bit 0: Normal operation (Output values updated on compare match A of selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected MTUn) (n = 0 to 3 and 6 to 9)	Group 4 non-overlap bit • PPG1.PTRSLR.PTRSL bit = 0 0: Normal operation (Output values updated on compare match A of selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected MTUn) (n = 0 to 3) • PPG1.PTRSLR.PTRSL = 1 0: Normal operation (Output values updated on compare match A of selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected TPUn) (n = 0 to 3)

Register	Bit	RX62N (PPG)	RX671 (PPG)
PPG1.PMR	G1NOV	Group 5 non-overlap bit 0: Normal operation (Output values updated on compare match A of selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected MTUn) (n = 0 to 3 and 6 to 9)	Group 5 non-overlap bit • PPG1.PTRSLR.PTRSL bit = 0 0: Normal operation (Output values updated on compare match A of selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected MTUn) (n = 0 to 3) • PPG1.PTRSLR.PTRSL bit = 1 0: Normal operation (Output values updated on compare match A of selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected TPUn) (n = 0 to 3)
	G2NOV	Group 6 non-overlap bit 0: Normal operation (Output values updated on compare match A of selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected MTUn) (n = 0 to 3 and 6 to 9)	Group 6 non-overlap bit • PPG1.PTRSLR.PTRSL bit = 0 0: Normal operation (Output values updated on compare match A of selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected MTUn) (n = 0 to 3) • PPG1.PTRSLR.PTRSL bit = 1 0: Normal operation (Output values updated on compare match A of selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected TPUn) (n = 0 to 3)

Register	Bit	RX62N (PPG)	RX671 (PPG)
PPG1.PMR	G3NOV	Group 7 non-overlap bit 0: Normal operation (Output values updated on compare match A of selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected MTUn) (n = 0 to 3 and 6 to 9)	Group 7 non-overlap bit • PPG1.PTRSLR.PTRSL bit = 0 0: Normal operation (Output values updated on compare match A of selected MTUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected MTUn) (n = 0 to 3) • PPG1.PTRSLR.PTRSL bit = 1 0: Normal operation (Output values updated on compare match A of selected TPUn) 1: Non-overlapping operation (Output values updated on compare match A or B of selected TPUn) (n = 0 to 3)

2.20 8-Bit Timer

Table 2.38 is a comparative overview of 8-bit timers, and Table 2.39 is a comparison of 8-bit timer registers.

Table 2.38 Comparative Overview of 8-Bit Timers

Item	RX62N (TMR)	RX671 (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external reset signal.	Selectable among compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	—	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0 or TMR2
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI5 and SCI6	Generation of SCI basic clock
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Each unit can be placed in a module stop state.	Ability to transition each unit to the module stop state

Table 2.39 Comparison of 8-Bit Timer Registers

Register	Bit	RX62N (TMR)	RX671 (TMRb)
TCSTR	—	—	Time counter start register

2.21 Compare Match Timer

Table 2.40 is a comparative overview of the compare match timers.

Table 2.40 Comparative Overview of Compare Match Timers

Item	RX62N (CMT)	RX671 (CMT)
Count clocks	Four frequency-divided clocks: One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.	Four frequency-divided clocks: One clock from among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected individually for each channel.
Interrupt	A compare match interrupt can be requested individually for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	Event signal output at CMT1 compare match
Event link function (input)	—	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	Each unit can be placed in a module stop state.	Each unit can be placed in a module stop state.

2.22 Realtime Clock

Table 2.41 is a comparative overview of the realtime clocks, and Table 2.42 is a comparison of realtime clock registers.

Table 2.41 Comparative Overview of Realtime Clocks

Item	RX62N (RTC)	RX671 (RTCd)
Count modes	Calendar count mode	Calendar count mode, binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (XCIN) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment — Start/stop function — Binary display of 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz status. — Clock (1 Hz) output	• Calendar count mode — Year, month, date, day of the week, hours, minutes, and seconds are counted and represented in BCD format — Selection of 12- or 24-hour mode — 30-second adjustment (30 seconds or less are rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute.) — Automatic leap year adjustment • Binary count mode — Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — Binary display of digits below seconds (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz) — Time error adjustment function — Clock (1 Hz/64 Hz) output
Interrupts	• Alarm interrupt (ALM) Year, month, date, day of the week, hours, minutes, and seconds can be selected as conditions for the alarm interrupt. • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/16 second, 1/64 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) Indicates occurrence of a carry to the seconds counter or a carry to the 64 Hz counter from the prescaler during reading of the 64 Hz counter.	• Alarm interrupt (ALM) Any of the following can be selected as conditions for the alarm interrupt: — Calendar count mode: Year, month, date, day of the week, hours, minutes, and seconds — Binary count mode: Each bit of 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as the interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings — When a carry from the 64 Hz counter to the second counter is generated. — When the 64 Hz counter is changed and the R64CNT register is read at the same time.

Item	RX62N (RTC)	RX671 (RTCd)
Interrupts	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt	• Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	—	Time capture using edge detection on the time capture event input pin is available. At each input event the month, date, hour, minute, and second is captured, or the 32-bit counter value is captured.
Event link function	—	Periodic event output

Table 2.42 Comparison of Realtime Clock Registers

Register	Bit	RX62N (RTC)	RX671 (RTCd)
BCNT0*1	—	—	Binary counter 0
BCNT1*1	—	—	Binary counter 1
RHRCNT	PM	—	PM bit
BCNT2*1	—	—	Binary counter 2
BCNT3*1	—	—	Binary counter 3
RDAYCNT	DAY1[3:0] (RX62N) DATE1[3:0] (RX671)	Ones place of days count bits	Ones place of days count bits
	DAY10[1:0] (RX62N) DATE10[1:0] (RX671)	Tens place of days count bits	Tens place of days count bits
RYRCNT	YEAR1[3:0] (RX62N) YR1[3:0] (RX671)	Ones place of years count bits	Ones place of years count bits
	YEAR10[3:0] (RX62N) YR10[3:0] (RX671)	Tens place of years count bits	Tens place of years count bits
	YEAR100[3:0]	Hundreds place of years count bits	—
	YEAR1000[3:0]	Thousands place of years count bits	—
BCNT0AR*1	—	—	Binary counter 0 alarm register
BCNT1AR*1	—	—	Binary counter 1 alarm register
RHRAR	HOUR1[3:0] (RX62N) HR1[3:0] (RX671)	Ones place of hours bits	Ones place of hours bits
	HOUR10[1:0] (RX62N) HR10[1:0] (RX671)	Tens place of hours bits	Tens place of hours bits
	PM	—	PM bit
BCNT2AR*1	—	—	Binary counter 2 alarm register

Register	Bit	RX62N (RTC)	RX671 (RTCd)
RWKAR	DAY[2:0] (RX62N) DAYW[2:0] (RX671)	Day-of-week setting bits	Day-of-week setting bits
BCNT3AR*1	—	—	Binary counter 3 alarm register
RDAYAR	DAY1[3:0] (RX62N) DATE1[3:0] (RX671)	Ones place of days bits	Ones place of days bits
	DAY10[1:0] (RX62N) DATE10[1:0] (RX671)	Tens place of days bits	Tens place of days bits
BCNT0AER*1	—	—	Binary counter 0 alarm enable register
BCNT1AER*1	—	—	Binary counter 1 alarm enable register
RYRAR	YEAR1[3:0] (RX62N) YR1[3:0] (RX671)	Ones place of years bits	Ones place of years bits
	YEAR10[3:0] (RX62N) YR10[3:0 (RX671)	Tens place of years bits	Tens place of years bits
	YEAR100[3:0]	Hundreds place of years bits	—
	YEAR1000[3:0]	Thousands place of years bits	—
BCNT2AER*1	—	—	Binary counter 2 alarm enable register
BCNT3AER*1	—	—	Binary counter 3 alarm enable register
RCR1	RTCOS	—	RTCOUT output select bit
	PES[2:0] (RX62N) PES[3:0] (RX671)	Periodic interrupt select bits (b6 to b4)	Periodic interrupt select bits (b7 to b4)
RCR2	ADJ (RX62N) ADJ30 (RX671)	30-second adjustment bit	30-second adjustment bit
	AADJE	—	Automatic adjustment enable bit
	AADJP	—	Automatic adjustment period select bit
	HR24	—	Hours mode bit
	CNTMD	—	Count mode select bit
RCR3	—	—	RTC control register 3
RCR4	—	—	RTC control register 4
RFRH RFRL	—	—	Frequency register H/L
RADJ	—	—	Time error adjustment register
RTCCRn	—	—	Time capture control register n (n = 0 to 2)
RSECCPn	—	—	Second capture register n (n = 0 to 2)

Register	Bit	RX62N (RTC)	RX671 (RTCd)
BCNT0CPn*1	—	—	BCNT0 capture register n (n = 0 to 2)
RMINCPn	—	—	Minute capture register n (n = 0 to 2)
BCNT1CPn*1	—	—	BCNT1 capture register n (n = 0 to 2)
RHRCPn	—	—	Hour capture register n (n = 0 to 2)
BCNT2CPn*1	—	—	BCNT2 capture register n (n = 0 to 2)
RDAYCPn	—	—	Date capture register n (n = 0 to 2)
BCNT3CPn*1	—	—	BCNT3 capture register n (n = 0 to 2)
RMONCPn	—	—	Month capture register n (n = 0 to 2)

Note: 1. In binary count mode

2.23 Watchdog Timer

Table 2.43 is a comparative overview of the watchdog timers, and Table 2.44 is a comparison of watchdog timer registers.

Table 2.43 Comparative Overview of Watchdog Timers

Item	RX62N (WDT)	RX671 (WDTA)
Count source	Peripheral module clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072	Divide by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting up using an 8-bit up-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Watchdog timer mode: The TCSR.TMS bit is set to 1 (watchdog timer mode) and the TCSR.TME bit is set to 1 (count start by TCNT counter). • Interval timer: The TCSR.TMS bit is cleared to 0 (interval timer mode) and the TCSR.TME bit is set to 1 (count start by TCNT counter).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the WDTRR register).
Conditions for stopping the counter	• Reset (The up-counter and other registers return to their initial values.) • An overflow occurs. • The TCSR.TME bit is cleared to 0 (TCNT counter initialized to 00h).	• Reset (The down-counter and other registers return to their initial values.) • Low power consumption state • Underflow or refresh error (register start mode only)
Window function	—	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Watchdog timer reset sources	In watchdog timer mode, a WDTOVF# signal is output externally when the counter overflows, and it is possible to select whether or not to internally reset the MCU at the same time.	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Interrupt sources	Interrupt sources • In interval timer mode, an interval timer interrupt (WOVI) is generated when the counter overflows.	Non-maskable interrupt/interrupt sources • Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Reading the counter value	The up-counter value can be read by reading the TCNT register.	The down-counter value can be read by reading the WDTSR register.

Table 2.44 Comparison of Watchdog Timer Registers

Register	Bit	RX62N (WDT)	RX671 (WDTA)
TCNT	—	Timer counter	—
TCSR	—	Timer control/status register	—
RSTCSR	—	Reset control/status register	—
WINA	—	Write window A register	—
WINB	—	Write window B register	—
WDTRR	—	—	WDT refresh register
WDTCR	—	—	WDT control register
WDTSR	—	—	WDT status register
WDTRCR	—	—	WDT reset control register

2.24 Independent Watchdog Timer

Table 2.45 is a comparative overview of the independent watchdog timers, and Table 2.46 is a comparison of independent watchdog timer registers.

Table 2.45 Comparative Overview of Independent Watchdog Timers

Item	RX62N (IWDT)	RX671 (IWDTa)
Count source	On-chip oscillator clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	IWDTCLK, IWDTCLK/16, IWDTCLK/32, IWDTCLK/64, IWDTCLK/128, IWDTCLK/256	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting starts when the down-counter is refreshed (by writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (The down-counter and other registers return to their initial values.) • An underflow occurs.	• Reset (The down-counter and other registers return to their initial values.) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	—	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
Reset output sources	• Down-counter underflow	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Interrupt sources	—	Non-maskable interrupt/interrupt sources • Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the IWDTSR register.	The down-counter value can be read by reading the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX62N (IWDT)	RX671 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	—	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits)	• Selecting the clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.46 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX62N (IWDT)	RX671 (IWDTa)
IWDTCR	—	IWDT control register	IWDT control register
		Initial values after a reset are different.	
	CKS[3:0]	Clock selection bits b7 b4 0 0 – –: IWDTCLK 0 1 0 0: IWDTCLK/16 0 1 0 1: IWDTCLK/32 0 1 1 0: IWDTCLK/64 0 1 1 1: IWDTCLK/128 1 – – –: IWDTCLK/256	Clock frequency division ratio select bits b7 b4 0 0 0 0: No division 0 0 1 0: ×1/16 0 0 1 1: ×1/32 0 1 0 0: ×1/64 0 1 0 1: ×1/256 1 1 1 1: ×1/128 Settings other than the above are prohibited.
	RPES[1:0]	—	Window end position select bits
	RPSS[1:0]	—	Window start position select bits
IWDTSR	REFEF	—	Refresh error flag
IWDTRCR	—	—	IWDT reset control register
IWDTCSTPR	—	—	IWDT count stop control register

2.25 USB 2.0 Host/Function Module

Table 2.47 is a comparative overview of the USB 2.0 Host/Function modules, and Table 2.48 is a comparison of USB 2.0 Host/Function module registers.

Table 2.47 Comparative Overview of USB 2.0 Host/Function Modules

Item	RX62N (USB)	RX671 (USBb)
Features	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 • Two ports are provided. • USB OTG is supported. • USB host controller and function controller (which can be switched by software) • Self-power mode or bus-power mode can be selected. When Host controller operation is selected: • Full-speed transfer (12 Mbps) is supported.*1 • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub When Function controller operation is selected: • Support for full-speed transfer (12 Mbps)*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function	• Integrated USB Device Controller (UDC) and transceiver for USB 2.0 Support for Host controller, Function controller, and USB OTG functionality (two channels) • Software can switch between the Host controller and Function controller modes. • Self-power mode or bus-power mode can be selected. When Host controller operation is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling of SOF and packet transmissions • Transfer interval setting function for isochronous and interrupt transfers • Communication with multiple peripheral devices connected via a single hub When Function controller operation is selected: • Support for full-speed transfer (12 Mbps)*1 • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS requests • SOF interpolation function
Communication data transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer
Internal bus interface	Connected to internal peripheral bus 3	Connected to internal peripheral bus 3

Item	RX62N (USB)	RX671 (USBb)
Pipe configuration	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9. Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC), buffer size: 8, 16, 32, and 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer, bulk transfer buffer size: 8, 16, 32, and 64 bytes (support for double buffer setting), isochronous transfer buffer size: 1 to 256 bytes (support for double buffer setting) • PIPE3 to PIPE5: Bulk transfer only, buffer size: 8, 16, 32, and 64 bytes (support for double buffer setting) • PIPE6 to PIPE9: Interrupt transfer only: buffer size: 1 to 64 bytes (single buffer)	• Buffer memory for USB communication is provided. • Up to ten pipes can be selected (including the default control pipe). • Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9. Transfer conditions that can be set for each pipe: • PIPE0: Control transfer only (default control pipe: DPC), buffer size: 64 bytes (single buffer) • PIPE1 and PIPE2: Bulk transfer or isochronous transfer, bulk transfer buffer size: 64 bytes (support for double buffer setting), isochronous transfer buffer size: 256 bytes (support for double buffer setting) • PIPE3 to PIPE5: Bulk transfer only, buffer size: 64 bytes (support for double buffer setting) • PIPE6 to PIPE9: Interrupt transfer only: buffer size: 64 bytes (single buffer)
Other functions	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK)	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip D+/D– pull-up and pull-down resistors
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state

Note: 1. Low-speed transfer (1.5 Mbps) is not supported.

Table 2.48 Comparison of USB 2.0 Host/Function Module Registers

Register	Bit	RX62N (USB)	RX671 (USBb)
SYSSTS0	LNST[1:0]	USB data line status monitor bits b1 b0 0 0: SE0 0 1: J-State 1 0: K-State 1 1: SE1	USB data line status monitor flags • Full-speed operation b1 b0 0 0: SE0 0 1: J-State 1 0: K-State 1 1: SE1 • Low-speed operation (only when Host controller is selected) b1 b0 0 0: SE0 0 1: K-State 1 0: J-State 1 1: SE1
	SOFEA	—	SOF active monitor when Host controller is selected bit
DVSTCTR0	RHST[2:0]	USB bus reset status bits • When the Host controller function is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection*1 0 1 0: Full-speed connection • When the Function controller function is selected b2 b0 0 0 0: Communication speed not determined 0 1 0: USB bus reset in progress or full-speed connection	USB bus reset status flags • When the Host controller function is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection • When the Function controller function is selected b2 b0 0 0 0: Communication speed not determined 0 0 1: USB bus reset in progress 0 1 0: USB bus reset in progress or full-speed connection
SOFCFG	TRNENSEL	—	Transaction-enabled time select bit
DEVADDn (n = 0 to 5)	USBSPD[1:0]	Transfer speed of communication target device bits b7 b6 0 0: DEVADDn register is not used. 0 1: Setting prohibited. 1 0: Full speed 1 1: Setting prohibited.	Transfer speed of communication target device bits b7 b6 0 0: DEVADDn register is not used. 0 1: Low speed 1 0: Full speed 1 1: Setting prohibited.

Register	Bit	RX62N (USB)	RX671 (USBb)
PHYSLEW	—	—	PHY cross point adjustment register
DPUSR0R	RPUE0	—	USB0 D+ pull-up resistor control bit
	DRPD0	—	USB0 D+/D– pull-down resistor control bit
	SRPC1	USB1 single end receiver control bit	—
	FIXPHY1	USB1 transceiver output fix bit	—
	DP1	USB1 DP input	—
	DM1	USB1 DM input	—
	DOVCA1	USB1 OVRCURA input	—
	DOVCB1	USB1 OVRCURB input	—
	DVBSTS1	USB1 VBUS input	—
DPUSR1R	DPINTE1	USB1 DP interrupt enable/clear bit	—
	DMINTE1	USB1 DM interrupt enable/clear bit	—
	DPINTE1	USB1 DP interrupt enable/clear bit	—
	DMINTE1	USB1 DM interrupt enable/clear bit	—
	DOVRCRAE1	USB1 OVRCURA interrupt enable/clear bit	—
	DOVRCRBE1	USB1 OVRCURB interrupt enable/clear bit	—
	DVBSE1	USB1 VBUS interrupt enable/clear bit	—
	OVRCURAINT0 (RX62N) DOVRCRA0 (RX671)	USB0 OVRCURA interrupt source recovery bit	USB0 OVRCURA interrupt source recovery flag
	OVRCURBINT0 (RX62N) DOVRCRB0 (RX671)	USB0 OVRCURB interrupt source recovery bit	USB0 OVRCURB interrupt source recovery flag
	DPINT1	USB1 DP interrupt source recovery flag	—
	DMINT1	USB1 DM interrupt source recovery flag	—
	DOVRCRA1	USB1 OVRCURA interrupt source recovery flag	—
	DOVRCRB1	USB1 OVRCURB interrupt source recovery flag	—
	DVBINT1	USB1 VBUS interrupt source recovery flag	—

Note: 1. The USB controller does not support communication with low-speed devices. Higher-level applications should perform abnormal connection processing if this value is read.

2.26 Serial Communications Interface

Table 2.49 is a comparative overview of the serial communications interfaces, Table 2.50 is a comparative listing of serial communications interface channels, and Table 2.51 is a comparison of serial communications interface registers.

Table 2.49 Comparative Overview of Serial Communications Interfaces

Item		RX62N (SCIa)	RX671 (SCIk, SCIm, SCIh)
Number of channels		• SCIa: 6 channels	• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous operation • Clock synchronous operation • Smart card interface	• Asynchronous operation • Clock synchronous operation • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable using on-chip baud rate generator.	Bit rate specifiable using on-chip baud rate generator.
Full-duplex communication		• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering	• Transmitter: Support for continuous transmission using double-buffering • Receiver: Support for continuous reception using double-buffering
Data transfer		Selectable between LSB-first and MSB-first	Selectable between LSB-first and MSB-first
I/O signal level inversion		—	Ability to invert levels of input and output signals independently
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error	• Transmit end, transmit data empty, receive data full, receive error, receive data ready, data match • Completion of generation of a start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		Ability to set module stop state for each channel	Ability to transition each channel to module stop state
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even, odd, or none	Even, odd, or none
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	—	Ability to use CTSn# and RTSn# pins for transmission and reception control

Item		RX62N (SCIa)	RX671 (SCIk, SCIm, SCIh)
Asynchronous mode	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception
	Data match detection	—	Ability to compare receive data and comparison data, and generates an interrupt when they match
	Start-bit detection	—	Selectable between low level and falling edge
	Receive data sampling timing adjustment	—	Ability to change the sampling point for receive data forward or backward relative to a reference point at the center of the data
	Transmit signal change timing adjustment	—	Ability to delay the falling or rising edge of the transmit data
	Break detection	Ability to detect a break when a framing error occurs by reading the level of the RXDn pin directly	Ability to detect a break when a framing error occurs by reading the level of the RXDn pin directly or reading the SPTR.RXDMON flag
	Clock source	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5 and SCI6)	• Selectable between internal or external clock • Ability to input transfer rate clock from TMR (SCI5, SCI6, and SCI12)
	Double-speed mode	—	Ability to select baud rate generator double-speed mode
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation function	—	The input signal paths from the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	—	Ability to use CTSn# and RTSn# pins for transmission and reception control
	Transmit/receive FIFO	—	Ability to use 16-stage FIFOs for transmission and reception
Smart card interface mode	Error processing	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission	• Automatic transmission of an error signal at detection of a parity error during reception • Automatic re-transmission of data at reception of an error signal during transmission
	Data type	Support for direct convention and inverse convention	Support for direct convention and inverse convention

Item		RX62N (SCIa)	RX671 (SCIk, SCIm, SCIh)
Simple I²C mode	Communication format	—	I²C bus format
	Operating mode	—	Master (single-master operation only)
	Transfer speed	—	Support for fast mode
	Noise cancellation	—	• The SSCLn and SSDAn input signal paths incorporate digital noise filters. • The noise cancellation interval is adjustable.
Simple SPI mode	Data length	—	8 bits
	Error detection	—	Overrun error
	SS input pin function	—	Ability to place output pins in high-impedance state by applying a high-level signal to the SSn# pin.
	Clock settings	—	Ability to select among four clock phase and clock polarity settings
Event link function (supported by SCI5 only)		—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output
Bit rate modulation function		—	Ability to reduce errors by correcting output from the on-chip baud rate generator
Extended serial mode (supported by SCI12 only)	Start Frame transmission	—	• Ability to output Break Field low width/output completion interrupt function • Bus collision detection function/detection interrupt function
	Start Frame reception	—	• Ability to detect Break Field low width/detection completion interrupt function • Control Field 0 and Control Field 1 data comparison/ match interrupt function • Ability to select between two data types for comparison (primary and secondary) in Control Field 1 • Ability to set priority interrupt bit in Control Field 1 • Support for Start Frames that do not include a Break Field • Support for Start Frames that do not include Control Field 0 • Bit rate measurement function

Item		RX62N (SCIa)	RX671 (SCIk, SCIm, SCIh)
Extended serial mode (supported by SCI12 only)	I/O control function	—	• Ability to select polarity of TXDX12 and RXDX12 signals • Ability to specify digital filter function for RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select sampling timing for data received on RXDX12
	Timer function	—	Usable as reload timer

Table 2.50 Comparative Listing of Serial Communications Interface Channels

Item	RX62N (SCIa)	RX671 (SCIk, SCIm, SCIh)
Asynchronous mode	SCI0 to SCI3, SCI5, SCI6	SCI0 to SCI12
Clock synchronous mode	SCI0 to SCI3, SCI5, SCI6	SCI0 to SCI12
Smart card interface mode	SCI0 to SCI3, SCI5, SCI6	SCI0 to SCI12
Simple I^2C mode	—	SCI0 to SCI12
Simple SPI mode	—	SCI0 to SCI12
Extended serial mode	—	SCI12
TMR clock input	SCI5, SCI6	SCI5, SCI6, SCI12
Event link function	—	SCI5
FIFO mode	—	SCI10, SCI11
Data match detection	—	SCI0 to SCI11
Peripheral module clock	PCLK: SCI0 to SCI3, SCI5, SCI6	PCLKB: SCI0 to SCI9, SCI12 PCLKA: SCI10, SCI11

Table 2.51 Comparison of Serial Communications Interface Registers

Register	Bit	RX62N (SCIa)	RX671 (SCIk, SCIm, SCIh)
SMR	CHR	Character length bit (Valid only in asynchronous mode) 0: Selects 8 bits as the data length for transmission and reception 1: Selects 7 bits as the data length for transmission and reception	Character length bit (Valid only when SCMR.SMIF = 0 in asynchronous mode) Selection is made in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Selects 9 bits as the data length for transmission and reception 0 1: Selects 9 bits as the data length for transmission and reception 1 0: Selects 8 bits as the data length for transmission and reception 1 1: Selects 7 bits as the data length for transmission and reception
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode	Communications mode bit 0: Asynchronous mode or simple I^2C mode 1: Clock synchronous mode or simple SPI mode
SCMR	CHR1	—	Character length bit 1
SEMR	ITE	—	Immediate transmit enable bit
	BRME	—	Bit rate modulation enable bit
	ABCSE	—	Clock-synchronous basic clock select extended bit
	NFEN	—	Digital noise filter function enable bit
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
RDRH, RDRL, RDRHL	—	—	Receive data register H, L, HL
FRDR	—	—	Receive FIFO data register
TDRH, TDRL, TDRHL	—	—	Transmit data register H, L, HL
FTDR	—	—	Transmit FIFO data register
SSRFIFO	—	—	Serial status register
MDDR	—	—	Modulation duty register
SNFR	—	—	Noise filter setting register
SIMR1	—	—	I^2C mode register 1
SIMR2	—	—	I^2C mode register 2
SIMR3	—	—	I^2C mode register 3
SISR	—	—	I^2C states register
SPMR	—	—	SPI mode register
FCR	—	—	FIFO control register

Register	Bit	RX62N (SCIa)	RX671 (SCIk, SCIm, SCIh)
FDR	—	—	FIFO data count register
LSR	—	—	Line status register
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register
ESMER	—	—	Extended serial mode enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control field 0 data register
CF0CR	—	—	Control field 0 compare enable register
CF0RR	—	—	Control field 0 receive data register
PCF1DR	—	—	Primary control field 1 data register
SCF1DR	—	—	Secondary control field 1 data register
CF1CR	—	—	Control field 1 compare enable register
CF1RR	—	—	Control field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

2.27 I²C bus Interface

Table 2.52 is a comparative overview of the I²C bus interfaces, and Table 2.53 is a comparison of I²C bus interface registers.

Table 2.52 Comparative Overview of I²C Bus Interfaces

Item	RX62N (RIIC)	RX671 (RIICa)
Communication format	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Selectable between master mode or slave mode. • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Up to 1 Mbps	Fast mode is supported (up to 1 Mbps).
Serial clock (SCL)	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detection conditions	• Start, restart, and stop conditions are generated automatically. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are generated automatically. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave addresses	• Three slave addresses can be specified. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is loaded automatically. — Transfer of the next data for transmission can be suspended automatically on reception of a not-acknowledge bit. • For reception, the acknowledge bit is transmitted automatically. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	For reception, the following wait periods can be obtained by holding the SCL clock at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles (wait function)	For reception, the following wait periods can be obtained by holding the SCL line at the low level: • Wait between the eighth and ninth clock cycles • Wait between the ninth and first clock cycles
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX62N (RIIC)	RX671 (RIICa)
Arbitration	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.	• Multi-master support — Operation to synchronize the SCL clock in cases of conflict with the SCL clock from another master is possible. — When issuing a start condition, loss of arbitration is detected by testing for non-matching of the signals for the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching of transmit data. • Loss of arbitration due to detection of a start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • Loss of arbitration in transfer of a not-acknowledge bit due to the signals for the SDA line not matching is detectable. • Loss of arbitration due to non-matching of data is detectable in slave transmission.
Timeout detection function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise canceler	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the bandwidth for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events (detection of AL, NACK, time-out, a start condition including a restart condition, or a stop condition) • Receive-data-full (including matching with a slave address) • Transmit-data-empty (including matching with a slave address) • Transmission complete	Four sources: • Error in transfer or occurrence of events (detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition) • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end
Low power consumption function	Module stop state can be set.	Ability to transition to module stop state.
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode

Item	RX62N (RIIC)	RX671 (RIICa)
Event link function (output)	—	Four sources (RIIC0): • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmit end

Table 2.53 Comparison of I²C Bus Interface Registers

Register	Bit	RX62N (RIIC)	RX671 (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNT	—	Timeout internal counter	—

2.28 CAN Module

Table 2.54 is a comparative overview of the CAN modules, and Table 2.55 is a comparison of CAN module registers.

Table 2.54 Comparative Overview of CAN Modules

Item	RX62N (CAN)	RX671 (CAN)
Number of channels	1 channel	2 channels
Protocol	ISO 11898-1 compliant (standard and extended frames)	ISO 11898-1 compliant (standard and extended frames)
Bit rate	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source	Programmable bit rate below 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	32 mailboxes: Two selectable mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for either transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for either transmission or reception. Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.
Reception	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be received. • Selectable receiving ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot reception function • Selectable between overwrite mode (messages overwritten) and overrun mode (messages discarded) • Reception-complete interrupt can be individually enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.	• Eight acceptance masks (one mask for every four mailboxes) • The mask can be individually enabled or disabled for each mailbox.

Item	RX62N (CAN)	RX671 (CAN)
Transmission	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.	• Data frames and remote frames can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) • Programmable one-shot transmission function • Selectable between ID priority mode and mailbox number priority mode • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission-complete interrupt can be individually enabled or disabled for each mailbox.
Mode transition for bus-off recovery	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program	The mode transition for recovery from the bus-off state can be selected. • ISO 11898-1 compliant • Automatic transition to CAN halt mode at bus-off start • Automatic transition to CAN halt mode at bus-off end • Transition to CAN halt mode by a program • Transition to error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off start, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.	• Time stamp function using a 16-bit counter • The reference clock can be selected from 1-, 2-, 4- and 8-bit time periods.
Interrupt function	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)	Five interrupt sources (reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupt)
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Current consumption can be reduced by stopping the CAN clock.
Software support units	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	Three software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
CAN clock source	Peripheral module clock (PCLK)	Peripheral module clock (PCLKB), CANMCLK

Item	RX62N (CAN)	RX671 (CAN)
Test mode	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	Three test modes for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.55 Comparison of CAN Module Registers

Register	Bit	RX62N (CAN)	RX671 (CAN)
BCR	CCLKS	—	CAN clock source select bit

2.29 Serial Peripheral Interface

Table 2.56 is a comparative overview of the serial peripheral interfaces, and Table 2.57 is a comparison of serial peripheral interface registers.

Table 2.56 Comparative Overview of Serial Peripheral Interfaces

Item	RX62N (RSPI)	RX671 (RSPId)
Number of channels	2 channels	3 channels
RSPI transfer functions	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Ability to perform transmit-only operation • Capable of serial communications in master/slave mode • Ability to switch the polarity of serial transfer clock • Ability to switch the phase of serial transfer clock	• Ability to use MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals to implement serial communication through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Communication mode: Selectable between full-duplex and simplex (transmit-only or receive-only (in slave mode)) • Ability to switch the polarity of RSPCK • Ability to switch the phase of RSPCK
Data format	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame)	• Selectable between MSB-first and LSB-first • Ability to select transfer bit length among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, and 32 bits • 128-bit transmit/receive buffers • Ability to transfer up to four frames in each round of transmission/reception (with up to 32 bits per frame) • Ability to swap transmit/receive data in byte units • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, the externally input clock is used as the serial clock (the maximum frequency is that of PCLK divided by 8). — Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (division ratio: 2 to 4,096). • In slave mode, PCLK divided by a minimum of 4 can be input as RSPCK (RSPCK maximum frequency: PCLK divided by 4). — Width at high level: 2 cycles of PCLK; width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for both the transmit and receive buffers • 128 bits for the transmit/receive buffers

Item	RX62N (RSPI)	RX671 (RSPId)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection When master receive and the RSPCK auto-stop function are enabled, the transfer clock stops at the point in time when overrun error detection occurs, so no overrun error is generated. • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLn0 to SSLn3) per channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode, the SSLn0 pin is input, and SSLn1 to SSLn3 pins are either output or unused. • In slave mode, the SSLn0 pin is input, and SSLn1 to SSLn3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity	• Four SSL pins (SSLx0 to SSLx3) per channel • In single-master mode, SSLx0 to SSLx3 pins are output. • In multi-master mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are either output or unused. • In slave mode, the SSLx0 pin is input, and SSLx1 to SSLx3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Controllable wait until next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: One RSPCK cycle • Function for changing SSL polarity
Control during master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified.	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following items can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value at SSL negation can be specified. • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.

Item	RX62N (RSPI)	RX671 (RSPId)
Interrupt sources	Maskable interrupt sources • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources • Receive buffer full interrupt • Transmit buffer empty interrupt • Error interrupt (mode fault, overrun, underrun, or parity error) • Idle interrupt • Communication end interrupt
Event link function (output)	—	The following events can be output to the event link controller (RSPI0): • Receive buffer full event signal • Transmit buffer empty event signal • Error events (mode fault, overrun, underrun, parity error) • Idle events • Communication completion events
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.57 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX62N (RSPI)	RX671 (RSPId)
SPPCR	SPOM	RSPI output pin mode bit	—
SPSR	MODF	Mode fault error flag 0: No mode fault error occurred 1: A mode fault error occurred	Mode fault error flag 0: No mode fault error occurred, no underrun error occurred. 1: A mode fault error occurred, an underrun error occurred.
	UDRF	—	Underrun error flag
	SPCF	—	Communication completion flag
SPDR	—	RSPI data register Possible access sizes: • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Possible access sizes: • Longword access (SPDCR.SPLW = 1, SPBYTE = 0) • Word access (SPDCR.SPLW = 0, SPBYTE = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SLSEL[1:0]	SSL pin output selection bits	—
	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: No transmit data parity bit appended No parity checking is performed on receive data. 1: A transmit data parity bit is appended. Parity checking is performed on receive data.	Parity enable bit 0: No transmit data parity bit appended No parity checking is performed on receive data. 1: A transmit data parity bit is appended, and parity checking is performed on receive data (when SPCR.TXMD = 0). A parity bit is appended to transmit data, but no parity checking is performed on receive data (when SPCR.TXMD = 1).
	SCKASE	—	RSPCK auto-stop function enable bit
SPDCR2	—	—	RSPI data control register 2
SPCR3	—	—	RSPI control register 3

2.30 CRC Calculator

Table 2.58 is a comparative overview of the CRC calculators, and Table 2.59 is a comparison of CRC calculator registers.

Table 2.58 Comparative Overview of CRC Calculators

Item	RX62N (CRC)	RX671 (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC code generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on eight bits in parallel	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ — $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	CRC code generation for LSB-first or MSB-first communication selectable	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	
Low power consumption function	Module stop state can be set	Ability to transition to module stop state	

Table 2.59 Comparison of CRC Calculator Registers

Register	Bit	RX62N (CRC)	RX671 (CRCA)
CRCCR	GPS[1:0] (RX62N) GPS[2:0] (RX671)	CRC generating polynomial switching bits (b1, b0) b1 b0 0 0: No calculation is executed. 0 1: $X^8 + X^2 + X + 1$ 1 0: $X^{16} + X^{15} + X^2 + 1$ 1 1: $X^{16} + X^{12} + X^5 + 1$	CRC generating polynomial switching bits (b2 to b0) b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register • When generating 16-bit or 8-bit CRCs CRC data input register (b7 to b0)	CRC data input register • When generating 32-bit CRCs CRC data input register (b31 to b0) • When generating 16-bit or 8-bit CRCs CRC data input register (b7 to b0)
CRCDOR	—	CRC data output register • When generating 16-bit CRCs CRC data output register (b15 to b0) The bottom byte (b7 to b0) is used when generating 8-bit CRCs.	CRC data output register • When generating 32-bit CRCs CRC data output register (b31 to b0) • When generating 16-bit CRCs CRC data output register (b15 to b0) • When generating 8-bit CRCs CRC data output register (b7 to b0)

2.31 Boundary Scan

Table 2.60 is a comparative overview of the boundary scan functions, and Table 2.61 is a comparison of boundary scan registers.

Table 2.60 Comparative Overview of Boundary Scan Functions

Item	RX62N	RX671
Boundary scan enable/disable	Boundary scan is enabled when the EMLE pin is driven low and the BSCANP pin is driven high.	Boundary scan is enabled when the RES# pin and the BSCANP pin are driven high and the EMLE pin is driven low.
Dedicated boundary scan pins	The following pins are used exclusively by the JTAG when the boundary scan function is enabled (TDO, TCK, TDI, TMS, and TRST#): • 176-pin LFBGA products: PF0, PF1, PF2, PF3, and PF4 • 145-pin TFLGA and 144-pin LQFP products: P26, P27, P30, P31, and P34 • 85-pin TFLGA products: P26, P27, P30, P31, and P34	The following pins are used exclusively by the JTAG when the boundary scan function is enabled (TDO, TCK, TDI, TMS, and TRST#): • 145-pin TFLGA and 64-pin TFBGA products: P26, P27, P30, P31, and P34
Six test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

Table 2.61 Comparison of Boundary Scan Registers

Register	Bit	RX62N	RX671
JTIDR	—	ID code register	ID code register
		Initial value after a reset differs.	

2.32 12-Bit A/D Converter

Table 2.62 is a comparative overview of the 12-bit A/D converters, and Table 2.63 is a comparison of 12-bit A/D converter registers and Table 2.64 is a comparison of A/D conversion start triggers that can be set in the ADSTRGR registers.

Table 2.62 Comparative Overview of 12-Bit A/D Converters

Item	RX62N (S12AD)	RX671 (S12ADFa)
Number of units	1 unit (S12AD0)	2 units (S12AD and S12AD1)
Input channels	8 channels	S12AD: 8 channels S12AD1: 12 channels + one extended channel
Extended analog function	—	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when operating with peripheral module clock PCLK = 50 MHz)	(0.48 µs) per channel (12-bit conversion mode) (0.45 µs) per channel (10-bit conversion mode) (0.42 µs) per channel (8-bit conversion mode) (Operating with A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock (ADCLK)	4 clocks: PCLK, PCLK/2, PCLK/4, PCLK/8	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the division ratio is one of the following: — PCLK: ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 • ADCLK is set using the clock generation circuit.
Data register	• 8 data registers • The results of A/D conversion are stored in 12-bit A/D data registers.	• For analog input: 20 data registers (S12AD: 8 data registers, S12AD1: 12 data registers), one data register for each unit for A/D conversion data multiplexing in double trigger mode, two data registers for each unit for A/D conversion data multiplexing in double trigger mode extended operation • For temperature sensor: One data register (S12AD1) • For internal reference voltage: One data register (S12AD1) • 1 register per unit for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion

Item	RX62N (S12AD)	RX671 (S12ADFa)
Data register	• In A/D-converted value addition mode, 14 bits of data are stored in an A/D data register.	• In value addition mode, the value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating mode	• Single-cycle scan mode: — A/D conversion is performed only once on the analog inputs of up to 8 user-selected channels. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 8 user-selected channels.	Operating modes can be set independently for two units. • Single scan mode: — A/D conversion is performed only once on the analog inputs of user-selected channel. — A/D conversion is performed only once on the temperature sensor output (S12AD1). — A/D conversion is performed only once on the internal reference voltage (S12AD1). — A/D conversion is performed only once on the extended analog input (S12AD1). • Continuous scan mode: — A/D conversion is performed repeatedly on the arbitrarily selected analog inputs, temperature sensor output (S12AD1), and internal reference voltage (S12AD1).

Item	RX62N (S12AD)	RX671 (S12ADFa)
Operating mode		• Group scan mode: — Either two (A and B) or three (A, B, and C) groups can be selected. (When the number of groups selected is two, only the combination of group A and group B is selectable.) — The analog inputs of user-selected channels, the temperature sensor output (S12AD1), or the internal reference voltage (S12AD1) are divided up among group A and group B, or among groups A, B, and C, and A/D conversion is performed only once on the analog inputs selected as a group unit. — The conditions for scanning start of groups A, B, and C (synchronous trigger) can be independently selected, thus allowing A/D conversion of each group to be started independently. • Group scan mode (with group priority control selected): — If a priority-group trigger is input during scanning of the low-priority group, scan of the low-priority group is stopped and scan of the priority group is started. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning of the low-priority group after processing for the high-priority group completes, is selectable. Rescan can also be set to start either from the beginning of the selected channel or the channel on which A/D conversion is not completed.
A/D conversion start conditions	• Software trigger • Conversion start is triggered by the Multi-function timer pulse unit (MTU) and 8-bit timer (TMR). • External trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the MTU, TPU, TMR, and ELC. • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin (S12AD) or ADTRG1# pin (S12AD1). (independently for two units)

Item	RX62N (S12AD)	RX671 (S12ADFa)
Functions	• Sample-and-hold function • Selectable A/D-converted value adding mode	• Variable sampling state count (ability to set for each channel independently) • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Function for switching among 12-, 10-, and 8-bit conversion • A/D data register auto-clear function • Extended analog input function • Compare function (window A, window B)
Interrupt sources	• An scan end interrupt request (S12ADI0) can be generated on completion of A/D conversion.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a single scan. (independently for two units) • In double trigger mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan. (independently for two units) • In group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (S12GBADI or S12GBADI1) can be generated, and on completion of a group C scan a dedicated group C scan end interrupt request (S12GCADI or S12GCADI1) can be generated. • When double trigger mode is selected in group scan mode, a scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of two scans of group A. On completion of two scans of group B or C a dedicated group B or group C scan end interrupt request (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated.

Item	RX62N (S12AD)	RX671 (S12ADFa)
Interrupt sources	• An S12ADI0 interrupt can activate the DMA controller (DMAC) and data transfer controller (DTC).	• A compare interrupt (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated when the digital compare function comparison conditions are met. • The DMA controller (DMAC) or data transfer controller (DTC) can be activated by the S12ADI/S12ADI1, S12GBADI/S12GBADI1, or S12GCADI/S12GCADI1 interrupt.
Event link function	—	• An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC.
Low power consumption function	Module stop state can be set.	Module stop state can be set.

Table 2.63 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX62N (S12AD)	RX671 (S12ADFa)
ADDRn	—	A/D data register n (n = 0 to 7)	A/D data register n (n = 0 to 11)
ADCSR	—	A/D control register ADCSR is an 8-bit register.	A/D control register ADCSR is a 16-bit register.
	EXTRG	Trigger select bit (b0)	Trigger select bit (b8)
	TRGE	Trigger start enable bit (b1)	Trigger start enable bit (b9)
	CKS[1:0]	A/D conversion clock select bits	—
	ADIE	Scan end interrupt enable bit (b4)	Scan end interrupt enable bit (b12)
	ADCS (RX62N) ADCS[1:0] (RX671)	Scan mode select bit (b6) 0: Single-cycle scan mode 1: Continuous scan mode	Scan mode select bits (b14, b13) b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited.
	ADST	A/D conversion start bit (b7)	A/D conversion start bit (b15)
	DBLANS[4:0]	—	Double trigger channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
ADANS (RX62N) ADANSA0 (RX671)	—	A/D channel select register	A/D channel select register A0
ADANSB0	—	—	A/D channel select register B0
ADANSC0	—	—	A/D channel select register C0
ADADS (RX62N) ADADS0 (RX671)	—	A/D-converted value addition mode select register	A/D-converted value addition/ average function select register 0
ADADS1	—	A/D-converted value addition mode select register 1	—

Register	Bit	RX62N (S12AD)	RX671 (S12ADFa)
ADADC	ADC[1:0] (RX62N) ADC[2:0] (RX671)	Addition count select bits (b1, b0) b1 b0 0 0: 1-time conversion (no addition, same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice) 1 1: 4-time conversion (addition three times)	Addition count select bits (b2 to b0) b2 b0 0 0 0: 1-time conversion (no addition, same as normal conversion) 0 0 1: 2-time conversion (addition once) 0 1 0: 3-time conversion (addition twice) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times) Settings other than the above are prohibited.
	AVEE	—	Average mode enable bit
ADCER	ADPRC[1:0]	—	A/D conversion resolution setting bit
	DIAGVAL[1:0]	—	Self-diagnostic conversion voltage select bits
	DIAGLD	—	Self-diagnostic mode select bit
	DIAGM	—	Self-diagnostic enable bit
ADSTRGR	ADSTRS[3:0] (RX62N) TRSA[5:0] (RX671)	A/D conversion start trigger select bits (b3 to b0) Refer to Table 2.64 for details	A/D conversion start trigger select bits (b13 to b8) Refer to Table 2.64 for details
	TRSB[5:0]	—	A/D conversion start trigger select for group B bits
ADDBLDR	—	—	A/D data duplication register
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADTSDR	—	—	A/D temperature sensor data register
ADOCDR	—	—	A/D internal reference voltage data register
ADRD	—	—	A/D self-diagnosis data register
ADEXICR	—	—	A/D conversion extended input control register
ADGCEXCR	—	—	A/D group C extended input control register
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	—	A/D sampling state register n (n = 0 to 11, T, or O)
ADDISCR	—	—	A/D disconnection detection control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0

Register	Bit	RX62N (S12AD)	RX671 (S12ADFa)
ADCMPANSER	—	—	A/D comparison function window A extended input select register
ADCMPLR0	—	—	A/D comparison function window A comparison condition setting register 0
ADCMPLER	—	—	A/D comparison function window A extended input comparison condition setting register
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADCMPSER	—	—	A/D comparison function window A extended input channel status register
ADWINMON	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADSAM	—	—	A/D conversion time setting register
ADSAMPR	—	—	A/D conversion time setting protection release register

Table 2.64 Comparison of A/D Conversion Start Triggers Set in ADSTRGR Register

Bit	RX62N (S12ADa)	RX671 (S12ADFa)
ADSTRS[3:0] (RX62N) TRSA[5:0] (RX671)	A/D conversion start trigger select bits b3 b0 0 0 0 0: A/D conversion startup trigger pin 0 0 0 1: TRG0AN_0 0 0 1 0: TRG0BN_0 0 0 1 1: TRGAN_0 0 1 0 0: TRGAN_1 0 1 0 1: TRG0EN_0 0 1 1 0: TRG0FN_0 0 1 1 1: TRG04ABN_0 1 0 0 0: TRG04ABN_1 1 0 0 1: TMTRG0AN_0 1 0 1 0: TMTRG0AN_1	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TPTRGAN 1 0 0 0 0 0: TPTRG0AN 1 1 0 0 0 0: ELCTRG0N/ELCTRG1N

2.33 RAM

Table 2.65 is a comparative overview of the RAM, and Table 2.66 is a comparison of RAM registers.

Table 2.65 Comparative Overview of RAM

Item	RX62N	RX671
Capacity	• 64 KB RAM0: 64 KB • 96 KB RAM0: 64 KB, RAM1: 32 KB	• 384 KB
Address	• When the RAM capacity is 64 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: None • When the RAM capacity is 128 KB RAM0: 0000 0000h to 0000 FFFFh (64 KB) RAM1: 0001 0000h to 0001 FFFFh (32 KB)	0000 0000h to 0003 FFFFh
Memory bus	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The on-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. — The number of cycles required is doubled when an access spans an 8-byte boundary. • The RAM can be enabled or disabled.
Data retention function	Data in RAM0 can be retained in deep standby mode.	Not available in deep software standby mode
Low power consumption function	The module stop state is independently selectable for RAM0 and RAM1.	Ability to transition to the module stop state.
Error checking function	—	• Parity check: Detection of 1-bit errors • Generation of non-maskable interrupt or interrupt when an error occurs

Table 2.66 Comparison of RAM Registers

Register	Bit	RX62N	RX671
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.34 Flash Memory

Table 2.67 is a comparative overview of the flash memory, and Table 2.68 is a comparison of flash memory registers.

Table 2.67 Comparative Overview of Flash Memory

Item	RX62N		RX671 (FLASH)	
	ROM	Data Flash	Code Flash Memory	Data Flash Memory
Memory capacity	• User mat: 512 KB, 384 KB, 256 KB • User boot mat: 16 KB	Data mat: 32 KB	User area: 2 MB, 1.5 MB, 1 MB	Data area: 8 KB
Address	• Products with capacity of 512 KB: FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB: FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB: FFFC 0000h to FFFF FFFFh	0010 0000h to 0010 7FFFh	• Products with capacity of 2 MB: FFE0 0000h to FFFF FFFFh • Products with capacity of 1.5 MB: FFE8 0000h to FFFF FFFFh • Products with capacity of 1 MB: FFF0 0000h to FFFF FFFFh	0010 0000h to 0010 1FFFh
ROM cache	—		• Capacity: 8 KB • Mapping method: direct mapping • Line size: 16 bytes	—

Item	RX62N		RX671 (FLASH)	
	ROM	Data Flash	Code Flash Memory	Data Flash Memory
Read cycles	A high-speed read operation takes one cycle of ICLK.	A read operation takes three cycles of PCLK in words or bytes	• While ROM cache operation is enabled: —When the cache is hit: One cycle —When the cache is missed: One to two cycles when ICLK ≤ 60 MHz; two to three cycles when ICLK > 60 MHz • When ROM cache operation is disabled: —One cycle when ICLK ≤ 60 MHz —Two cycles when ICLK > 60 MHz	Reading proceeds in every cycle of FCLK.
Value after erase	FFh	Undfined	FFh	Undfined
Programming/ erasing method	• The MCU incorporates a dedicated sequencer (FCU) for programming of the ROM and data flash. • The ROM and data flash are programmed and erased by issuing commands to the FCU.		• Use of FACI commands specified in the FACI command issuing area (007E 0000h) to program and erase the code flash memory and data flash memory, and to program the option-setting memory (self-programming) • Programming/erasure through communication by a serial-programmer via a serial interface (serial programming)	
Security function	Protects against illicit tampering with or reading out of data in flash memory		Protects against illicit tampering with or reading out of data in flash memory	
Protection function	• Software-controlled protection: The FENTRYR.FENTRY0 and FWEPROR.FLWE[1:0] bits, the DFLREk and DFLWEk registers (k = 0 or 1), and lock bits can be used to prevent unintentional programming. • Error protection: Further programming or erasure is prohibited after detection of abnormal operations during programming or erasure.		Protection against rewriting of the flash memory (software protection, error protection, startup program protection, area protection, and dual bank function)	

Item	RX62N		RX671 (FLASH)	
	ROM	Data Flash	Code Flash Memory	Data Flash Memory
Dual bank function	—		The dual-bank structure makes a safe update possible in cases where programming is suspended. • Linear mode: the code flash memory is used as one area • Dual mode: the code flash memory is divided into two areas	—
Trusted Memory (TM) function	—		Protection against unauthorized reading of the code flash memory • Linear mode: blocks 8, 9 • Dual mode: blocks 8, 9,46, and 47	—
Background operation (BGO) function	• The CPU can execute program code from areas other than the ROM or data flash while the ROM is being programmed or erased. • Execution of program code from the ROM is possible while the data flash is being programmed or erased.		• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user mat or user boot mat: 256 bytes • Units of erasure for the user mat: 4 KB (8 blocks), 16 KB (30 blocks) • Units of erasure for the user boot mat: 16 KB	• Unit of programming for the data mat: 8 bytes or 128 bytes • Unit of erasure for the data mat: 2 KB (16 blocks)	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: 64 bytes, 128 bytes, or 256 bytes

Item	RX62N		RX671 (FLASH)	
	ROM	Data Flash	Code Flash Memory	Data Flash Memory
Other functions	—		• Ability to accept interrupts during self-programming • Ability to specify initial settings for the microcontroller in option-setting memory	
On-board programming (Serial programming/ self-programming)	• Boot mode — The user mat and user boot mat are programmable via the SCI. — The bit rate for SCI communication between the host and RX62N or RX621 can be adjusted automatically. • USB (user) boot mode — It is possible to boot from the user boot mat and program the user mat. — A USB boot program is preprogrammed in the user boot mat when the MCU is shipped from the factory, and the user mat can be programmed using the USB. — By reprogramming the user boot mat it is possible to program the user mat using a user-defined interface. • User program — The user mat can be programmed using a program created by the user.		• Programming/erasing in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Programming/erasing in boot mode (for the USB interface) — USBb is used. — Dedicated hardware is not required, so direct connection to a PC is possible. • Programming/erasing in boot mode (FINE interface) — Uses FINE. • Programming and erasure in single-chip mode — Programming and erasure can be performed by a code flash memory or data flash memory programming routine in a user program.	
Off-board programming	A PROM programmer can be used to program the user mat and user boot mat.	—	A parallel programmer can be used to program and erase the code flash memory and option-setting memory.	A parallel programmer cannot be used to program and erase the data flash memory.
Unique ID	—		A 16-byte ID code provided for each MCU	

Table 2.68 Comparison of Flash Memory Registers

Register	Bit	RX62N	RX671 (FLASH)
FMODR	—	Flash mode register	—
FASTAT	DFLWPE	Data flash programming/erasure protection violation bit	—
	DFLRPE	Data flash read protection violation bit	—
	DFLAE (RX62N) DFAE (RX671)	Data flash access violation bit	Data flash memory access violation flag
	ROMAE (RX62N) CFAE (RX671)	ROM access violation bit	Code flash memory access violation flag
FAEINT	—	Flash access error interrupt enable register	Flash access error interrupt enable register
		Initial values after a reset are different.	
	DFLWPEIE	Data flash programming/erasure protection violation interrupt enable bit	—
	DFLRPEIE	Data flash read protection violation interrupt enable bit	—
	DFLAEIE (RX62N) DFAEIE (RX671)	Data flash access violation interrupt enable bit	Data flash memory access violation interrupt enable bit
	ROMAEIE (RX62N) CFAEIE (RX671)	ROM access violation interrupt enable bit	Code flash memory access violation interrupt enable bit
FCURAME	—	FCU RAM enable register	—
FSTATR0 (RX62N) FSTATR (RX671)	—	Flash status register 0 FSTATR0 is an 8-bit register.	Flash status register FSTATR is a 32-bit register.
	PRGSPD	Programming suspend status bit (b0)	Programming suspend status flag (b8)
	ERSSPD	Erasure suspend status bit (b1)	Erasure suspend status flag (b9)
	DBFULL	—	Data buffer full flag
	SUSRDY	Suspend ready flag (b3)	Suspend ready flag (b11)
	PRGERR	Programming error bit (b4)	Programming error flag (b12)
	ERSERR	Erasure error bit (b5)	Erasure error flag (b13)
	ILGLERR	Illegal command error bit (b6)	Illegal command error flag (b14)
	FRDY	Flash ready bit (b7)	Flash ready flag (b15)
	FLWEERR	—	Flash write/erase protect error flag
	OTERR	—	Other error flag
	SECERR	—	Security error flag
	FESETERR	—	FENTRY setting error flag
	ILGCOMERR	—	Illegal command error flag
FSTATR1	—	Flash status register 1	—

Register	Bit	RX62N	RX671 (FLASH)
FENTRYR	FENTRY0 (RX62N) FENTRYC (RX671)	ROM P/E mode entry 0 bit	Code flash P/E mode entry bit
	FEKEY[7:0] (RX62N) KEY[7:0] (RX671)	Key code bits	Key code bits
FPROTR	—	Flash protection register	—
FRESETR	—	Flash reset register	—
DFLBCCNT	—	Data flash blank check control register	—
FPESTAT	—	Flash P/E status register	—
DFLBCSTAT	—	Data flash blank check status register	—
PCKAR (RX62N) FPCKAR (RX671)	PCKA[7:0]	Peripheral clock notification bits These bits are used to set the peripheral clock (PCLK) during programming and erasure of the ROM or data flash.	Flash sequencer processing clock frequency notification bits These bits are used to set the frequency of the FlashIF clock (FCLK) and notify the flash sequencer of the frequency used.
	KEY[7:0]	—	Key code bits
DFLRE0	—	Data flash read enable register 0	—
DFLRE1	—	Data flash read enable register 1	—
DFLWE0	—	Data flash programming/erasure enable register 0	—
DFLWE1	—	Data flash programming/erasure enable register 1	—
DFLBCCNT	—	Data flash blank check control register	—
DFLBCSTAT (RX62N) FBCSTAT (RX671)	BCST	Blank check status bit	Blank check status flag
ROMCE	—	—	ROM cache enable register
ROMCIV	—	—	ROM cache invalidate register
NCRGn	—	—	Non-cacheable area n address register (n = 0 or 1)
NCRCn	—	—	Non-cacheable area n setting register (n = 0 or 1)
FSADDR	—	—	FACI command processing start address register
FEADDR	—	—	FACI command processing end address register
FSUINITR	—	—	Flash sequencer set-up initialization register
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register

Register	Bit	RX62N	RX671 (FLASH)
FAWMON	—	—	Flash access window monitor register
FSUACR	—	—	Start-up area control register
EEPFCLK	—	—	Data flash memory access frequency setting register
UIDRn	—	—	Unique ID register n (n = 0 to 3)

2.35 Packages

As indicated in Table 2.69, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage. For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.69 Packages

Package Type	Renesas Code	
	RX62N	**RX671**
176-pin LFBGA	○	×
145-pin TFLGA	PTLG0145JB-A	PTLG0145JC-A, PTLG0145KB-A
144-pin LQFP (RX62N) 144-pin LFQFP (RX671)	PLQP0144KA-A	PLQP0144KA-B
100-pin TFLGA	×	○
85-pin TFLGA	○	×
64-pin TFBGA	×	○
64-pin LFQFP	×	○
48-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 145-Pin TFLGA Package (RX671: 0.65 mm Pin Pitch)

Table 3.1 is a comparative listing of the pin functions of 145-pin TFLGA package (RX671: 0.65 mm pin pitch) products.

Table 3.1 Comparative Listing of 145-Pin TFLGA Package Pin Functions (RX671: 0.65 mm Pin Pitch)

145-Pin TFLGA	RX62N	RX671 (0.65 mm Pin Pitch)
A1	AVSS	AVSS0
A2	AVCC	P07/IRQ15/ADTRG0#
A3	VREFL	P40/IRQ8-DS/AN000
A4	P42/IRQ10-B/AN2	P42/IRQ10-DS/AN002
A5	P44/IRQ12/AN4	P45/IRQ13-DS/AN005
A6	P47/IRQ15-B/AN7	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/ AN108
A7	P91/A17-B	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ IRQ10
A8	PD0/D0/POE7#	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
A9	PD3/D3/MTIC11V-B/POE4#	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
A10	PD6/D6/MTIC5V/POE1#	VSS
A11	P60/CS0#-A	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
A12	P62/CS2#-A/RAS#	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
A13	P64/CS4#-A/WE#	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
B1	P03/IRQ11-A/DA0	AVCC1
B2	P07/IRQ15-A/ADTRG0#-A	AVCC0
B3	VREFH	P05/IRQ13
B4	P40/IRQ8-B/AN0	VREFL0
B5	P45/IRQ13-B/AN5	P43/IRQ11-DS/AN003
B6	P90/A16-B	P47/IRQ15-DS/AN007
B7	PD1/D1/POE6#	P91/A17/SCK7/IRQ9
B8	PD5/D5/MTIC5W/POE2#	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
B9	VSS	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
B10	PE0/D8/SSLB1-B	VCC
B11	PE2/D10/POE9#/SSLB3-B	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1
B12	PE1/D9/SSLB2-B	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
B13	PE4/D12/SSLB0-B	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12

145-Pin TFLGA	RX62N	RX671 (0.65 mm Pin Pitch)
C1	P01/TMCI0-A/RxD6-A/IRQ9-A	AVSS1
C2	P05/IRQ13-A/DA1	P02/TMCI1/SCK6/IRQ10/AN109
C3	VSS	VREFH0
C4	P41/IRQ9-B/AN1	P41/IRQ9-DS/AN001
C5	P46/IRQ14/AN6	P46/IRQ14-DS/AN006
C6	P92/A18-B	VSS
C7	PD2/D2/MTIC11W-B/POE5#	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
C8	PD7/D7/MTIC5U/POE0#	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
C9	P61/CS1#-A/SDCS#	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
C10	P63/CS3#-A/CAS#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
C11	PE5/D13/RSPCKB-B/IRQ5-A	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0
C12	PE3/D11/POE8#	P70/SDCLK/IRQ0
C13	SDCLK/P70	VSS
D1	EMLE	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN111
D2	VCC	PF5/IRQ4
D3	P02/TMCI1-A/SCK6-A/IRQ10-A	P03/IRQ11
D4	P43/IRQ11-B/AN3	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN110
D5	VCC	VCC
D6	VSS	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
D7	P93/A19-B	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ POE10#/SSLC1-A/SDHI_CLK-B/QSPCLK-B/ IRQ5/AN102
D8	PD4/D4/MTIC11U-B/POE3#	P60/CS0#/IRQ0
D9	VCC	P64/CS4#/WE#/D3[A3/D3]/IRQ4
D10	VSS	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
D11	VCC	VCC
D12	PE7/D15/MISOB-B/IRQ7-A	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
D13	PE6/D14/MOSIB-B/IRQ6-A	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
E1	VCL	VSS
E2	VSS	VCL
E3	P00/TMRI0-A/TxD6-A/IRQ8-A	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
E4	BSCANP	EMLE
E5	(N.C)	P44/IRQ12-DS/AN004
E10	P65/CS5#-A/CKE	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
E11	P67/CS7#-A/DQM1	P66/CS6#/DQM0/MTIOC7D/IRQ14
E12	PA0/A0/BC0#/MTIOC6A/PO16/SSLA1-B	P65/CS5#/CKE/IRQ13
E13	P66/CS6#-A/DQM0	P67/CS7#/DQM1/MTIOC7C/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT

145-Pin TFLGA	RX62N	RX671 (0.65 mm Pin Pitch)
F3	WDTOVF#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
F4	MDE	VBATT
F10	PA1/A1/MTIOC6B/PO17/SSLA2-B	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
F11	PA3/A3/MTIOC6D/PO19	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
F12	VCC	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
F13	PA2/A2/MTIOC6C/PO18/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/ SMISO12/SSCL12/RXDX12/SDHI_WP/ IRQ10
G1	XTAL	XTAL/P37
G2	VSS	RES#
G3	MD1	MD/FINED
G4	MD0	BSCANP
G10	VSS	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
G11	PA5/A5/MTIOC7B/PO21/RSPCKA-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/ SS12#/IRQ14
G12	PA6/A6/MTIOC8A/PO22/MOSIA-B	VSS_USB
G13	PA4/A4/MTIOC7A/PO20/SSLA0-B	USB1_DP
H1	EXTAL	EXTAL/P36
H2	P34/MTIOC0A/TMCI3/PO12/SCK6-B/ IRQ4-A/TRST#	VCC
H3	VCC	VSS
H4	RES#	UPSEL/P35/NMI
H10	PB0/A8/MTIOC9A/PO24	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ IRQ12
H11	P71/CS1#-B/ET_MDIO	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
H12	PB1/A9/MTIOC9C/PO25	VCC_USB
H13	PA7/A7/MTIOC8B/PO23/MISOA-B	USB1_DM
J1	P33/MTIOC0D/PO11/CRX0/RxD6-B/IRQ3-A	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
J2	P27/CS7#-C/MTIOC2B/PO7/RSPCKB-A/ SCK1/TCK	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
J3	P35/NMI	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2

145-Pin TFLGA	RX62N	RX671 (0.65 mm Pin Pitch)
J4	P32/MTIOC0C/PO10/RTCOUT/CTX0/ TxD6-B/IRQ2-A	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
J10	PB2/A10/MTIOC9B/MTCLKG-B/PO26	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ PMC0-DS/IRQ3
J11	PB4/A12/MTIOC10A/MTCLKE-B/PO28	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
J12	PB5/A13/MTIOC10C/MTCLKF-B/PO29	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
J13	P72/CS2#-B/ET_MDC	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/IRQ4-DS
K1	P30/MTIOC4B-A/TMRI3/PO8/RxD1/ MISOB-A/IRQ0/TDI	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A/IRQ7/TS2
K2	P24/CS4#-C/EDREQ1-B/USB0_VBUSEN-A/ MTIOC4A-A/MTCLKA-A/TMRI1/PO4/ SCK3-B	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
K3	P31/MTIOC4D-A/TMCI2-B/PO9/SSLB0-A/ IRQ1/TMS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
K4	P26/CS6#-C/MTIOC2A/TMO1/PO6/ MOSIB-A/TxD1/TDO	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
K5	BCLK/P53	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/MOSIC-B/IRQ4
K6	VSS	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/ TS12
K7	PC7/A23/CS0#-B/ET_COL/MTIC11U-A/ MTCLKB-B/MISOA-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
K8	P82/EDREQ1-A/ET_ETXD1/RMII_TXD1/ MTIOC4A-B/TRSYNC	VCC
K9	PC3/A19-A/ET_TX_ER/MTCLKF-A/TxD5	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ USB1_EXICEN/SDHI_WP/QIO2-A/IRQ8
K10	PB7/A15/MTIOC10D/PO31	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/SMISO011/SSCL011/ RXD011/SDHI_CMD-A/QSSL-A/IRQ14
K11	P73/CS3#-B/ET_WOL	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
K12	PC0/A16-A/ET_ERXD3/MTCLKG-A/ SSLA1-A	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
K13	PB3/A11/MTIOC9D/MTCLKH-B/PO27	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
L1	P25/CS5#-C/EDACK1-B/USB0_DPRPD/ MTIOC4C-A/MTCLKB-A/PO5/RxD3-B/ ADTRG0#-B	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT

145-Pin TFLGA	RX62N	RX671 (0.65 mm Pin Pitch)
L2	P22/EDREQ0-B/USB0_DRPD/MTIOC3B-A/ MTCLKC-A/TMO0/PO2/SCK0	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
L3	P17/MTIOC3A/PO15/TxD3-A/IRQ7-B	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
L4	P12/TMCI1-B/SCL0/RxD2-A/IRQ2-B	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
L5	VCC_USB	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
L6	P56/EDACK1-C/MTIOC3C-B	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6
L7	P52/RD#/SSLB3-A/RxD2-B	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
L8	P83/EDACK1-A/ET_CRS/RMII_CRS_DV/ MTIOC4C-B/TRCLK	TRCLK/P83/EDACK1/MTIOC4C/SS10#/ CTS10#/SCK10/SS010#/CTS010#/SCK010/ IRQ3
L9	P81/EDACK0-A/ET_ETXD0/RMII_TXD0/ MTIOC3D-B/TRDATA1	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
L10	P77/CS7#-B/ET_RX_ER/RMII_RX_ER	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/ TSCAP
L11	P75/CS5#-B/ET_ERXD0/RMII_RXD0	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
L12	VCC	TRDATA4/P73/CS3#/PO16/USB1_VBUS/ USB1_VBUSEN/USB1_OVRCURB/IRQ8
L13	PB6/A14/MTIOC10B/PO30	VSS
M1	P23/EDACK0-B/USB0_DPUPE-A/ MTIOC3D-A/MTCLKD-A/PO3/TxD3-B	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
M2	P20/USB0_ID/MTIOC1A/TMRI0-B/PO0/ SDA1/TxD0	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
M3	PLLVCC	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/SMISO010/SSCL010/RXD010/ IRQ14
M4	P15/MTIOC0B/TMCI2-A/PO13/SCK3-A/ IRQ5-B	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
M5	P14/USB0_OVRCURA/USB0_DPUPE-B/ TMRI2/IRQ4-B	VCC_USB
M6	VSS_USB	VSS_USB
M7	P55/WAIT#-B/EDREQ0-C/ET_EXOUT/ MTIOC4D-B/TRDATA3	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0

145-Pin TFLGA	RX62N	RX671 (0.65 mm Pin Pitch)
M8	P50/WR0#/WR#/SSLB1-A/TxD2-B	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/SSILRCK0/SMISO010/SSCL010/RXD010/MOSI0-A/IRQ13/TS13
M9	PC6/A22/CS1#-C/ET_ETXD3/MTIC11V-A/MTCLKA-B/MOSIA-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/SMISO10/SSCL10/RXD10/SMISO010/SSCL010/RXD010/USB1_OVRCURB/SDHI_CD/QIO3-A/IRQ9
M10	P80/EDREQ0-A/ET_TX_EN/RMII_TXD_EN/MTIOC3B-B/TRDATA0	TRDATA7/P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/SMOSI011/SSDA011/TXD011/USB1_ID/SDHI_CLK-A/QSPCLK-A/IRQ7
M11	PC2/A18-A/ET_RX_DV/MTCLKE-A/SSLA3-A/RxD5	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/SSCL011/SSL01-A/IRQ14/TS16
M12	PC1/A17-A/ET_ERXD2/MTCLKH-A/SSLA2-A/SCK5	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/TXD011/SMOSI011/SSDA011/TXDA011/SSL02-A/IRQ12/TS15
M13	VSS	VCC
N1	P21/USB0_EXICEN/MTIOC1B/TMCI0-B/PO1/SCL1/RxD0	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/PO1/RXD0/SMISO0/SSCL0/SCL1/USB0_EXICEN/SSILRCK0/SDHI_CLK-C/IRQ9/TS8
N2	P16/USB0_VBUS/USB0_OVRCURB/USB0_VBUSEN-B/MTIOC3C-A/TMO2/PO14/RxD3-A/IRQ6-B	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/SDHI_CMDC/IRQ8/TS9
N3	PLLVSS	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/TXD10/SMOSI010/SSDA010/TXD010/SDHI_D2-C/IRQ15
N4	P13/TMO3/SDA0/TxD2-A/IRQ3-B/ADTRG1#	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA/IRQ4/TS11
N5	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
N6	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
N7	P54/EDACK0-C/ET_LINKSTA/MTIOC4B-B/TRDATA2	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/CRX1/MISOC-B/IRQ10
N8	P51/WR1#/BC1#/WAIT#-D/SSLB2-A/SCK2	VSS
N9	VCC	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/MISOA-A/SSITXD0/SMOSI010/SSDA010/TXD010/MISO0-A/IRQ14
N10	PC5/A21/CS2#-C/WAIT#-C/ET_ETXD2/MTIC11W-A/MTCLKD-B/RSPCKA-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/SMOSI10/SSDA10/TXD10/SMOSI010/SSDA010/TXD010/USB1_VBUSEN/IRQ2
N11	PC4/A20/CS3#-C/ET_TX_CLK/MTCLKC-B/SSLA0-A	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/QIO0-A/IRQ11
N12	P76/CS6#-B/ET_RX_CLK/REF50CK	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/SCK011/RTS011#/DE011/USB1_OVRCURA/SDHI_D2-A/IRQ13

145-Pin TFLGA	RX62N	RX671 (0.65 mm Pin Pitch)
N13	P74/CS4#-B/ET_ERXD1/RMII_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/SS011#/CTS011#/USB1_VBUSEN/ IRQ12

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.2 145-Pin TFLGA Package (RX671: 0.50 mm Pin Pitch)

Table 3.2 is a comparative listing of the pin functions of 145-pin TFLGA package (RX671: 0.50 mm pin pitch) products.

Table 3.2 Comparative Listing of 145-Pin TFLGA Package Pin Functions (RX671: 0.50 mm Pin Pitch)

145-Pin TFLGA	RX62N	RX671 (0.50 mm Pin Pitch)
A1	AVSS	AVSS0
A2	AVCC	P07/IRQ15/ADTRG0#
A3	VREFL	P40/IRQ8-DS/AN000
A4	P42/IRQ10-B/AN2	P42/IRQ10-DS/AN002
A5	P44/IRQ12/AN4	P45/IRQ13-DS/AN005
A6	P47/IRQ15-B/AN7	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/ AN108
A7	P91/A17-B	P92/A18/POE4#/RXD7/SMISO7/SSCL7/ IRQ10
A8	PD0/D0/POE7#	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
A9	PD3/D3/MTIC11V-B/POE4#	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
A10	PD6/D6/MTIC5V/POE1#	VSS
A11	P60/CS0#-A	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
A12	P62/CS2#-A/RAS#	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
A13	P64/CS4#-A/WE#	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
B1	P03/IRQ11-A/DA0	AVCC1
B2	P07/IRQ15-A/ADTRG0#-A	AVCC0
B3	VREFH	P05/IRQ13
B4	P40/IRQ8-B/AN0	VREFL0
B5	P45/IRQ13-B/AN5	P43/IRQ11-DS/AN003
B6	P90/A16-B	P47/IRQ15-DS/AN007
B7	PD1/D1/POE6#	P91/A17/SCK7/IRQ9
B8	PD5/D5/MTIC5W/POE2#	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
B9	VSS	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103
B10	PE0/D8/SSLB1-B	VCC
B11	PE2/D10/POE9#/SSLB3-B	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1
B12	PE1/D9/SSLB2-B	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
B13	PE4/D12/SSLB0-B	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
C1	P01/TMCI0-A/RxD6-A/IRQ9-A	AVSS1
C2	P05/IRQ13-A/DA1	P02/TMCI1/SCK6/IRQ10/AN109
C3	VSS	VREFH0
C4	P41/IRQ9-B/AN1	P41/IRQ9-DS/AN001
C5	P46/IRQ14/AN6	P46/IRQ14-DS/AN006
C6	P92/A18-B	VSS

145-Pin TFLGA	RX62N	RX671 (0.50 mm Pin Pitch)
C7	PD2/D2/MTIC11W-B/POE5#	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
C8	PD7/D7/MTIC5U/POE0#	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
C9	P61/CS1#-A/SDCS#	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
C10	P63/CS3#-A/CAS#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
C11	PE5/D13/RSPCKB-B/IRQ5-A	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ SSLB1-B/IRQ8/ANEX0
C12	PE3/D11/POE8#	P70/SDCLK/IRQ0
C13	SDCLK/P70	VSS
D1	EMLE	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN111
D2	VCC	PF5/IRQ4
D3	P02/TMCI1-A/SCK6-A/IRQ10-A	P03/IRQ11
D4	P43/IRQ11-B/AN3	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN110
D5	VCC	VCC
D6	VSS	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
D7	P93/A19-B	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ POE10#/SSLC1-A/SDHI_CLK-B/ QSPCLK-B/IRQ5/AN102
D8	PD4/D4/MTIC11U-B/POE3#	P60/CS0#/IRQ0
D9	VCC	P64/CS4#/WE#/D3[A3/D3]/IRQ4
D10	VSS	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
D11	VCC	VCC
D12	PE7/D15/MISOB-B/IRQ7-A	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
D13	PE6/D14/MOSIB-B/IRQ6-A	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
E1	VCL	VSS
E2	VSS	VCL
E3	P00/TMRI0-A/TxD6-A/IRQ8-A	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
E4	BSCANP	EMLE
E5	(N.C)	P44/IRQ12-DS/AN004
E10	P65/CS5#-A/CKE	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
E11	P67/CS7#-A/DQM1	P66/CS6#/DQM0/MTIOC7D/IRQ14
E12	PA0/A0/BC0#/MTIOC6A/PO16/SSLA1-B	P65/CS5#/CKE/IRQ13
E13	P66/CS6#-A/DQM0	P67/CS7#/DQM1/MTIOC7C/IRQ15
F1	XCIN	XCIN
F2	XCOUT	XCOUT
F3	WDTOVF#	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
F4	MDE	VBATT
F10	PA1/A1/MTIOC6B/PO17/SSLA2-B	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
F11	PA3/A3/MTIOC6D/PO19	VSS

145-Pin TFLGA	RX62N	RX671 (0.50 mm Pin Pitch)
F12	VCC	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
F13	PA2/A2/MTIOC6C/PO18/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/ SMISO12/SSCL12/RXDX12/SDHI_WP/ IRQ10
G1	XTAL	XTAL/P37
G2	VSS	RES#
G3	MD1	MD/FINED
G4	MD0	BSCANP
G10	VSS	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
G11	PA5/A5/MTIOC7B/PO21/RSPCKA-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/ SS12#/IRQ14
G12	PA6/A6/MTIOC8A/PO22/MOSIA-B	VCC
G13	PA4/A4/MTIOC7A/PO20/SSLA0-B	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
H1	EXTAL	EXTAL/P36
H2	P34/MTIOC0A/TMCI3/PO12/SCK6-B/ IRQ4-A/TRST#	VCC
H3	VCC	VSS
H4	RES#	UPSEL/P35/NMI
H10	PB0/A8/MTIOC9A/PO24	P72/A19/CS2#/IRQ10
H11	P71/CS1#-B/ET_MDIO	P71/A18/CS1#/IRQ1
H12	PB1/A9/MTIOC9C/PO25	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/ RXD6/SMISO4/SMISO6/SSCL4/SSCL6/ IRQ12
H13	PA7/A7/MTIOC8B/PO23/MISOA-B	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7
J1	P33/MTIOC0D/PO11/CRX0/RxD6-B/IRQ3-A	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
J2	P27/CS7#-C/MTIOC2B/PO7/RSPCKB-A/ SCK1/TCK	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
J3	P35/NMI	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
J4	P32/MTIOC0C/PO10/RTCOUT/CTX0/ TxD6-B/IRQ2-A	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
J10	PB2/A10/MTIOC9B/MTCLKG-B/PO26	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/ PMC0-DS/IRQ3
J11	PB4/A12/MTIOC10A/MTCLKE-B/PO28	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4

145-Pin TFLGA	RX62N	RX671 (0.50 mm Pin Pitch)
J12	PB5/A13/MTIOC10C/MTCLKF-B/PO29	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/ RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
J13	P72/CS2#-B/ET_MDC	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/ SSDA4/SSDA6/IRQ4-DS
K1	P30/MTIOC4B-A/TMRI3/PO8/RxD1/ MISOB-A/IRQ0/TDI	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A/IRQ7/TS2
K2	P24/CS4#-C/EDREQ1-B/USB0_VBUSEN-A/ MTIOC4A-A/MTCLKA-A/TMRI1/PO4/ SCK3-B	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
K3	P31/MTIOC4D-A/TMCI2-B/PO9/SSLB0-A/ IRQ1/TMS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
K4	P26/CS6#-C/MTIOC2A/TMO1/PO6/ MOSIB-A/TxD1/TDO	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
K5	BCLK/P53	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/MOSIC-B/IRQ4
K6	VSS	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/ TS12
K7	PC7/A23/CS0#-B/ET_COL/MTIC11U-A/ MTCLKB-B/MISOA-A	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
K8	P82/EDREQ1-A/ET_ETXD1/RMII_TXD1/ MTIOC4A-B/TRSYNC	VCC
K9	PC3/A19-A/ET_TX_ER/MTCLKF-A/TxD5	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ SDHI_WP/QIO2-A/IRQ8
K10	PB7/A15/MTIOC10D/PO31	TRDATA6/P76/CS6#/PO22/SMISO11/ SSCL11/RXD11/SMISO011/SSCL011/ RXD011/SDHI_CMD-A/QSSL-A/IRQ14
K11	P73/CS3#-B/ET_WOL	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
K12	PC0/A16-A/ET_ERXD3/MTCLKG-A/ SSLA1-A	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
K13	PB3/A11/MTIOC9D/MTCLKH-B/PO27	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
L1	P25/CS5#-C/EDACK1-B/USB0_DPRPD/ MTIOC4C-A/MTCLKB-A/PO5/RxD3-B/ ADTRG0#-B	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
L2	P22/EDREQ0-B/USB0_DRPD/MTIOC3B-A/ MTCLKC-A/TMO0/PO2/SCK0	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
L3	P17/MTIOC3A/PO15/TxD3-A/IRQ7-B	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
L4	P12/TMCI1-B/SCL0/RxD2-A/IRQ2-B	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5

145-Pin TFLGA	RX62N	RX671 (0.50 mm Pin Pitch)
L5	VCC_USB	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/SMOSI2/SSDA2/SDA0[FM+]/SDAHS0[FM+/HS]/IRQ3/ADTRG1#
L6	P56/EDACK1-C/MTIOC3C-B	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/RSPCKC-B/IRQ6
L7	P52/RD#/SSLB3-A/RxD2-B	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/IRQ2
L8	P83/EDACK1-A/ET_CRS/RMII_CRS_DV/MTIOC4C-B/TRCLK	TRCLK/P83/EDACK1/MTIOC4C/SS10#/CTS10#/SCK10/SS010#/CTS010#/SCK010/IRQ3
L9	P81/EDACK0-A/ET_ETXD0/RMII_TXD0/MTIOC3D-B/TRDATA1	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/PO29/SCK8/SCK10/RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/IRQ5/TS14
L10	P77/CS7#-B/ET_RX_ER/RMII_RX_ER	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/SSLA0-A/AUDIO_CLK/SS010#/CTS010#/RTS010#/DE010/SSL00-A/SDHI_D1-A/QIO1-A/IRQ12/TSCAP
L11	P75/CS5#-B/ET_ERXD0/RMII_RXD0	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/TXDB011/SSL03-A/SDHI_D3-A/IRQ10
L12	VCC	TRDATA4/P73/CS3#/PO16/IRQ8
L13	PB6/A14/MTIOC10B/PO30	VSS
M1	P23/EDACK0-B/USB0_DPUPE-A/MTIOC3D-A/MTCLKD-A/PO3/TxD3-B	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/TMO0/PO2/SCK0/USB0_OVRCURB/AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
M2	P20/USB0_ID/MTIOC1A/TMRI0-B/PO0/SDA1/TxD0	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0/SDHI_D3-C/IRQ7/ADTRG1#
M3	PLLVCC	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/RXD10/SMISO010/SSCL010/RXD010/IRQ14
M4	P15/MTIOC0B/TMCI2-A/PO13/SCK3-A/IRQ5-B	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
M5	P14/USB0_OVRCURA/USB0_DPUPE-B/TMRI2/IRQ4-B	VCC_USB
M6	VSS_USB	VSS_USB
M7	P55/WAIT#-B/EDREQ0-C/ET_EXOUT/MTIOC4D-B/TRDATA3	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/SSLB1-A/IRQ0
M8	P50/WR0#/WR#/SSLB1-A/TxD2-B	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/SSILRCK0/SMISO010/SSCL010/RXD010/MOSI0-A/IRQ13/TS13
M9	PC6/A22/CS1#-C/ET_ETXD3/MTIC11V-A/MTCLKA-B/MOSIA-A	TRDATA1/P81/EDACK0/MTIOC3D/PO27/SMISO10/SSCL10/RXD10/SMISO010/SSCL010/RXD010/SDHI_CD/QIO3-A/IRQ9
M10	P80/EDREQ0-A/ET_TX_EN/RMII_TXD_EN/MTIOC3B-B/TRDATA0	TRDATA7/P77/CS7#/PO23/SMOSI11/SSDA11/TXD11/SMOSI011/SSDA011/TXD011/SDHI_CLK-A/QSPCLK-A/IRQ7

145-Pin TFLGA	RX62N	RX671 (0.50 mm Pin Pitch)
M11	PC2/A18-A/ET_RX_DV/MTCLKE-A/ SSLA3-A/RxD5	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/ SSCL011/SSL01-A/IRQ14/TS16
M12	PC1/A17-A/ET_ERXD2/MTCLKH-A/ SSLA2-A/SCK5	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/SSDA011/ TXDA011/SSL02-A/IRQ12/TS15
M13	VSS	VCC
N1	P21/USB0_EXICEN/MTIOC1B/TMCI0-B/ PO1/SCL1/RxD0	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
N2	P16/USB0_VBUS/USB0_OVRCURB/ USB0_VBUSEN-B/MTIOC3C-A/TMO2/ PO14/RxD3-A/IRQ6-B	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
N3	PLLVSS	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SMOSI010/SSDA010/TXD010/ SDHI_D2-C/IRQ15
N4	P13/TMO3/SDA0/TxD2-A/IRQ3-B/ADTRG1#	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
N5	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
N6	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
N7	P54/EDACK0-C/ET_LINKSTA/MTIOC4B-B/ TRDATA2	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/MISOC-B/IRQ10
N8	P51/WR1#/BC1#/WAIT#-D/SSLB2-A/SCK2	VSS
N9	VCC	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ MISOA-A/SSITXD0/SMOSI010/SSDA010/ TXD010/MISO0-A/IRQ14
N10	PC5/A21/CS2#-C/WAIT#-C/ET_ETXD2/ MTIC11W-A/MTCLKD-B/RSPCKA-A	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ SMOSI10/SSDA10/TXD10/SMOSI010/ SSDA010/TXD010/IRQ2
N11	PC4/A20/CS3#-C/ET_TX_CLK/MTCLKC-B/ SSLA0-A	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
N12	P76/CS6#-B/ET_RX_CLK/REF50CK	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/ SCK011/RTS011#/DE011/SDHI_D2-A/ IRQ13
N13	P74/CS4#-B/ET_ERXD1/RMII_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/ CTS11#/SS011#/CTS011#/IRQ12

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.3 144-Pin LQFP/144-Pin LFQFP Package

Table 3.3 is a comparative listing of the pin functions of 144-pin LQFP/144-pin LFQFP package products.

Table 3.3 Comparative Listing of 144-Pin LQFP/144-Pin LFQFP Package Pin Functions

144-Pin	RX62N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
1	AVSS	AVSS0
2	P05/IRQ13-A/DA1	P05/IRQ13
3	VCC	AVCC1
4	P03/IRQ11-A/DA0	P03/IRQ11
5	VSS	AVSS1
6	P02/TMCI1-A/SCK6-A/IRQ10-A	P02/TMCI1/SCK6/IRQ10/AN109
7	P01/TMCI0-A/RxD6-A/IRQ9-A	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/AN110
8	P00/TMRI0-A/TxD6-A/IRQ8-A	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/AN111
9	BSCANP	PF5/IRQ4
10	EMLE	EMLE
11	WDTOVF#	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
12	VSS	VSS
13	MDE	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
14	VCL	VCL
15	MD1	VBATT
16	MD0	MD/FINED
17	XCIN	XCIN
18	XCOUT	XCOUT
19	RES#	RES#
20	XTAL	XTAL/P37
21	VSS	VSS
22	EXTAL	EXTAL/P36
23	VCC	VCC
24	P35/NMI	UPSEL/P35/NMI
25	P34/MTIOC0A/TMCI3/PO12/SCK6-B/IRQ4-A/TRST#	TRST#/P34/MTIOC0A/TMCI3/PO12/POE10#/SCK6/SCK0/IRQ4/TS0
26	P33/MTIOC0D/PO11/CRX0/RxD6-B/IRQ3-A	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/PO11/POE4#/POE11#/RXD6/RXD0/SMISO6/SMISO0/SSCL6/SSCL0/CRX0/IRQ3-DS/TS1
27	P32/MTIOC0C/PO10/RTCOUT/CTX0/TxD6-B/IRQ2-A	P32/MTIOC0C/TIOCC0/TMO3/PO10/RTCOUT/RTCIC2/POE0#/POE10#/TXD6/TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
28	P31/MTIOC4D-A/TMCI2-B/PO9/SSLB0-A/IRQ1/TMS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/TAMPI1
29	P30/MTIOC4B-A/TMRI3/PO8/RxD1/MISOB-A/IRQ0/TDI	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/POE8#/RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS/TAMPI0
30	P27/CS7#-C/MTIOC2B/PO7/RSPCKB-A/SCK1/TCK	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/SCK1/RSPCKB-A/IRQ7/TS2

144-Pin	RX62N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
31	P26/CS6#-C/MTIOC2A/TMO1/PO6/ MOSIB-A/TxD1/TDO	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
32	P25/CS5#-C/EDACK1-B/USB0_DPRPD/ MTIOC4C-A/MTCLKB-A/PO5/RxD3-B/ ADTRG0#-B	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
33	P24/CS4#-C/EDREQ1-B/USB0_VBUSEN-A/ MTIOC4A-A/MTCLKA-A/TMRI1/PO4/ SCK3-B	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
34	P23/EDACK0-B/USB0_DPUPE-A/ MTIOC3D-A/MTCLKD-A/PO3/TxD3-B	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6
35	P22/EDREQ0-B/USB0_DRPD/MTIOC3B-A/ MTCLKC-A/TMO0/PO2/SCK0	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
36	P21/USB0_EXICEN/MTIOC1B/TMCI0-B/ PO1/SCL1/RxD0	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
37	P20/USB0_ID/MTIOC1A/TMRI0-B/PO0/ SDA1/TxD0	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
38	P17/MTIOC3A/PO15/TxD3-A/IRQ7-B	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
39	PLLVCC	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SMOSI010/SSDA010/TXD010/ SDHI_D2-C/IRQ15
40	P16/USB0_VBUS/USB0_OVRCURB/ USB0_VBUSEN-B/MTIOC3C-A/TMO2/ PO14/RxD3-A/IRQ6-B	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
41	PLLVSS	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/SMISO010/SSCL010/RXD010/IRQ14
42	P15/MTIOC0B/TMCI2-A/PO13/SCK3-A/ IRQ5-B	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
43	P14/USB0_OVRCURA/USB0_DPUPE-B/ TMRI2/IRQ4-B	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
44	P13/TMO3/SDA0/TxD2-A/IRQ3-B/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
45	P12/TMCI1-B/SCL0/RxD2-A/IRQ2-B	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
46	VCC_USB	VCC_USB
47	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
48	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
49	VSS_USB	VSS_USB
50	P56/EDACK1-C/MTIOC3C-B	P56/EDACK1/MTIOC3C/TIOCA1/SCK7/ RSPCKC-B/IRQ6

144-Pin	RX62N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
51	P55/WAIT#-B/EDREQ0-C/ET_EXOUT/ MTIOC4D-B/TRDATA3	TRDATA3/P55/D0[A0/D0]/WAIT#/EDREQ0/ MTIOC4D/TMO3/TXD7/SMOSI7/SSDA7/ CRX1/MISOC-B/IRQ10
52	P54/EDACK0-C/ET_LINKSTA/MTIOC4B-B/ TRDATA2	TRDATA2/P54/ALE/D1[A1/D1]/EDACK0/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX1/MOSIC-B/IRQ4
53	BCLK/P53	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/ TS12
54	P52/RD#/SSLB3-A/RxD2-B	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
55	P51/WR1#/BC1#/WAIT#-D/SSLB2-A/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
56	P50/WR0#/WR#/SSLB1-A/TxD2-B	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
57	VSS	VSS
58	P83/EDACK1-A/ET_CRS/RMII_CRS_DV/ MTIOC4C-B/TRCLK	TRCLK/P83/EDACK1/MTIOC4C/SS10#/ CTS10#/SCK10/SS010#/CTS010#/SCK010/ IRQ3
59	VCC	VCC
60	PC7/A23/CS0#-B/ET_COL/MTIC11U-A/ MTCLKB-B/MISOA-A	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ MISOA-A/SSITXD0/SMOSI010/SSDA010/ TXD010/MISO0-A/IRQ14
61	PC6/A22/CS1#-C/ET_ETXD3/MTIC11V-A/ MTCLKA-B/MOSIA-A	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
62	PC5/A21/CS2#-C/WAIT#-C/ET_ETXD2/ MTIC11W-A/MTCLKD-B/RSPCKA-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
63	P82/EDREQ1-A/ET_ETXD1/ RMII_TXD1/MTIOC4A-B/TRSYNC	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ SMOSI10/SSDA10/TXD10/SMOSI010/ SSDA010/TXD010/IRQ2
64	P81/EDACK0-A/ET_ETXD0/ RMII_TXD0/MTIOC3D-B/TRDATA1	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ SMISO10/SSCL10/RXD10/SMISO010/ SSCL010/RXD010/SDHI_CD/QIO3-A/IRQ9
65	P80/EDREQ0-A/ET_TX_EN/ RMII_TXD_EN/MTIOC3B-B/TRDATA0	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ SCK10/RTS10#/SCK010/RTS010#/DE010/ SDHI_WP/QIO2-A/IRQ8
66	PC4/A20/CS3#-C/ET_TX_CLK/MTCLKC-B/ SSLA0-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/ IRQ12/TSCAP
67	PC3/A19-A/ET_TX_ER/MTCLKF-A/TxD5	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
68	P77/CS7#-B/ET_RX_ER/RMII_RX_ER	TRDATA7/P77/CS7#/PO23/SMOSI11/ SSDA11/TXD11/SMOSI011/SSDA011/ TXD011/SDHI_CLK-A/QSPCLK-A/IRQ7

144-Pin	RX62N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
69	P76/CS6#-B/ET_RX_CLK/REF50CK	TRDATA6/P76/CS6#/PO22/SMISO11/SSCL11/RXD11/SMISO011/SSCL011/RXD011/SDHI_CMD-A/QSSL-A/IRQ14
70	PC2/A18-A/ET_RX_DV/MTCLKE-A/SSLA3-A/RxD5	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/SMISO5/SSCL5/SSLA3-A/TXDB011/SSL03-A/SDHI_D3-A/IRQ10
71	P75/CS5#-B/ET_ERXD0/RMII_RXD0	TRSYNC1/P75/CS5#/PO20/SCK11/RTS11#/SCK011/RTS011#/DE011/SDHI_D2-A/IRQ13
72	P74/CS4#-B/ET_ERXD1/RMII_RXD1	TRDATA5/P74/A20/CS4#/PO19/SS11#/CTS11#/SS011#/CTS011#/IRQ12
73	PC1/A17-A/ET_ERXD2/MTCLKH-A/SSLA2-A/SCK5	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/SSLA2-A/TXD011/SMOSI011/SSDA011/TXDA011/SSL02-A/IRQ12/TS15
74	VCC	VCC
75	PC0/A16-A/ET_ERXD3/MTCLKG-A/SSLA1-A	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/SSCL011/SSL01-A/IRQ14/TS16
76	VSS	VSS
77	P73/CS3#-B/ET_WOL	TRDATA4/P73/CS3#/PO16/IRQ8
78	PB7/A15/MTIOC10D/PO31	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/SMOSI011/SSDA011/TXD011/IRQ15
79	PB6/A14/MTIOC10B/PO30	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/SMISO011/SSCL011/RXD011/IRQ6
80	PB5/A13/MTIOC10C/MTCLKF-B/PO29	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/IRQ13
81	PB4/A12/MTIOC10A/MTCLKE-B/PO28	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/SS011#/CTS011#/RTS011#/DE011/IRQ4
82	PB3/A11/MTIOC9D/MTCLKH-B/PO27	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/TCLKD/TMO0/PO27/POE11#/SCK4/SCK6/PMC0-DS/IRQ3
83	PB2/A10/MTIOC9B/MTCLKG-B/PO26	PB2/A10/TIOCC3/TCLKC/PO26/CTS4#/RTS4#/CTS6#/RTS6#/SS4#/SS6#/IRQ2
84	PB1/A9/MTIOC9C/PO25	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/TMCI0/PO25/TXD4/TXD6/SMOSI4/SMOSI6/SSDA4/SSDA6/IRQ4-DS
85	P72/CS2#-B/ET_MDC	P72/A19/CS2#/IRQ10
86	P71/CS1#-B/ET_MDIO	P71/A18/CS1#/IRQ1
87	PB0/A8/MTIOC9A/PO24	PB0/A8/MTIC5W/TIOCA3/PO24/RXD4/RXD6/SMISO4/SMISO6/SSCL4/SSCL6/IRQ12
88	PA7/A7/MTIOC8B/PO23/MISOA-B	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/IRQ7
89	PA6/A6/MTIOC8A/PO22/MOSIA-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#/CTS5#/RTS5#/SS5#/MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#/IRQ14
90	PA5/A5/MTIOC7B/PO21/RSPCKA-B	PA5/A5/MTIOC6B/TIOCB1/PO21/RSPCKA-B/RSPCK0-B/IRQ5
91	VCC	VCC

144-Pin	RX62N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
92	PA4/A4/MTIOC7A/PO20/SSLA0-B	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
93	VSS	VSS
94	PA3/A3/MTIOC6D/PO19	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
95	PA2/A2/MTIOC6C/PO18/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/ SMISO12/SSCL12/RXDX12/SDHI_WP/ IRQ10
96	PA1/A1/MTIOC6B/PO17/SSLA2-B	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
97	PA0/A0/BC0#/MTIOC6A/PO16/SSLA1-B	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
98	P67/CS7#-A/DQM1	P67/CS7#/DQM1/MTIOC7C/IRQ15
99	P66/CS6#-A/DQM0	P66/CS6#/DQM0/MTIOC7D/IRQ14
100	P65/CS5#-A/CKE	P65/CS5#/CKE/IRQ13
101	PE7/D15/MISOB-B/IRQ7-A	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
102	PE6/D14/MOSIB-B/IRQ6-A	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
103	VCC	VCC
104	SDCLK/P70	P70/SDCLK/IRQ0
105	VSS	VSS
106	PE5/D13/RSPCKB-B/IRQ5-A	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
107	PE4/D12/SSLB0-B	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
108	PE3/D11/POE8#	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
109	PE2/D10/POE9#/SSLB3-B	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
110	PE1/D9/SSLB2-B	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
111	PE0/D8/SSLB1-B	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ SCK12/SSLB1-B/IRQ8/ANEX0
112	P64/CS4#-A/WE#	P64/CS4#/WE#/D3[A3/D3]/IRQ4
113	P63/CS3#-A/CAS#	P63/CS3#/CAS#/D2[A2/D2]/IRQ3
114	P62/CS2#-A/RAS#	P62/CS2#/RAS#/D1[A1/D1]/IRQ2
115	P61/CS1#-A/SDCS#	P61/CS1#/SDCS#/D0[A0/D0]/IRQ1
116	VSS	VSS
117	P60/CS0#-A	P60/CS0#/IRQ0
118	VCC	VCC
119	PD7/D7/MTIC5U/POE0#	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100

144-Pin	RX62N (144-Pin LQFP)	RX671 (144-Pin LFQFP)
120	PD6/D6/MTIC5V/POE1#	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
121	PD5/D5/MTIC5W/POE2#	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/POE10#/SSLC1-A/SDHI_CLK-B/QSPCLK-B/IRQ5/AN102
122	PD4/D4/MTIC11U-B/POE3#	PD4/D4[A4/D4]/MTIOC8B/POE11#/SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/AN103
123	PD3/D3/MTIC11V-B/POE4#	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/AN104
124	PD2/D2/MTIC11W-B/POE5#	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
125	PD1/D1/POE6#	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/MOSIC-A/IRQ1/AN106
126	PD0/D0/POE7#	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
127	P93/A19-B	P93/A19/POE0#/CTS7#/RTS7#/SS7#/IRQ11
128	P92/A18-B	P92/A18/POE4#/RXD7/SMISO7/SSCL7/IRQ10
129	P91/A17-B	P91/A17/SCK7/IRQ9
130	VSS	VSS
131	P90/A16-B	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0/AN108
132	VCC	VCC
133	P47/IRQ15-B/AN7	P47/IRQ15-DS/AN007
134	P46/IRQ14/AN6	P46/IRQ14-DS/AN006
135	P45/IRQ13-B/AN5	P45/IRQ13-DS/AN005
136	P44/IRQ12/AN4	P44/IRQ12-DS/AN004
137	P43/IRQ11-B/AN3	P43/IRQ11-DS/AN003
138	P42/IRQ10-B/AN2	P42/IRQ10-DS/AN002
139	P41/IRQ9-B/AN1	P41/IRQ9-DS/AN001
140	VREFL	VREFL0
141	P40/IRQ8-B/AN0	P40/IRQ8-DS/AN000
142	VREFH	VREFH0
143	AVCC	AVCC0
144	P07/IRQ15-A/ADTRG0#-A	P07/IRQ15/ADTRG0#

Note: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

3.4 100-Pin LQFP/100-Pin LFQFP Package

Table 3.4 is a comparative listing of the pin functions of 100-pin LQFP/100-pin LFQFP package products.

Table 3.4 Comparative Listing of 100-Pin LQFP/100-Pin LFQFP Package Pin Functions

100-Pin	RX62N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
1	VCC	AVCC1
2	EMLE	EMLE
3	VSS	AVSS1
4	MDE	EXCIN/PJ3/EDACK1/MTIOC3C/CTS6#/ RTS6#/CTS0#/RTS0#/SS6#/SS0#/IRQ11
5	VCL	VCL
6	MD1	VBATT
7	MD0	MD/FINED
8	XCIN	XCIN
9	XCOUT	XCOUT
10	RES#	RES#
11	XTAL	XTAL/P37
12	VSS	VSS
13	EXTAL	EXTAL/P36
14	VCC	VCC
15	P35/NMI	UPSEL/P35/NMI
16	P34/MTIOC0A/TMCI3/PO12/SCK6/IRQ4-A/ TRST#	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/SCK6/SCK0/IRQ4/TS0
17	P33/MTIOC0D/PO11/CRX0/RxD6/IRQ3-A	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/RXD0/ SMISO6/SMISO0/SSCL6/SSCL0/CRX0/ IRQ3-DS/TS1
18	P32/MTIOC0C/PO10/RTCOUT/CTX0/TxD6/ IRQ2-A	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCOUT/RTCIC2/POE0#/POE10#/TXD6/ TXD0/SMOSI6/SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS/TAMPI2
19	P31/MTIOC4D-A/TMCI2/PO9/SSLB0-A/ IRQ1/TMS	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS/ TAMPI1
20	P30/MTIOC4B-A/TMRI3/PO8/RxD1/ MISOB-A/IRQ0/TDI	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/MISOB-A/ IRQ0-DS/TAMPI0
21	P27/CS7#/MTIOC2B/PO7/RSPCKB-A/SCK1/ TCK	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A/IRQ7/TS2
22	P26/CS6#/MTIOC2A/TMO1/PO6/MOSIB-A/ TxD1/TDO	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/TXD1/ CTS3#/RTS3#/SMOSI1/SS3#/SSDA1/ MOSIB-A/IRQ6/TS3
23	P25/CS5#/USB0_DPRPD/MTIOC4C/ MTCLKB-A/PO5/RxD3/ADTRG0#-B	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD/IRQ5/ADTRG0#/TS4/CLKOUT
24	P24/CS4#/USB0_VBUSEN-A/MTIOC4A/ MTCLKA-A/TMRI1/PO4/SCK3	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP/IRQ12/TS5
25	P23/USB0_DPUPE-A/MTIOC3D/ MTCLKD-A/PO3/TxD3	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/CTS0#/RTS0#/SMOSI3/SS0#/ SSDA3/SSIBCK0/SDHI_D1-C/IRQ3/TS6

100-Pin	RX62N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
26	P22/USB0_DRPD/MTIOC3B/MTCLKC-A/ TMO0/PO2/SCK0	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ AUDIO_CLK/SDHI_D0-C/IRQ15/TS7
27	P21/USB0_EXICEN/MTIOC1B/TMCI0/PO1/ RxD0	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1/ USB0_EXICEN/SSILRCK0/SDHI_CLK-C/ IRQ9/TS8
28	P20/USB0_ID/MTIOC1A/TMRI0/PO0/TxD0	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1/USB0_ID/SSIRXD0/ SDHI_CMDC/IRQ8/TS9
29	PLLVCC	P17/MTIOC3A/MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/PO15/POE8#/SCK1/TXD3/ SMOSI3/SSDA3/SDA2-DS/SSITXD0/ SDHI_D3-C/IRQ7/ADTRG1#
30	P16/USB0_VBUS/USB0_OVRCURB/ USB0_VBUSEN-B/MTIOC3C/ TMO2/PO14/IRQ6-B	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/RXD3/ SMOSI1/SMISO3/SSDA1/SSCL3/SCL2-DS/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#
31	PLLVSS	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SCK3/SMISO1/SSCL1/ CRX1-DS/IRQ5/TS10
32	P14/USB0_OVRCURA/USB0_DPUPE-B/ MTIOC3A/TMRI2/PO15/IRQ4-B	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4/TS11
33	P13/MTIOC0B/TMO3/PO13/SDA0/TxD2-A/ IRQ3-B/ADTRG1#	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]/IRQ3/ADTRG1#
34	P12/TMCI1/SCL0/RxD2-A/IRQ2-B	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/SCLHS0[FM+/HS]/IRQ2
35	VCC_USB	VCC_USB
36	USB0_DM	PH2/TMRI0/USB0_DM/IRQ1
37	USB0_DP	PH1/TMO0/USB0_DP/IRQ0
38	VSS_USB	VSS_USB
39	P55/WAIT#-B/MTIOC4D-B	P55/D0[A0/D0]/WAIT#/EDREQ0/MTIOC4D/ TMO3/CRX1/MISOC-B/IRQ10
40	P54/MTIOC4B-B	P54/ALE/D1[A1/D1]/EDACK0/MTIOC4B/ TMCI1/CTS2#/RTS2#/SS2#/CTX1/MOSIC-B/ IRQ4
41	BCLK/P53	P53*1/BCLK/SSIRXD0/PMC0-DS/IRQ3/TS12
42	P52/RD#/SSLB3-A/RxD2-B	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A/ IRQ2
43	P51/WR1#/BC1#/WAIT#-D/SSLB2-A/SCK2	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A/ IRQ1
44	P50/WR0#/WR#/SSLB1-A/TxD2-B	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A/IRQ0
45	PC7/A23/CS0#/ET_COL/MTIC11U-A/ MTCLKB-B/MISOA-A	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/TOC0/PO31/CACREF/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ MISOA-A/SSITXD0/SMOSI010/SSDA010/ TXD010/MISO0-A/IRQ14

100-Pin	RX62N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
46	PC6/A22/CS1#/ET_ETXD3/MTIC11V-A/ MTCLKA-B/MOSIA-A	PC6/D2[A2/D2]/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/PO30/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/MOSIA-A/ SSILRCK0/SMISO010/SSCL010/RXD010/ MOSI0-A/IRQ13/TS13
47	PC5/A21/CS2#/WAIT#-C/ET_ETXD2/ MTIC11W-A/MTCLKD-B/RSPCKA-A	PC5/D3[A3/D3]/A21/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/PO29/SCK8/SCK10/ RSPCKA-A/SSIBCK0/SCK010/RSPCK0-A/ IRQ5/TS14
48	PC4/A20/CS3#/ET_TX_CLK/MTCLKC-B/ SSLA0-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/SSLA0-A/ AUDIO_CLK/SS010#/CTS010#/RTS010#/ DE010/SSL00-A/SDHI_D1-A/QIO1-A/ IRQ12/TSCAP
49	PC3/A19/ET_TX_ER/MTCLKF-A/TxD5	PC3/A19/MTIOC4D/TCLKB/PO24/TXD5/ SMOSI5/SSDA5/PMC0-DS/SDHI_D0-A/ QIO0-A/IRQ11
50	PC2/A18/ET_RX_DV/MTCLKE-A/SSLA3-A/ RxD5	PC2/A18/MTIOC4B/TCLKA/PO21/RXD5/ SMISO5/SSCL5/SSLA3-A/TXDB011/ SSL03-A/SDHI_D3-A/IRQ10
51	PC1/A17/ET_ERXD2/MTCLKH-A/SSLA2-A/ SCK5	PC1/A17/MTIOC3A/TCLKD/PO18/SCK5/ SSLA2-A/TXD011/SMOSI011/SSDA011/ TXDA011/SSL02-A/IRQ12/TS15
52	PC0/A16/ET_ERXD3/MTCLKG-A/SSLA1-A	PC0/A16/MTIOC3C/TCLKC/PO17/CTS5#/ RTS5#/SS5#/SSLA1-A/RXD011/SMISO011/ SSCL011/SSL01-A/IRQ14/TS16
53	PB7/A15/ET_CRS/RMII_CRS_DV/ MTIOC10D/PO31	PB7/A15/MTIOC3B/TIOCB5/PO31/TXD9/ SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/ SMOSI011/SSDA011/TXD011/IRQ15
54	PB6/A14/ET_ETXD1/RMII_TXD1/ MTIOC10B/PO30	PB6/A14/MTIOC3D/TIOCA5/PO30/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SMISO011/SSCL011/RXD011/IRQ6
55	PB5/A13/ET_ETXD0/RMII_TXD0/ MTIOC10C/MTCLKF-B/PO29	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/SCK9/SCK11/SCK011/ IRQ13
56	PB4/A12/ET_TX_EN/RMII_TXD_EN/ MTIOC10A/MTCLKE-B/PO28	PB4/A12/TIOCA4/PO28/CTS9#/RTS9#/ SS9#/SS11#/CTS11#/RTS11#/SS011#/ CTS011#/RTS011#/DE011/IRQ4
57	PB3/A11/ET_RX_ER/RMII_RX_ER/ MTIOC9D/MTCLKH-B/PO27	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/SCK6/ PMC0-DS/IRQ3
58	PB2/A10/ET_RX_CLK/REF50CK/MTIOC9B/ MTCLKG-B/PO26	PB2/A10/TIOCC3/TCLKC/PO26/CTS6#/ RTS6#/SS6#/IRQ2
59	PB1/A9/ET_ERXD0/RMII_RXD0/MTIOC9C/ PO25	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/TXD6/SMOSI6/SSDA6/ IRQ4-DS
60	VCC	VCC
61	PB0/A8/ET_ERXD1/RMII_RXD1/MTIOC9A/ PO24	PB0/A8/MTIC5W/TIOCA3/PO24/RXD6/ SMISO6/SSCL6/IRQ12
62	VSS	VSS
63	PA7/A7/ET_WOL/MTIOC8B/PO23/MISOA-B	PA7/A7/TIOCB2/PO23/MISOA-B/MISO0-B/ IRQ7

100-Pin	RX62N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
64	PA6/A6/ET_EXOUT/MTIOC8A/PO22/ MOSIA-B	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/CTS5#/RTS5#/SS5#/ MOSIA-B/MOSI0-B/CTS12#/RTS12#/ SS12#/IRQ14
65	PA5/A5/ET_LINKSTA/MTIOC7B/PO21/ RSPCKA-B	PA5/A5/MTIOC6B/TIOCB1/PO21/ RSPCKA-B/RSPCK0-B/IRQ5
66	PA4/A4/ET_MDC/MTIOC7A/PO20/SSLA0-B	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/TXD5/SMOSI5/SSDA5/SSLA0-B/ SSL00-B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ5-DS
67	PA3/A3/ET_MDIO/MTIOC6D/PO19	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/RXD5/SMISO5/SSCL5/ IRQ6-DS
68	PA2/A2/MTIOC6C/PO18/SSLA3-B	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/SSL03-B/RXD12/ SMISO12/SSCL12/RXDX12/SDHI_WP/ IRQ10
69	PA1/A1/MTIOC6B/PO17/SSLA2-B	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/SCK5/SSLA2-B/SSL02-B/ SCK12/SDHI_CD/IRQ11
70	PA0/A0/BC0#/MTIOC6A/PO16/SSLA1-B	PA0/A0/BC0#/MTIOC4A/MTIOC6D/TIOCA0/ CACREF/PO16/SSLA1-B/SSL01-B/IRQ0
71	PE7/D15/MISOB-B/IRQ7	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/MISOB-B/SDHI_WP/SDHI_D1-B/ QIO1-B/IRQ7
72	PE6/D14/MOSIB-B/IRQ6-A	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/MOSIB-B/SDHI_CD/SDHI_D0-B/ QIO0-B/IRQ6
73	PE5/D13/RSPCKB-B/IRQ5	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/RSPCKB-B/IRQ5
74	PE4/D12/SSLB0-B	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/PO28/SSLB0-B/IRQ12
75	PE3/D11/POE8#	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ PO26/POE8#/TOC3/CTS12#/RTS12#/ SS12#/IRQ11
76	PE2/D10/POE9#/SSLB3-B	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ PO23/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/SSLB3-B/IRQ7-DS
77	PE1/D9/SSLB2-B	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/PO18/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2-B/IRQ9/ANEX1
78	PE0/D8/SSLB1-B	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ SCK12/SSLB1-B/IRQ8/ANEX0
79	PD7/D7/MTIC5U/POE0#	PD7/D7[A7/D7]/MTIC5U/POE0#/SSLC3-A/ SDHI_D1-B/QIO1-B/IRQ7/AN100
80	PD6/D6/MTIC5V/POE1#	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/SDHI_D0-B/QIO0-B/IRQ6/AN101
81	PD5/D5/MTIC5W/POE2#	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ POE10#/SSLC1-A/SDHI_CLK-B/QSPCLK-B/ IRQ5/AN102
82	PD4/D4/MTIC11U-B/POE3#	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/SDHI_CMD-B/QSSL-B/IRQ4/ AN103

100-Pin	RX62N (100-Pin LQFP)	RX671 (100-Pin LFQFP)
83	PD3/D3/MTIC11V-B/POE4#	PD3/D3[A3/D3]/MTIOC8D/POE8#/TOC2/ RSPCKC-A/SDHI_D3-B/QIO3-B/IRQ3/ AN104
84	PD2/D2/MTIC11W-B/POE5#	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0/ MISOC-A/SDHI_D2-B/QIO2-B/IRQ2/AN105
85	PD1/D1/POE6#	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0/ MOSIC-A/IRQ1/AN106
86	PD0/D0/POE7#	PD0/D0[A0/D0]/POE4#/IRQ0/AN107
87	P47/IRQ15-B/AN7	P47/IRQ15-DS/AN007
88	P46/IRQ14/AN6	P46/IRQ14-DS/AN006
89	P45/IRQ13-B/AN5	P45/IRQ13-DS/AN005
90	P44/IRQ12/AN4	P44/IRQ12-DS/AN004
91	P43/IRQ11/AN3	P43/IRQ11-DS/AN003
92	P42/IRQ10/AN2	P42/IRQ10-DS/AN002
93	P41/IRQ9/AN1	P41/IRQ9-DS/AN001
94	VREFL	VREFL0
95	P40/IRQ8/AN0	P40/IRQ8-DS/AN000
96	VREFH	VREFH0
97	AVCC	AVCC0
98	P07/IRQ15-A/ADTRG0#-A	P07/IRQ15/ADTRG0#
99	AVSS	AVSS0
100	P05/DA1/IRQ13-A	P05/IRQ13

Notes: 1. P53, which is multiplexed as the BCLK pin, cannot be used as an I/O port when the external bus is enabled.

4. Notes on Migration

This section provides the important information regarding differences between the RX671 Group and the RX62N Group. 4.1 Notes on Pin Design describes notes regarding the hardware and 4.2 Notes on Function Settings describes notes regarding the software.

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

Connect a decoupling capacitor rated at 0.22 µF to the VCL pin of the RX671 Group for stabilization of the internal power supply.

4.1.2 Transition to Boot Mode (FINE Interface)

On the RX671 Group a transition to boot mode (FINE interface) occurs when the MD pin is low-level at the time of release from a reset and is then switched to high-level within 20 to 100 msec.

For details on operating modes, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.1.3 Main Clock Oscillator

When connecting a resonator to the EXTAL or XTAL pin of the RX671 Group, select a resonator with an oscillation frequency of 8 MHz to 24 MHz.

4.1.4 Inputting an External Clock

On the RX62N Group it was permissible, when inputting an external clock, to input on the XTAL pin the reverse phase of the clock input on the EXTAL pin. However, this is not permitted on the RX671 Group. Keep this in mind when designing systems.

4.1.5 USB External Connection Circuit

The USB external connection circuit differs on the RX62N Group and RX671 Group.

For details on external connection circuits, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2 Notes on Function Settings

Software operating on the RX62N Group are compatible with some software on the RX671 Group. However, careful evaluation is required since specifications such as operating timing and electrical characteristics are different between the Groups.

This section describes notes on software regarding settings of functions that are different between the RX671 Group and the RX62N Group.

For differences in modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware, listed in 5, Reference Documents.

4.2.1 Exception Vector Table

Addresses allocated in the vector table are fixed on the RX62N Group, but on the RX671 Group the vector addresses are relocatable using the value set in the exception table register (EXTB) as the start address.

4.2.2 Performing RAM Self-Diagnostics on Save Register Banks

On the RX671 Group save register banks are configured in the RAM. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

1. Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
2. Use the SAVE instruction to write data to a bank other than that written to in step 1.
3. Use the RSTR instruction to read data from the bank written to in step 1.

4.2.3 Option-Setting Memory

ID code protection and ID code protection of the on-chip debugger are located in the ROM on the RX62N Group, and in the option-setting memory on the RX671 Group. Note that setting procedures are different between the Groups.

4.2.4 Flash Access Window Setting Register (FAW)

On the RX671 Group, once the access window protect bit (FSPR) in the flash access window setting register (FAW) is written to 0, it cannot be reset to 1.

For further information, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2.5 Software Standby Mode

On the RX671 Group it is possible to select whether the main clock or sub-clock oscillator operates or is stopped in software standby mode. To stop the main clock oscillator, clear the main clock oscillator forced oscillation (MOFXIN) bit in the main clock oscillator forced oscillation control register (MOFCR) to 0.

4.2.6 Operation of Main Clock Oscillation Stop Detection Function

The oscillation stop detection function detects when the operation of the main clock oscillator stops and supplies a LOCO clock using the output of the low-speed on-chip oscillator as the clock source for the system clock, instead of the main clock or PLL clock.

Note that on the RX671 Group, when the HOCO clock is selected as the PLL clock source and the PLL clock is selected as the system clock source, the system clock does not switch to the LOCO clock even if main clock oscillation stop is detected.

4.2.7 Note on RX671 Group 48-Pin Package Products

It is not possible to use the sub-clock and RTC on 48-pin package product versions of the RX671 Group. The sub-clock control circuit is in an unstable state after a cold start, so make sure to set any undefined bits following a cold start.

For further information, refer to the User's Manual: Hardware, listed in 5, Reference Documents.

4.2.8 Inrush Current to VBATT Pin

On the RX671 Group, if the VCC voltage exceeds VBATT + 0.6 V when operating in battery backup mode, current flows from the VCC pin to the VBATT pin via a parasitic diode in the power switch on the VCC side. If this presents a problem, insert a low-dropout diode between the backup power supply and the VBATT pin.

4.2.9 Software Configurable Interrupts

A software configurable interrupt function has been added to the RX671 Group. An interrupt source assigned to each interrupt vector number from 128 to 255 can be selected from multiple sources.

For details on software configurable interrupts, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2.10 Bus Priority

On the RX62N Group the bus priority is fixed such that internal main bus 2 has higher priority than internal main bus 1, but on the RX671 Group the bus priority can be specified in the bus priority control register (BUSPRI).

4.2.11 Watchdog Timer and Independent Watchdog Timer

On the RX671 Group it is possible to select either maskable or non-maskable as the type of the WDT underflow and refresh error interrupts and the IWDT underflow and refresh error interrupts.

4.2.12 Initialization of Port Direction Register (PDR)

The method of initializing the PDR differs between the RX62N Group and RX671 Group, even on products with the same pin count.

4.2.13 Pin Assignments

On the RX62N Group pins are assigned to module functions corresponding to specific port function registers as described in the I/O Ports section of the User's Manual: Hardware, but on the RX671 Group pins can be assigned to multiple modules corresponding to the pin function control registers as described in the Multi-Function Pin Controller (MPC) section of the User's Manual: Hardware.

Note that the pin function control registers are protected by the write-protect register. It is necessary to disable protection before writing to the pin function control registers.

4.2.14 MTIOC Pin Output Level When Counter Stops

During operation with the MTIOC pin set to output, writing 0 to a CSTn bit in TSTRA, TSTRB, or TSTR causes the corresponding counter to stop. At this point, in complementary PWM mode or reset-synchronized PWM mode on the RX671 Group, the output on the MTIOC pin is at the initial output level set in the TOCR1A or TOCR2A register.

In other than complementary PWM mode or reset-synchronized PWM mode, the output compare output level of the MTIOC pin is maintained.

4.2.15 A/D Conversion Start Requests in Complementary PWM Mode

To generate PWM waveforms in complementary PWM mode, MTU4.TGRA (MTU7.TGRA) compare match detection is performed with not only MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB). Therefore, TRGA4N (TRGA7N) is also generated when a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB) occurs.

When operating MTU3 and MTU4 (MTU6 and MTU7) in complementary PWM mode to generate A/D conversion start requests, use compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA or MTU4.TADCORB (MTU7.TADCORA or MTU7.TADCORB) as the A/D conversion start request.

4.2.16 Note on Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX671 Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.2.17 High-Impedance Control of Unselected MTU Pins

On the RX671 Group, when high-impedance control is enabled for MTU pins in the POECR1 or POECR2 register and the control conditions are met, output on the pins multiplexed with the MTU function enters the high-impedance state regardless of whether or not the MTU function is selected.

To prevent pin output from entering the high-impedance state unexpectedly, make settings such that the MTU pins selected in the PmnPFS register of the MPC and the MTU pins selected in the pin selection register of the POE3 match.

4.2.18 Eliminating I^2C Bus Interface Noise

The RX62N Group has integrated analog noise filters on the SCL and SDA lines, but the RX671 Group has no integrated analog noise filters.

4.2.19 Restrictions on Comparison Function

On the RX671 Group the comparison function of the 12-bit A/D converter has the following restrictions:

1. Use of the self-diagnostic function and double-trigger mode are prohibited.
2. When temperature sensor or internal reference voltage is selected for window A, operation of window B is prohibited.
3. When temperature sensor or internal reference voltage is selected for window B, operation of window A is prohibited.
4. The same channel cannot be set for both window A and window B.
5. It is necessary to make settings such that high-side reference value ≥ low-side reference value.

4.2.20 Changing Option-Setting Memory by Self-Programming

Making changes to the option-setting memory by self-programming on the RX671 Group is accomplished by programming the configuration setting area in the option-setting memory using the configuration setting command.

For details on the configuration setting command, refer to RX671 Group Flash Memory User's Manual: Hardware Interface, listed in 5, Reference Documents.

4.2.21 Setting Number of Flash Memory Access Wait States

On the RX671 Group it is necessary to specify the number of access wait states to be used when accessing the flash memory, based on the system clock (ICLK) frequency of the microcontroller. This setting is made to the ROMWT register.

Table 4.1 lists the number of flash memory access wait states, according to ICLK frequency.

Table 4.1 Flash Memory Access Wait States by ICLK Frequency

	ICLK ≤ 60 MHz	60 MHz < ICLK ≤ 120 MHz
Wait states	0 or 1	1

For details on register settings and specifications, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

4.2.22 User Boot Mode

UB code A, UB code B, and user boot mode are implemented on the RX62N Group but not on the RX671 Group.

When using the startup program protection function on the RX671 Group, it is possible to use any interface to program and erase the user area in flash memory as an alternative to user boot mode. For details, refer to Startup Program Protection Function, in RX671 Group Flash Memory User's Manual: Hardware Interface, listed in 5, Reference Documents.

4.2.23 Transferring Firmware to FCU RAM

In order to use FCU commands with the RX62N Group, it is necessary first to store the FCU firmware in the FCU RAM. This step is not necessary for the RX671 Group.

4.2.24 Command Usage with Flash Memory

On the RX62N Group it is possible to program and erase the flash memory by issuing FCU commands to the FCU. On the RX671 Group the FCU can be controlled in order to program and erase the flash memory by setting FACI commands in the FACI command issuance area.

Table 4.2 is a comparison of the specifications of the FCU and FACI commands.

Table 4.2 Specification Comparison of FCU and FACI Commands

Item	FCU Command (RX62N)	FACI Command (RX671)
Command issuance area	Programming/erasure address (00F8 0000h to 00FF FFFFh)	FACI command issuance area (007E 0000h)
Usable commands	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition (lock bit read 1) • Peripheral clock notification • Programming • Block erase • P/E suspend • P/E resume • Status register clear • Lock bit read 2 • Blank checking	• Programming • Block erase • Multi-block erase • P/E suspend • P/E resume • Status clear • Forced end • Blank checking • Configuration settings

4.2.25 ROM Cache

The RX671 Group has the ROM cache, and ROM cache operation is disabled after a reset is released.

To use the ROM cache, set the ROMCE.ROMCEN bit to 1.

4.2.26 Notes on Sub-Clock Oscillator

On the RX671 Group set the SOSCCR.SOSTP bit to 1 (stopping the sub-clock oscillator) within two seconds after release from the reset state.

For details on register settings and specifications, refer to RX671 Group User's Manual: Hardware, listed in 5, Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX62N Group, RX621 Group User's Manual: Hardware, Rev. 1.40 (R01UH0033EJ0140)
(The latest version can be downloaded from the Renesas Electronics website.)

RX671 Group User's Manual: Hardware, Rev. 1.10 (R01UH0899EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

RX Family Design Guide for Migration between RX Family Differences in Package External form (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

- TN-RX*-A193A/E
- TN-RX*-A185B/E
- TN-RX*-A0225A/E
- TN-RX*-A0257A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 14, 2021	—	First edition issued
1.10	May. 20, 2022	124	*Revised:* Table 2.69 Packages
		154	*Added:* 4.2.26 Notes on Sub-Clock Oscillator

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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